RV-8
Receiver
Service Manual

Harman Specialty Group 3 Oak Park, Bedford, MA, 01730-1413 USA
Customer Service: Telephone: 781-280-0300 | Service Fax: 781-280-0499 | www.lexicon.com

Part No. 070-17537 | Rev 0

IMPORTANT SAFETY INSTRUCTIONS

1. Read and keep these instructions.
2. Heed all warnings.
3. Follow all operation instructions.
4. Do not use this apparatus near water.
5. Clean only with a dry cloth.
6. Do not block any ventilation openings.
7. Install in accordance with the manufacturer's instructions.
8. Do not install near any heat sources such as radiators, heat registers, stoves, or another apparatus (including amplifiers) that produces heat.
9. Do not defeat the safety purpose of the polarized or grounding-type plug. A polarized plug has two blades with one wider than the other. A grounding-type plug has two blades and a third grounding prong. The wide blade or the third prong are provided for your safety. If the provided plug does not fit into your outlet, consult an electrician for replacement of the obsolete outlet.
10. Protect the power cord from being walked on or pinched particularly at plugs, convenience receptacles, and the point where they exit from the apparatus.
11. Only use attachments/accessories specified by the manufacturer.
12. Use only with the cart, stand, tripod, bracket, or table specified by the manufacturer, or sold with the apparatus. When a cart is used, use caution when moving the cart/apparatus combination to avoid injury from tip-over.

13. Unplug this apparatus during lightning storms or when unused for long periods of time.
14. Refer all servicing to qualified service personnel. Servicing is required when the apparatus has been damaged in any way, such as when a power-supply cord or plug is damaged, liquid has been spilled or objects have fallen into the apparatus, the apparatus has been exposed to rain or moisture, does not operate normally, or has been dropped.
15. Refer to the operating instructions for power requirements. Be advised that different operating voltages may require the use of different line cord and/or attachment plug.
16. Do not install the unit in an unventilated rack, or directly above heat-producing equipment such as power amplifiers. Observe the maximum ambient operating temperature listed in the product specification.
17. Never attach audio power amplifier outputs directly to any of the unit's connectors.
18. To reduce the risk of fire or electric shock, do not expose this apparatus to rain or moisture.
19. This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of FCC Rules.

These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and radiates radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on. The user is encouraged to try to correct the interference by one or more of the following measures:

- Re-orient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/ television technician for help.

SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this unit. Failure to comply with these precautions or with specific warnings elsewhere in these instructions violates manufacturer safety standards and intended use of this unit. Harman Specialty Group assumes no liability for failure to comply with these requirements.

GROUND THE INSTRUMENT

To minimize shock hazard, the unit chassis and cabinet must be connected to an electrical ground. The unit is equipped with a three-wire grounding type plug. It will only fit into a grounding type power outlet. This is a safety feature. If you are unable to insert the plug into the outlet, contact your electrician to replace your obsolete outlet. Do not defeat the safety purpose of the grounding type plug.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the unit in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must not remove unit covers. Qualified maintenance personnel must make component replacements and internal adjustments. Do not replace components with the power cord connected. Under certain conditions, dangerous voltages may exist even with the power cord removed. To avoid personal injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE

Do not attempt internal service or adjustment unless another person capable of rendering first-aid resuscitation is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the unit.

DANGEROUS PROCEDURE WARNINGS

Warnings such as the example shown below precede potentially dangerous procedures throughout this document. Instructions contained in warnings must be followed.

WARNING

Dangerous voltages capable of causing death are present in this unit. Use extreme caution when handling, testing, or adjusting.

CAUTION

ELECTROSTATIC DISCHARGE (ESD) PRECAUTIONS

The following practices minimize possible damage to circuit boards resulting from electrostatic discharge or improper insertion.

- Keep circuit boards in their original packaging until ready for use.
- Avoid having plastic, vinyl, or Styrofoam in the work area.
- Wear an anti-static wrist strap.
- Discharge personal static before handling circuit boards.
- Remove and insert circuit boards with care.
- When removing circuit boards, handle only by non-conductive surfaces. Never touch open-edge connectors except at a static-free workstation.
- Minimize handling of circuit boards.
- Handle each circuit board by its edges.
- Do not slide circuit boards over any surface.
- Insert circuit boards with the proper orientation.
- Use static-shielded containers for storing and transporting circuit boards.

3 Oak Park
Bedford, MA 01730-1413 USA
Telephone: 781-280-0300
Fax: 781-280-0490
www.lexicon.com

Customer Service
Telephone: 781-280-0300
Sales Fax: 781-280-0495

Service Fax: 781-280-0499

Product Shipments
16 Progress Road
Billerica, MA 01821-5730 USA

A Harman International Company

Part No. 070-17537 | Rev 0 | 07/05

WARNING

These service instructions are only intended for use by qualified personnel. Do not perform any servicing other than that contained in these instructions unless qualified to do so. Refer to the Safety Summary on the previous page prior to performing any service.

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U.S. patent numbers and other worldwide patents issued and pending.

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TABLE OF CONTENTS

CHAPTER 1 – REFERENCE DOCUMENT & EQUIPMENT LISTS 1-1

CHAPTER 2 – GENERAL INFORMATION 2-1

CHAPTER 3 – SPECIFICATIONS 3-1

CHAPTER 4 – FUNCTIONAL VERIFICATION 4-1

- Performance Verification 4-1
- Initial Inspection 4-1
- Functional Tests 4-1
- Functional Audio I/O Tests 4-8
- Audio Performance Verification 4-19
- Video Input/Output Tests 4-22
- Lexicon Audio Precision ATE Summary 4-29

CHAPTER 5 – TROUBLESHOOTING 5-1

- Diagnostic Categories 5-1
- Power On Modes 5-1
- Diagnostic User Interface 5-1
- Diagnostic Reporting 5-2
- Power On Diagnostics 5-6
- Extended Diagnostics Tests 5-8
- Functional Diagnostic Descriptions 5-11
- Disassembly Instructions 5-19

CHAPTER 6 – THEORY OF OPERATION 6-1

- RV-8 Amplifier Theory 6-1
- RV-8 Analog Board Theory 6-4
- RV-8 Main Board Theory 6-9
- RV-8 Phono/Microphone Input Board Theory 6-47
- RV-8 Tuner Board Theory 6-48
- RV-8 Video System Theory 6-50

CHAPTER 7 – PARTS LIST 7-1
Main Board Assembly 7-1
VCO Masterclock Board Assembly 7-3
Microphone/Preamplifier Board Assembly 7-4
Tuner Board Assembly 7-4
IR/Encoder Board Assembly 7-5
Switch/LED Board Assembly 7-5
Headphone Board Assembly 7-6
Analog Input/Output Board Assembly 7-6
3 Channel Amplifier Board Assembly 7-9
4 Channel Amplifier Board Assembly 7-12
Speaker EMI Filter Board Assembly 7-14
Video Board Assembly 7-15
Video In Board Assembly 7-17
Video Out Board Assembly 7-17
Power Supply Board Subassembly 7-17
Chassis Assembly 7-18
FP Mechanical Assembly 7-20
Video Mechanical Assembly 7-20
Tuner/Preamp Mechanical Assembly 7-20
Fan Assembly 7-21
Power Supply Mechanical Assembly 7-21
Bridge Rectifier Assembly 7-21
VCO Mechanical Assembly 7-21
3 Channel Amp Bd Mechanical Assembly 7-21
4 Channel Amp Bd Mechanical Assembly 7-21
Single Positive Heatsink Assembly 7-22
Single Negative Heatsink Assembly 7-22
Double Positive Heatsink Assembly 7-22
Double Negative Heatsink Assembly 7-22
Mounting Bracket Assembly (Option) 7-22
Power Cord Options 7-22
Packaging/Miscellaneous 7-22

ASSEMBLY DRAWINGS

080-14834	PC,ASSY DWG,MECH VCO
080-15508	PC,ASSY DWG,VIDEO IN BD
080-15518	PC,ASSY DWG,VIDEO OUT BD
080-15528	PC,ASSY DWG,MIC/PREAMP BD
080-15538	PC,ASSY DWG,HEADPHONE BD
080-15548	PC,ASSY DWG,TUNER BD
080-15558	PC,ASSY DWG,MAIN BD
080-15568	PC,ASSY DWG,SW/LED BD
080-15578	PC,ASSY DWG,ANLG I/O BD
080-15588	PC,ASSY DWG,VIDEO BD
080-16158	PC,ASSY DWG,AMP MOD,3CH
080-16168	PC,ASSY DWG,AMP MOD,4CH
080-16178	PC,ASSY DWG,PS BD
080-16188	PC,ASSY DWG,SPKR EMI FILT
080-15644	ASSY DWG,SHIPMENT
080-15645	ASSY DWG,ACCESS
080-15646	ASSY DWG,CHASSIS
080-15647	ASSY DWG,MECH,FP
080-15648	ASSY DWG,MECH,VIDEO
080-15649	ASSY DWG,FAN,60MM
080-15848	ASSY DWG,MECH,TUNER/PREAMP
080-16434	ASSY DWG,AMP,3CH
080-16435	ASSY DWG,AMP,4CH
080-16436	ASSY DWG,MECH,PS
080-16437	ASSY DWG,BRIDGE RECT
080-16438	ASSY DWG,HS,SGL
080-16439	ASSY DWG,HS,DBL

SCHEMATICS

060-13699	SCHEM,IR/ENC BD
060-15509	SCHEM,VIDEO IN BD
060-15519	SCHEM,VIDEO OUT BD
060-15529	SCHEM,MIC/PREAMP BD
060-15539	SCHEM,HEADPHONE BD
060-15549	SCHEM,TUNER BD
060-15559	SCHEM,MAIN BD
060-15569	SCHEM,SW/LED BD
060-15579	SCHEM,ANLG I/O BD
060-15589	SCHEM,VIDEO BD
060-16139	SCHEM,VCO BD,MCLK
060-16169	SCHEM,AMP MOD,4CH,3CH
060-16179	SCHEM,PS BD

CHAPTER 1 – REFERENCE DOCUMENT & EQUIPMENT LISTS

Reference Document

Refer to the RV-8 User Guide-Lexicon P/N 070-15838.

Required Equipment

The following is a minimum suggested equipment list required to perform the proof of performance tests:

- High quality amplifier with RCA input connectors and volume control capabilities
- A pair of high quality speakers
- High quality video monitor with composite (RCA), S-video, and component (RCA) input connections
- High quality DVD player with RCA analog L/R outputs, digital coaxial and optical outputs, and composite, S-video and component outputs
- CD disc for a test audio source
- DVD disc for a test video source
- DAT recorder with digital coaxial and optical record inputs, for testing the digital output of the RV-8
- A pair of stereo headphones
- Variac variable AC power supply (2 amp minimum, 0-220 VAC)
- Digital multimeter (3.5 digits, 0.5% or better accuracy)
- Low Distortion Audio Oscillator with single-ended or balanced analog outputs, switchable 30kHz low-pass filter or band-pass (20-20kHz) filter, and output THD+N < .001%
- Distortion Analyzer with switchable 30Hz high-pass filter or band-pass (20-20kHz) filter
- Digital Distortion Analyzer
- RS232 DB9 wrap around plugs (These are created by connecting pins 2 & 3 of a female DB9 connector)
- Debug terminal monitor (optional).

Required Cables

- Shielded audio cable with an RCA connector and an appropriate connector on the opposite end for connection to a Low Distortion Audio Oscillator
- Shielded audio cable with an RCA connector on one end and an appropriate connector on the opposite end for connection to a Low Distortion Audio Analyzer
- Shielded audio cable (balanced) and an XLR female connector on one end and an appropriate connector on the opposite end for connection to a Low Distortion Analyzer
- 4 Shielded audio cables with RCA connectors on both ends
- 2 Shielded AES audio cables with XLR male on one end and XLR female on the other

- Digital S/PDIF audio cable with RCA connectors on both ends
- Digital S/PDIF audio cable with optical connectors on both ends
- 2 Video cables with RCA connectors on both ends
- 2 Video cables with S-Video connectors on both ends
- 2 Video cables with 3-wire component RCA connectors on both ends
- RV-8 AC power cord
- RV-8 remote control.

Required Tools

- Clean, antistatic, well lit work area with grounding wrist strap
- Number 1 Phillips tip screwdriver (magnetic tip preferred)
- Number 2 Phillips tip screwdriver (magnetic tip preferred)
- 1/4 hex nut driver, full hollow
- 7/16 hex nut driver, full hollow
- 9/32 hex nut driver, full hollow
- M8 slotted mini-phone jack driver
- Slim needle nose pliers
- 9/32, 7/16, 1/4 and 3/16, sockets 1/8 drive type
- 1/8-Ratchet wrench
- Magnification glasses and lamp
- Surface Mount Technology (SMT) Soldering/De-soldering bench-top repair station.

CHAPTER 2 – GENERAL INFORMATION

Periodic Maintenance

Under normal conditions the RV-8 requires minimal maintenance. Use a soft, lint-free cloth slightly dampened with warm water and a mild detergent to clean the exterior surfaces of the unit.

Do not use alcohol, benzene or acetone-based cleaners or any strong commercial cleaners. Avoid using abrasive materials such as steel wool or metal polish. It the unit is exposed to a dusty environment, a vacuum may be used to remove dust from the unit's exterior.

Ordering Parts

When ordering parts, identify each part by type, board assembly location, component location, price and HSG/Lexicon Part Number.

Replacement parts can be ordered from:

Harman Specialty Group
3 Oak Park Drive
Bedford, MA 01730-1441
Telephone: 781-280-0300; Fax: 781-280-0499; email: csupport@harmanspecialtygroup.com
ATTN: Customer Service

Returning Units to HSG/Lexicon for Service

Before returning a unit for warranty or non-warranty service, consult with HSG/Lexicon Customer Service to determine the extent of the problem and to obtain Return Authorization. No equipment will be accepted without Return Authorization from HSG/Lexicon.

If HSG/Lexicon recommends that a RV-8 be returned for repair and you choose to return the unit to HSG/Lexicon for service, HSG/Lexicon assumes no responsibility for the unit in shipment from the customer to the factory, whether the unit is in or out of warranty. All shipments must be well packed (using the original packing materials if possible), properly insured and consigned, prepaid, to a reliable shipping agent.

When returning a unit for service, please include the following information:

- Name
- Company Name
- Street Address
- City, State, Zip Code, Country
- Telephone number (including area code and country code where applicable)
- Serial Number of the unit
- Description of the problem
- Preferred method of return shipment
- Return Authorization number (on both the inside and outside of the package).

Please enclose a brief note describing any conversations with HSG/Lexicon personnel (indicate the name of the person at HSG/Lexicon) and give the name and daytime telephone number of the person directly responsible for maintaining the unit.

Do not include accessories such as manuals, cables, remote control, etc. with the unit, unless specifically requested to do so by HSG/Lexicon Customer Service personnel.

CHAPTER 3 – SPECIFICATIONS

Audio Input and Output Connectors

Analog Audio Inputs	8 stereo (RCA) or 5 stereo and one 5.1-channel or 2 stereo and two 5.1-channel connectors
Digital Audio Inputs	4 S/PDIF coaxial (RCA) and 4 S/PDIF optical connectors; coaxial and optical input connectors conform to IEC-958, S/PDIF standards
Sample Rates:	44.1, 48, 88.2, 96kHz
Accepts	16-24 bits PCM audio, Dolby Digital, DTS, DTS-ES and DTS-96k discrete data formats
Main Audio Outputs	8 Unbalanced (RCA) connectors for Front L/R, Center, Sub, Side L/R and Rear L/R
Zone 2 Audio Outputs	1 Unbalanced (RCA, variable output level) stereo connector, 1 Unbalanced (RCA, fixed output level) stereo connector, 1 S/PDIF coaxial (RCA) connector and 1 optical connector
Zone 3 Audio Output	1 Stereo (RCA, variable output level) connector
Headphone Output	1 Stereo (1/4-inch phone) connector
Amplifier Outputs	7 Channels, 2 channels assignable to Zone 2 or Zone 3

Main Zone Audio Performance

A/D Conversion	24-bit, 96kHz, multi-bit $\Delta\Sigma$ architecture
D/A Conversion	24-bit, 44.1 to 192kHz, multi-bit $\Delta\Sigma$ architecture
Frequency Response*	20Hz to 20kHz, +0.1dB/-0.1dB, -0.25dB at 10Hz, -0.5dB at 40kHz, reference 1kHz
THD + Noise*	Below 0.02%, 20Hz to 20kHz, 140Wrms all channels driven
Dynamic Range*	105dB minimum, 22kHz bandwidth, “A” weighted; 102dB minimum, 22kHz bandwidth, unweighted
Signal-to-Noise Ratio*	105dB minimum, 22kHz bandwidth, “A” weighted; 102dB minimum, 22kHz bandwidth, unweighted
Input Sensitivity	200mVrms (2Vrms for maximum output level) at 0dB input gain
Input Impedance	100kΩ in parallel with 150pF

**** Combined measurements of preamplifier and power amplifier sections***

Preamp Output Level	150mVrms typical, 6Vrms maximum (RCA connectors) Maximum value with full-scale input signal and volume at +12dB
Preamp Output Impedance	500Ω in parallel with 150pF (RCA connectors)

* Combined measurements of preamplifier and power amplifier sections

Zone 2 and Zone 3 Audio Performance

A/D Conversion	24-bit, 44.1 to 96kHz, multi-bit ΔΣ architecture (Zone 2 only)
D/A Conversion	24-bit, 44.1 to 192kHz, multi-bit ΔΣ architecture
Frequency Response	10Hz to 20kHz, +0.1dB/-0.25dB, -0.75dB at 40kHz, reference 1kHz
THD + Noise	Below 0.005% at 1kHz, (1Vrms output level)
Dynamic Range	101dB minimum, 22kHz bandwidth
Signal-to-Noise Ratio	101dB minimum, 22kHz bandwidth
Input Sensitivity	200mVrms (4Vrms for maximum output level)
Input Impedance	100kΩ in parallel with 150pF
Preamp Output Level	200mVrms typical, 4Vrms maximum; maximum value with full-scale input signal and volume at 0dB
Preamp Output Impedance	300Ω in parallel with 150pF

Video Input and Output Connectors

Video Inputs	5 composite (RCA), 5 S-video and 3 component video (RCA)
Video Outputs	5 composite (RCA), (2 monitor, 2 Zone2, 1 Zone3), 4 S-video (2 monitor, 2 Zone2) and 1 component (RCA)

Composite and S-video Performance

Compatibility	NTSC, PAL and SECAM
Switching	Active
Output Level	1.0V peak-to-peak
Impedance	75Ω

Input Return Loss	>40dB
Differential Gain	<0.5%
Differential Phase	<0.5°
Bandwidth	>25MHz
K Factor	<0.3%
Gain	±0.15dB
Signal-to-Noise Ratio	>65dB
Frequency Response	10Hz to 10MHz + 0.1/-0.3dB

Component Video Performance

Compatibility	3-Channel (Y/Pb/Pr), format-independent
Switching	Passive
Impedance	75Ω
Bandwidth	>150MHz
Insertion Loss	<3dB
Video Converter	NTSC, PAL, SECAM to Y/Pb/Pr

Other

Trigger Outputs	1 Power on/off and 1 programmable connector on detachable screw terminals (+12 VDC, 0.5 amps each)
RS-232 Serial Input/Output	2 9-pin D-sub connectors
Power Requirements	120/230 VAC, 50-60Hz, 1300W (universal line input), detachable power cord

Dimensions & Weight

Height (with feet): 7.76 inches (197.1mm)

Width: 17.3 inches (440mm)

Depth: 21.2 inches (538.48mm)

Weight: 65lb (29.48kg)

Rack Mounting	Optional brackets are available for installation in a standard 19-inch equipment rack (4 rack units required)
Environment	**Operating Temp:** 0° to 35°C (32° to 95°F)
	Storage Temp: -30° to 75°C (-22° to 167°F)
	Relative Humidity: 95% maximum without condensation
Remote Control	Hand-held, backlit infrared remote control unit, preprogrammed & learning
	Requires 4 AAA batteries (alkaline batteries recommended)

FM Tuner Performance

Tuning Range	64MHz to 108MHz
Usable Sensitivity	<4uV, 1.6uV typical
Selectivity	>87dbmV, 93dbmV typical
Frequency Response	50Hz to 16kHz, +0.1dB/-1.0dB
THD + Noise	Below 0.4% at 1 kHz (stereo)
Signal-to-Noise Ratio	50dB minimum at 60dBmV (stereo, A-Wtg)
Image Rejection	>50dB, >60dB typical
AM Suppression	>45dB, >55dB typical

AM Tuner Performance

Tuning Range	520 to 1720kHz
Usable Sensitivity	<8uV, typ. 4uV
THD + Noise	<0.56%, 0.32% typical (1kHz, 60dBmV, 30% mod)
Wideband AGC	>80dBmV

Phono Performance (MM)

Frequency Response	50Hz to 20kHz, ±0.5dB, rumble filter -4dB at 10Hz
THD + Noise	Below 0.02%, 20Hz to 20kHz, 4.7mV input
Signal-to-Noise Ratio	72dB minimum

Compatible Amplifier Connectors

Banana Plugs	Standard 0.75 inch plugs
Spade Connectors	Size 10-12 gauge
Bare Wire	Up to 10 gauge bare wire

**** Specifications are subject to change without notice.***

CHAPTER 4 – FUNCTIONAL VERIFICATION

PERFORMANCE VERIFICATION

This section describes a quick verification of the operation of the RV-8 and the integrity of its analog and digital audio signal paths.

WARNING

Dangerous voltages capable of causing death are present in this unit. Use extreme caution when handling, testing, or adjusting.

INITIAL INSPECTION

1. Inspect the RV-8 for obvious signs of misuse, abuse, or neglect.
2. With the power off, verify that all switches operate smoothly.
3. With the power off and AC cord disconnected, remove the RV-8 top cover.
4. Verify that all cables are correctly installed and are securely fastened.
5. Check for burnt or obviously damaged components.
6. Check the voltage select connector for the primary windings of the power transformer for the analog power supply: J14=220VAC, J15=120VAC.
7. Put the cover back on.
8. Connect the AC cord. Using the main power switch on the back of the RV-8, verify that the unit runs through its Power On Diagnostics.
9. Check each of the front panel switches for smooth mechanical operation. Verify each LED turns on and off when the associated switch is depressed, and that the display acknowledges each switch function.
10. Press each button on the remote and verify that the RV-8 responds to all the remote commands.

FUNCTIONAL TESTS

The following tests verify the basic functions of the RV-8.

Power Supply Tests

The main power supply in the RV-8 has an operational range of 120/230 VAC, 50-60Hz, 1300W. The following test is for North American line voltage of 120VAC.

Test:

1. Set the Variac to the voltage the unit is configured for (0-220 VAC) .
2. Verify that the RV-8 is powered off at its rear panel power switch.
3. Connect the AC power cord to the RV-8 AC power connector.
4. Check for power supply shorts to ground.

5. Turn on the RV-8 using the rear main power switch.
6. Power on the Variac at 220VAC or 120VAC.
7. Monitor the current draw. During the boot, the current draw should be ~175mA. At the end of the boot, when the power amp is on, the current should be ~375mA.

Safety – Complete Supply Test

These tests will verify that the High Current Power Supply operates properly.

Setup:

1. Set the rear panel power switch of the RV-8 to the “0” (OFF) position.
2. Disconnect the AC Line cord from the unit.
3. Plug the transformer primary wiring harness into the connector J15 “120VAC” on the Power Supply Board to the left of the transformer.
4. Set the Digital Multi-Meter (DMM) for a DC resistance reading on the highest range.
5. Set the rear panel power switch of the RV-8 to the “1” (ON) position.

Test:

1. Verify the resistance between the Line (Brown) pin and chassis ground is an open circuit.
2. Verify the resistance between the Neutral (Blue) pin and chassis ground is an open circuit.
3. Install the top cover (P/N 700-15809).

Power On – Complete Supply Test

This test will verify that there are no shorts from the transformer secondary winding to ground.

WARNING

Lethal voltage will be present during this test. DO NOT come into contact with the Amplifier Output Transistors or the Heat Sinks. Power Supply Discharge time is more than ten minutes unless discharged using a discharge box.

Setup:

1. Set the rear panel power switch of the RV-8 to the "0" (OFF) position.
2. Connect one end of the AC power cord to the RV-8 and the other end to the Variac.
3. Power on the Variac.
4. Set the Variac voltage to 120VAC. Test.

Test:

1. Set the rear panel power switch of the RV-8 to the "1" (ON) position.
2. While monitoring the current draw on the Variac, after approximately sixty seconds, verify that the current draw is less than 1.0A (0.85A typical) and all seven amplifier channel LEDs are lit.

Brown-Out Test

This test verifies that the unit responds to a brown-out (reduction in AC Line Voltage).

Setup:

1. The RV-8 should be powered-on normally through the Variac.
2. Wait for the RV-8 to complete its power-up initialization.
3. Verify that all seven of the Amp Status LEDs at the bottom of the front panel are lit.

Test:

1. Slowly turn the Variac voltage down until the RV-8 display indicates:
   "********BROWN OUT !! ****
   ****CYCLE POWER ****"
2. Verify that all seven of the Amp Status LEDs at the bottom of the front panel are OFF.
3. Set the Digital Multi-Meter (DMM) to measure AC Volts reading on the highest range.
4. Disconnect the AC Line cord from the rear of the RV-8.
5. Verify the voltage at the AC Line cord is between 80 and 90 VAC.

Power Supplies

The following tests and information will verify the voltages and handling issues of the RV-8.

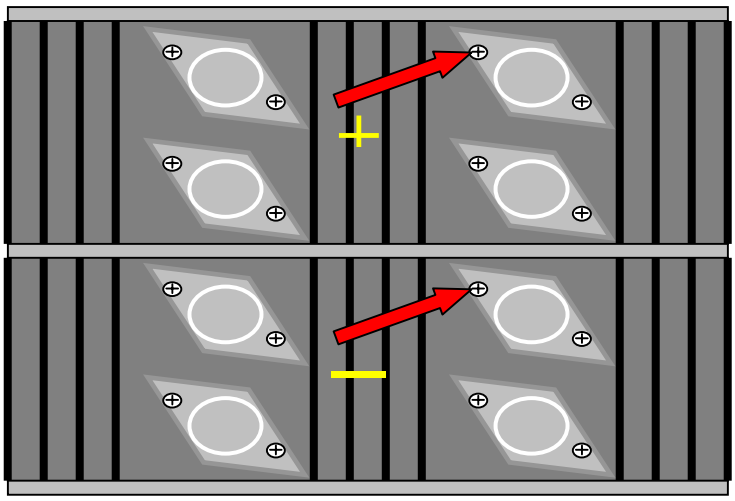
Lethal voltages are present on the RV-8 heat sinks. DO NOT come into contact with the Amplifier Output Transistors or the heat sinks. Power Supply Discharge time is more than ten minutes unless manually discharged.

Whenever the RV-8 covers are removed, the amplifier channels carry a lethal voltage. Stay clear of them when testing the inside of the RV-8. When replacing the channels, it is important to discharge them before removing them from the chassis. Follow the safety and handling procedures below when service is required inside the RV-8.

Discharging The Power Supply:

1. The unit must be disconnected from the AC Power before it is discharged.
2. Wait ten minutes.
3. Remove the top cover and measure the voltage from positive (+) to negative (-). See figure 1 below.

Figure 1: Measure the Voltage from Positive to Negative



Changing the Voltage

This procedure gives instructions for changing an RV-8 from 120V to 220-240 VAC.

1. Disconnect the RV-8 from AC Power.
2. Wait ten minutes.
3. Remove the cover of the RV-8.
4. Measure the voltage on the output devices.
5. Replace the fuse with the proper value (see table below for part number listing).
6. Move the Transformer primary wire harness to the proper connector (see table below for connector information).
7. Replace the rear panel Voltage label with the appropriate label for the configured voltage (Part number 740-16015: LABEL,100-120V,50-60Hz; Part number 740-16017: LABEL,220-240V,50-60Hz).

Item	Description	120VAC	220-240VAC
1	AC Fuse on Power Supply PCB	440-16213 15A	440-16212 6.3A
2	Transformer primary wire harness	Plug to 100V/120V connector J15	Plug to 220V/230V/240V connector J14

Measuring Power Supply Voltages

In this procedure, testing of the supplies will be performed with the top cover removed and the unit turned on. Due to risk of shock, do not remove the cover with the unit powered on.

WARNING

The Amp channels on both sides of the RV-8 heat sinks are Live Voltage. Great care must be taken to avoid touching these areas when testing for voltages inside the unit.

1. Disconnect power.
2. Wait ten minutes.
3. Remove the top cover of the RV-8.
4. With the RV-8 facing you, locate the switching power supply mounted vertically on the left side of the chassis.
5. Power on the unit.

6. Locate the wire connection at the top of the switching supply.
7. With the DMM, measure the voltages on the connector using the black probe to chassis.
8. Yellow is +15 volt rail measure for a voltage range of +14.75V to +15.250V.
9. Blue is –15 volt rail measure for a voltage range of +14.75V to +15.250V.
10. Red is +5 volt rail measure for a voltage range of +4.75V to +5.25V.
11. Locate the two black six-wire connectors that run from the main power supply board in the middle of the RV-8 to the two amp channels left and right of the chassis.
12. With the black lead of the DMM connected to the chassis, carefully probe the inside of each black wire with the red probe. (Some pins contain +65V. Some pins contain -65V).

AM/FM Tuner & Headphone Output Tests

These tests confirm that the tuner and the headphone output in the RV-8 are functioning normally.

Test:

1. Attach both the AM and FM antennas to the back of the RV-8.
2. Connect the RCA front left and right outputs of the RV-8 to the external amplifier left and right inputs. Connect the outputs of the external amplifier to the pair of speakers.
3. Power on the RV-8.
4. Press the remote control **MAIN** soft button.
5. Press the remote **TUNER** soft button.
6. The RV-8's display will display "Tuner" in the upper left, and the AM or FM radio station it is tuned to in the upper right.
7. Raise the RV-8 volume to a comfortable level.
8. Randomly scan to different radio stations by pushing the **TUNE/SEEK** buttons on the front panel or remote control, stopping at each station to listen for clarity.
9. Switch between the AM and FM bands by pressing the **AM/FM** button on the front panel or remote control, checking stations for clarity.
10. Power down the external amplifier. Remove the cables from the outputs of the amplifier and connect them to the RV-8's front left and right amplifier outputs.
11. Repeat steps 7 and 8 above, adjusting the volume on the front panel of the RV-8 to a comfortable listening level.
12. Lower the volume on the RV-8, and plug a pair of headphones into the **Phones** jack on the front panel.
13. Repeat steps 7 and 8 above adjusting the volume on the front panel of the RV-8 to a comfortable listening level.

Trigger Test

This test will verify the trigger circuits of the RV-8. For this test you will need the RV-8 remote control and a Digital Multimeter (DMM).

Test:

1. Power on the RV-8.
2. Turn on the DMM and set it to read DC voltage for a 12V level.
3. Using the remote control Menu ▸ arrow, select SETUP from the Main Menu.
4. Scroll down through the SETUP menu and select TRIGGERS.
5. Scroll to DVD1 and change the trigger from OFF to ON.
6. Press the remote control **MAIN** button, then press the remote control **DVD1** button to select DVD1 as the input for the Main Zone.
7. On the RV-8 rear panel, locate the Trigger Outputs block.
8. Connect the DMM's red probe to positive (+) and connect the black probe to negative (–). Measure the PWR +/- and the #1 +/- trigger outputs for 12 Volts DC.

RS232 Test

This test will verify that the RS232 port 1 on the back of the RV-8 is functioning normally by comparing the transmitted signal (at pin 2) to the received signal (at pin 3).

Test:

1. Connect the video monitor to the main composite video output of the RV-8 and turn the monitor on. This will allow full viewing of the RV-8's Diagnostics menus.
2. Power on the RV-8 using the main power switch on the rear panel.
3. When "LEXICON" appears on the display, press and hold the **Zone2 DVD2** and **Zone3 DVD2** buttons on the front panel within eight seconds.
4. Continue to hold down the buttons until the RV-8 display reads "DIAGS MENU FUNCTIONAL TESTS."
5. Turn the **volume knob** until "REPAIR TESTS" is displayed on the front panel.
6. Press the **Mode** ▸ button on the front panel to enter the REPAIR TEST menu.
7. Turn the **volume knob** to the right until "RS232 WRAP TEST" appears on the display.
8. Press the front panel **Mode** ▸ button until the display reads "INSERT WRAP PLUGS."
9. Connect the wraparound plugs to pins 2 and 3 of the female DB9 connector labeled "RS232 1" on the back of the RV-8.
10. Press the **Mode** ▸ button to engage the test.
11. The display should read "SERIAL PORT 1 PASSED" and "SERIAL PORT 2 FAILED."

FUNCTIONAL AUDIO I/O TESTS

***Note**:*
The DVD1 input will be used throughout the functional audio I/O tests. Any other input may be substituted as desired. You will need the RV-8 remote control throughout to configure the Setup menus.

Analog Inputs to Zone2 Outputs Test

This test will verify the audio path between the paired inputs labeled 1 to 8 and the fixed and variable RCA Zone 2 output.

Setup:

1. Connect the video monitor to the main composite output of the RV-8 and turn the monitor on. This will allow full viewing of the of the RV-8's menus.
2. Connect the RCA left and right outputs labeled "Fix" from Zone 2 to an external amplifier.
3. Connect the outputs of the external amplifier to the pair of speakers.
4. If the RV-8 is powered off, turn on using the main power switch on the rear panel.
5. Once the unit is in standby mode, press the front panel **standby button** or the remote control **POWER button** to enter normal operation.

Test:

1. To enter the MAIN MENU, press the remote control Menu ▸ arrow.
2. Scroll to the MAIN MENU using the Menu ▲/▼ arrows and highlight SETUP. Press the Menu ▸ arrow to enter SETUP.
3. In the SETUP menu, highlight INPUTS. Press the Menu ▸ arrow to enter INPUT SETUP.
4. Highlight DVD1 and press the Menu ▸ arrow button to select the DVD1 INPUT SETUP menu.
5. Scroll down through the DVD1 menu options and highlight ANALOG IN. Press the Menu ▸ arrow to enter DVD1 ANALOG IN.
6. Scroll through the DVD1 ANALOG IN input options and highlight ANALOG-1. Press the Menu ▸ arrow to assign the input to DVD1.
7. Press the Menu ◂ arrow once to return to the DVD1 INPUT SETUP menu.
8. Scroll down through the menu and highlight ZONE2 IN. Press the Menu ▸ arrow to select the ZONE2 IN parameter.
9. Press the Menu ▲/▼ arrows until ANLG is listed.
10. Press the Menu ◂ arrow once to confirm.
11. Analog should now be selected as the Zone 2 source.
12. Press the Menu ◂ arrow four times to exit the setup menus.
13. Connect the oscillator output to the left and right audio inputs labeled 1 on the RV-8 rear panel.
14. Confirm DVD 1 is selected in the Main Zone as well as the Zone 2 section of the front panel.
15. Slowly increase the volume on the amplifier to a comfortable listening level for the speakers.
16. Sweep the oscillator from 20Hz to 20kHz.
17. Verify that you hear clean, clear audio coming from the speakers.

18. Power down the amplifier and move the cables from RCA left and right outputs from “Fix” to “Var” in Zone 2.
19. Repeat the procedure above to test the Zone 2 variable output.
20. Once complete, repeat steps 1-19 to test Analog Inputs 2 through 8. Change the DVD1 ANALOG IN selected in step 6 to the next appropriate input.

Analog Inputs to Zone 3 Output Test

This test will verify the audio path between the paired inputs 1 to 8 and the RCA Zone 3 output.

Setup:

1. Connect the video monitor to the main composite output of the RV-8 and turn the monitor on. This will allow full viewing of the RV-8’s menus.
2. Connect the Zone 3 RCA left and right audio outputs to an external amplifier.
3. Connect the outputs of the external amplifier to the pair of speakers.
4. If the RV-8 is powered down, turn it on using the main power switch on the rear panel.
5. Once the unit is in standby mode, press the front panel **standby button** or the remote control **POWER button** to enter normal operation.

Test:

1. To enter the MAIN MENU, press the remote control Menu ▸ arrow.
2. Scroll through the MAIN MENU using the ▲/▼ arrows and highlight SETUP. Press the Menu ▸ arrow to enter SETUP.
3. In the SETUP menu, highlight INPUTS. Press the Menu ▸ arrow to enter INPUT SETUP.
4. Highlight DVD1 and press the Menu ▸ arrow to select the DVD1 INPUT SETUP menu.
5. Scroll down through the DVD1 menu options and highlight ANALOG IN. Press the Menu ▸ arrow to enter DVD1 ANALOG IN.
6. Scroll through the DVD1 ANALOG IN input options and highlight ANALOG-1. Press the Menu ▸ arrow to assign the input to DVD1.
7. Press the Menu ◂ arrow button four times to exit the setup menus.
8. Connect the oscillator output to the left and right audio inputs labeled 1 on the rear panel of the RV-8.
9. Confirm DVD 1 is selected in the Main Zone as well as the Zone 3 section of the front panel.
10. Slowly increase the volume on the amplifier to a comfortable listening level for the speakers.
11. Sweep the oscillator from 20Hz to 20kHz.
12. Verify that clean, undistorted audio can be heard from the Zone 3 audio outputs of the RV-8.
13. Once complete, repeat steps 1-12 to test Analog Inputs 2 through 8 to the audio output of Zone3. Change the DVD1 ANALOG IN selected in step 6 to the next appropriate input.

Analog Inputs to Digital Outputs Test

This test will verify the audio path between the paired analog inputs 1 to 8 to Zone 2 digital outputs.

Setup:

1. Connect the video monitor to the main composite output of the RV-8 and turn the monitor on. This will allow full viewing of the of the RV-8's menus.
2. Connect the S/PDIF coaxial digital output of Zone 2 on the RV-8 rear panel to the digital record input jack of the DAT machine.
3. Connect the left and right analog outputs of the DAT machine to the analog left and right inputs of an external amplifier. Connect the outputs of the external amplifier to a pair of speakers.
4. Turn on the RV-8 using the main power switch on the rear panel.
5. Once the unit is in standby mode, press the front panel **standby button** or the remote control **POWER button** to enter normal operation.

Test:

1. To enter the MAIN MENU, press the remote control Menu ▸ arrow.
2. Scroll through the MAIN MENU using the Menu ▲/▼ arrows and highlight SETUP. Press the Menu ▸ arrow to enter SETUP.
3. In the SETUP menu, highlight INPUTS. Press the Menu ▸ arrow to enter INPUT SETUP.
4. Highlight DVD1 and Press the Menu ▸ arrow to select the DVD1 INPUT SETUP menu.
5. Scroll down through the DVD1 menu options and highlight ANALOG IN. Press the Menu ▸ arrow to enter DVD1 ANALOG IN.
6. Scroll through the DVD1 ANALOG IN input options and highlight ANALOG-1. Press the Menu ▸ arrow to assign the input to DVD1.
7. Press the Menu ◂ arrow once to return to the DVD1 INPUT SETUP menu.
8. Scroll down through the menu and highlight ZONE2 IN. Press the Menu ▸ arrow to select the ZONE2 IN parameter.
9. Press the Menu ▲/▼ arrows until ANLG is displayed.
10. Press the Menu ◂ arrow once to confirm.

    Analog should now be selected as the Zone 2 source.
11. Press the Menu ◂ arrow four times to exit the setup menus.
12. Connect the oscillator output to the left and right audio inputs labeled 1 on the rear panel of the RV-8.
13. Confirm DVD 1 is selected in the Main Zone as well as the Zone 2 section of the front panel.
14. Place the DAT machine into Record mode.
15. Slowly increase the volume on the amplifier to a comfortable listening level for the speakers.
16. Sweep the oscillator from 20Hz to 20kHz.
17. Verify that clean, undistorted audio can be heard from the Zone 2 digital outputs of the RV-8.
18. Once complete, repeat steps 1-17 to test Analog Inputs 2 through 8. Change the DVD1 ANALOG IN selected in step 6 to the next appropriate input.
19. Now perform the setup and test steps 1 to 18 to test the digital optical outputs. Be sure to use the appropriate digital cable.

Digital Input to Digital Outputs Test:

This test will verify the audio path between the S/PDIF coaxial and optical inputs 1 to 4 and the Zone 2 S/PDIF coaxial and optical digital outputs.

Setup:

1. Connect the video monitor to the main composite output of the RV-8 and turn the monitor on. This will allow full viewing of the RV-8's menus.
2. Connect a S/PDIF coaxial digital output from a DVD or CD player to the S/PDIF coaxial digital input labeled 1 on the rear panel of the RV-8.
3. Connect the S/PDIF coaxial digital output on the RV-8 rear panel to the digital record input jack of the DAT machine.
4. Connect the left and right analog outputs of the DAT machine to the analog left and right inputs of an external amplifier. Connect the outputs of the external amplifier to a pair of speakers.
5. Power on the RV-8 using the main power switch on the rear panel.
6. Once the unit is in standby mode, press the front panel **standby button** or the remote control **POWER button** to enter normal operation.

Test:

1. To enter the MAIN MENU, press the remote control Menu ▸ arrow.
2. Scroll through the MAIN MENU using the Menu ▲/▼ arrows and highlight SETUP. Press the Menu ▸ arrow to enter SETUP.
3. In the SETUP menu, highlight INPUTS. Press the Menu ▸ arrow to enter INPUT SETUP.
4. Highlight DVD1 and press the Menu ▸ arrow to select the DVD1 INPUT SETUP menu.
5. Scroll down through the DVD1 menu options and highlight DIGITAL IN. Press the Menu ▸ arrow to enter DVD1 DIGITAL IN.
6. Scroll through the DVD1 DIGITAL IN input options and highlight COAX-1. Press the Menu ▸ arrow to assign the input to DVD1.
7. Press the Menu ◂ arrow once to return to the DVD1 INPUT SETUP menu.
8. Scroll down through the menu and highlight ZONE2 IN. Press the Menu ▸ arrow to select the ZONE2 IN parameter.
9. Press the Menu ▲/▼ arrows on the remote until DIGITAL is listed.
10. Press the Menu ◂ arrow once to confirm.

    Digital should now be selected as the Zone 2 source.
11. Press the Menu ◂ arrow four times to exit the setup menus.
12. Confirm DVD 1 is selected in the Main Zone and Zone 2 section of the front panel.
13. Place the DAT machine into Record mode.
14. Power on the external amplifier.
15. Insert a disc into the DVD or CD player and press Play. Slowly increase the volume on the RV-8 to a comfortable listening level.
16. Verify that clean, undistorted audio can be heard.
17. Press Stop on the DVD or CD player and power down the external amplifier.

18. Repeat steps 1-17 to test S/PDIF coaxial Inputs 2 through 4. Change the DVD1 DIGITAL IN selected in step 6 to the next appropriate input.
19. To test the S/PDIF Optical I/O, use the S/PDIF optical output on the RV-8 to the S/PDIF optical input of the DAT player. Repeat steps 1-18 to test S/PDIF optical Inputs 1 through 4. Change the DVD1 DIGITAL IN selected in step 6 from COAX to Optical and use the appropriate digital cable.

Phono Input to Zone 2 Outputs Test

This test will verify the audio path between the left and right phono inputs and the Zone 2 Fixed and Variable outputs.

Test:

1. Connect the Low Distortion Oscillator output to the phono left and right audio inputs on the rear panel of the RV-8.
2. Connect the Zone 2 RCA left and right Fixed outputs of the RV-8 to the external amplifier left and right inputs. Connect the outputs of the external amplifier to a pair of speakers.
3. Power on the external amplifier. Slowly increase the volume on the external amplifier to a comfortable listening level.
4. Sweep the oscillator from 20Hz to 20kHz. Verify that clean, undistorted audio can be heard throughout the frequency sweep.
5. Power down the external amplifier.
6. Switch from the Zone 2 Fixed outputs to the Zone 2 Variable outputs and repeat steps 3 to 5 above.

Phono Input to Zone 3 Output Test

This test will verify the audio path between the left and right phono inputs and the RCA Zone 3 outputs.

Test:

1. Connect the Low Distortion Oscillator output to the phono left and right audio inputs on the rear panel of the RV-8.
2. Connect the RCA left and right Zone 3 outputs of the RV-8 to the external amplifier left and right inputs. Connect the outputs of the external amplifier to a pair of speakers.
3. Power on the external amplifier. Slowly increase the volume on the external amplifier to a comfortable listening level.
4. Sweep the oscillator from 20Hz to 20kHz. Verify that clean, undistorted audio can be heard throughout the frequency sweep.
5. Power down the external amplifier.

Phono Input to Digital Outputs

This test will verify the audio path between the left and right Phono inputs and the Zone 2 S/PDIF coaxial and optical digital outputs.

Setup:

1. Connect the video monitor to the main composite output of the RV-8 and turn the monitor on. This will allow full viewing of the RV-8's menus.
2. Connect the S/PDIF coaxial digital output on the RV-8 rear panel to the digital record input jack of the DAT machine.
3. Connect the left and right analog outputs of the DAT machine to the analog left and right inputs of an external amplifier. Connect the outputs of the external amplifier to a pair of speakers.
4. Turn on the RV-8 using the main power switch on the rear panel.
5. Once the unit is in standby mode, press the front panel **standby button** or the remote control **POWER button** to enter normal operation.

Test:

1. Connect the low distortion oscillator output to the left and right phono inputs on the rear panel of the RV-8.
2. Connect the S/PDIF coaxial digital output on the RV-8 rear panel to the digital record input jack of the DAT machine.
3. Connect the left and right analog outputs of the DAT machine to the analog left and right inputs of the external amplifier. Connect the outputs of the external amplifier to a pair of speakers.
4. Place the DAT machine into Record mode.
5. Power on the external amplifier. Slowly increase the volume on the external amplifier to a comfortable listening level.
6. Sweep the oscillator from 20Hz to 20kHz. Verify that clean, undistorted audio can be heard throughout the frequency sweep.
7. Power down the external amplifier.
8. Repeat steps 2 through 7 for the S/PDIF optical output. Use the appropriate digital cable.

Digital Input to Amplifier Output

This test will verify the audio path between the S/PDIF coaxial and optical inputs labeled 1 to 4 and the amplifier outputs.

Setup:

1. Connect the video monitor to the main composite output of the RV-8 and turn the monitor on. This will allow full viewing of the RV-8's menus.
2. Connect a S/PDIF coaxial digital output from a DVD or CD player to the S/PDIF coaxial digital input labeled 1 on the rear panel of the RV-8.
3. Connect the outputs of the front left and front right channels (channels 1 and 5) of the RV-8 amplifier to a pair of speakers.
4. Turn on the RV-8 using the main power switch on the rear panel.

5. Once the unit is in standby mode, press the front panel **standby button** or the remote control **POWER button** to enter normal operation.

Test:

1. To enter the MAIN MENU, press the remote control Menu ▸ arrow .
2. Scroll through the MAIN MENU using the Menu ▴/▾ arrows and highlight SETUP. Press the Menu ▸ arrow to enter SETUP.
3. In the SETUP menu, highlight INPUTS. Press the Menu ▸ arrow to enter INPUT SETUP.
4. Highlight DVD1 and press the Menu ▸ arrow button to select the DVD1 INPUT SETUP menu.
5. Scroll down through the DVD1 menu options and highlight DIGITAL IN. Press the Menu ▸ arrow to enter DVD1 DIGITAL IN.
6. Scroll through the DVD1 DIGITAL IN input options and highlight COAX-1. Press the Menu ▸ arrow to assign the input to DVD1.
7. Press the Menu ◂ arrow button five times to exit the setup menus.
8. Insert a disc into the DVD or CD player and press Play. Slowly increase the volume on the RV-8 to a comfortable listening level.
9. Verify that clean, undistorted audio can be heard.
10. Once complete, repeat steps 1 to 9 to test the remaining digital inputs 2 to 4. Change the DVD1 DIGITAL IN selected in step 6 to the next appropriate input.
11. Now test the optical inputs using steps 1 to 10. Be sure to use the appropriate digital cable.

AUDIO I/O TESTS

In order to properly test the RV-8 as described in this procedure, the RV-8 must be in Diagnostics mode. Perform the following procedure to enter the Diagnostics mode.

To enter Diagnostics mode:

1. Connect the video monitor to the main composite output of the RV-8 and turn the monitor on. This will allow full viewing of the RV-8's Diagnostics menus.
2. Turn on the RV-8 using the rear panel main power switch.
3. When "** LEXICON **" appears on the display, press and hold the **Zone2 DVD2** and **Zone3 DVD2** buttons on the front panel within twenty seconds.
4. Continue to hold down the buttons until the RV-8 display reads "DIAGS MENU FUNCTIONAL TESTS."

Analog Inputs To Main Zone Outputs Test

This test will verify the audio path between the paired analog inputs 1 to 8 and all Main outputs.

Test:

1. Connect the low distortion oscillator output to the left and right analog audio inputs labeled 1 on the rear panel of the RV-8.
2. Connect the RCA front left and front right outputs of the RV-8 to the external amplifier left and right inputs. Connect the outputs of the external amplifier to the pair of speakers.

3. Using the Menu ▼ arrow, scroll down through the Diagnostics Menu and select AUDIO I/O TESTS.
4. In the AUDIO I/O TEST menu, highlight AUDIO INPUT 1 TEST. Press the Menu ▶ arrow to engage the test. The RV-8 is now set to route audio from the left and right analog inputs labeled 1 to all Main Zone outputs.
5. Power on the external amplifier. Slowly increase the volume on the external amplifier to a comfortable listening level.
6. Sweep the oscillator from 20Hz to 20kHz. Verify that clean, undistorted audio can be heard throughout the frequency sweep.
7. Power down the external amplifier.
8. Once complete, repeat steps 5 through 7 to test the remaining paired RCA outputs (Center/Sub, Side L/R, and Rear L/R). Repeat steps 5 through 7 to test Analog Inputs 2 through 8. Change the INPUT TEST selected in step 4 to the next appropriate input. Switch the Oscillator outputs to the RV-8 input that corresponds to the input selected in the AUDIO I/O TEST menu.

Analog Inputs to Amplifier Outputs Test

This test will verify the audio path between the paired analog inputs labeled 1 to 8 and all analog amp output channels.

Test:

1. Connect the low distortion oscillator output to the left and right analog audio inputs labeled 1 on the rear panel of the RV-8.
2. With the RV-8 powered off, connect the RV-8 amplifier front left and front right outputs to the pair of speakers.
3. Power on the RV-8.
4. Using the Menu ▲/▼ arrows, scroll through the Diagnostics Menu and select the AUDIO I/O TESTS.
5. In the AUDIO I/O TESTS menu, highlight the AMP TEST. Press the remote control Menu ▶ arrow to engage the test. The RV-8 is now set to route audio from the left and right analog inputs labeled 1 to all amplifier outputs.
6. Using the **volume knob** on the front panel of the RV-8, slowly increase the volume to a comfortable listening level.
7. Sweep the oscillator from 20Hz to 20kHz. Verify that clean, undistorted audio can be heard throughout the frequency sweep.
8. Lower the volume of the RV-8.
9. Power off the RV-8 and carefully disconnect the front left and front right speaker wires from the RV-8 amplifier outputs and connect them to the side left and side right amplifier outputs.
10. Power on the RV-8 and repeat steps 5 to 7.
11. Repeat steps 5 to 9 to test the RV-8 amplifier outputs for the rear left, rear right, and center channel outputs.

Phono Input To Main Zone Outputs Test

This test will verify the audio path between the Phono inputs labeled left and right, to all Main Zone Outputs.

Test:

1. Connect the low distortion oscillator output to the Phono left and right inputs on the rear panel of the RV-8.
2. Connect the RCA front left and front right outputs of the RV-8 to the external amplifier left and right inputs. Connect the outputs of the external amplifier to the pair of speakers.
3. Using the Menu ▲/▼ arrows, scroll through the Diagnostics Menu and select the AUDIO I/O TESTS.
4. In the AUDIO I/O TESTS menu, highlight AUDIO PHONO TEST. Press the remote control Menu ▶ arrow to engage the test. The RV-8 is now set to route audio from the Phono left and right inputs to all Main Zone outputs.
5. Power on the external amplifier. Slowly increase the volume on the external amplifier to a comfortable listening level.
6. Sweep the oscillator from 20Hz to 20kHz. Verify that clean, undistorted audio can be heard throughout the frequency sweep.
7. Power down the external amplifier.
8. Repeat steps 5 through 7 for the remaining paired RCA outputs (center/sub, side L/R, and rear L/R).

Digital Inputs to Main Zone Outputs Test

This test will verify the audio path between the S/PDIF coaxial and optical digital audio inputs labeled 1 to 4, and all Main Zone analog outputs.

***Note**:*
This test requires the use of a CD player as a source. The tests to follow will be run using a PCM signal at a 44.1kHz sample rate.

Test:

1. Connect the S/PDIF coaxial digital output of the CD player to the S/PDIF coaxial digital input 1 on the RV-8 rear panel. Connect the S/PDIF optical digital output of the CD player to the S/PDIF optical digital input 1 on the RV-8 rear panel.
2. Connect the RCA front left and front right outputs of the RV-8 to the external amplifier left and right inputs. Connect the outputs of the external amplifier to a pair of speakers.
3. Using the Menu ▲/▼ arrows, scroll through the Diagnostic Menu and select the AUDIO I/O TESTS.
4. In the AUDIO I/O TEST Menu, highlight S/PDIF INPUT CX1 TEST. Press the Menu ▶ arrow to engage the test. The RV-8 is now set to route digital audio from the S/PDIF coaxial digital input labeled 1 to all the RCA analog outputs.
5. Power on the external amplifier. Press Play on the CD player.
6. Slowly increase the volume on the external amplifier to a comfortable listening level.
7. Verify that clean, undistorted audio can be heard.
8. Stop the CD player and power down the external amplifier.
9. Repeat steps 2 through 8 for the remaining paired RCA outputs (Center/Sub, Side L/R, Rear L/R).

10. The above procedure should be repeated to test digital S/PDIF COAX inputs labeled 2 through 4, as well as the optical inputs labeled 1 to 4. Change the INPUT TEST selected in step 4 of setup procedure to the next appropriate input. Move the output of the DVD player to the appropriate RV-8 input. When testing the optical inputs, be sure to use the appropriate digital cable.

Digital Inputs To Zone 2 Outputs Test

This test will verify the audio path between the RV-8 S/PDIF coaxial and optical digital inputs and the Zone 2 RCA Fixed and Variable outputs.

***Note**:*
This test requires the use of a CD player as a source. The tests to follow will be run using a PCM signal at a 44.1kHz sample rate.

Test:

1. Connect the S/PDIF coaxial digital output of the CD player to the S/PDIF coaxial digital input 1 on the RV-8 rear panel.
2. Connect the Zone 2 RCA left and right Fixed outputs of the RV-8 to the external amplifier left and right inputs.
3. Using the Menu ▲/▼ arrows scroll through the Diagnostics Menu and select the AUDIO I/O TESTS.
4. In the AUDIO I/O TEST menu, highlight S/PDIF INPUT CX 1 TEST. Press the remote control Menu ▶ arrow to engage the test. The RV-8 is now set to route digital audio from the S/PDIF coaxial digital input labeled 1 to all the RCA analog outputs.
5. Power on the external amplifier. Press play on the CD player.
6. Slowly increase the volume on the external amplifier to a comfortable listening level.
7. Verify that clean, undistorted audio can be heard.
8. Stop the CD player and power down the external amplifier.
9. Switch the RCA cables from the Zone 2 RCA Fixed output to the Zone 2 RCA Variable outputs and repeat steps 5 through 8.
10. The above procedure should be repeated to test S/PDIF coaxial digital inputs 2 through 4 as well as the optical inputs 1 to 4. To do this, repeat the procedure, changing the Input Test selected in step 4 to the next appropriate input. Move the output of the CD player to the appropriate RV-8 input that corresponds to the input selected in the AUDIO I/O TEST menu. When testing the optical inputs, be sure to use the appropriate digital cable.

Digital Inputs To Zone 3 Outputs Test

This test will verify the audio path between the RV-8 S/PDIF coaxial digital input 1 to the Zone 3 RCA analog outputs.

***Note**:*
This test requires the use of a CD player as a source. The tests to follow will be run using a PCM signal at a 44.1kHz sample rate.

Test:

1. Connect the S/PDIF coaxial digital output of the CD player to the S/PDIF coaxial digital input 1 on the RV-8 rear panel. Connect the S/PDIF optical digital output of the CD player to the S/PDIF optical digital input 1 on the RV-8 rear panel.
2. Connect the Zone 3 RCA left and right Fixed outputs of the RV-8 to the external amplifier left and right inputs. Connect the outputs of the external amplifier to a pair of speakers.
3. Using the Menu ▲/▼ arrows scroll through the Diagnostics Menu and select the AUDIO I/O TESTS.
4. In the AUDIO I/O TEST menu, highlight S/PDIF INPUT CX 1 TEST. Press the remote control Menu ▶ arrow to engage the test. The RV-8 is now set to route digital audio from the S/PDIF COAX digital input labeled 1 to all the RCA analog outputs.
5. Power on the external amplifier. Press Play on the CD player.
6. Slowly increase the volume on the external amplifier to a comfortable listening level.
7. Verify that clean, undistorted audio can be heard.
8. Stop the CD player and power down the external amplifier.
9. The above procedure should be repeated to test S/PDIF coaxial digital inputs 2 through 4 as well as the optical inputs 1 to 4. To do this, repeat the procedure, changing the Input Test selected in step 4 to the next appropriate input. Move the output of the CD player to the appropriate RV-8 input that corresponds to the input selected in the AUDIO I/O TEST menu. When testing the optical inputs, be sure to use the appropriate digital cable.

AUDIO PERFORMANCE VERIFICATION

Performing these tests assures that the audio signal paths in the RV-8 meet published specifications. These tests will verify the performance specifications of the gain, frequency response, THD+N, and S/N ratio of each channel.

Analog Audio Inputs To Main Zone RCA Outputs Test

This test will verify the specifications of the Main Zone RCA outputs.

Setup:

1. Connect an audio cable between the output of the Low Distortion Oscillator and the RV-8 left RCA input 1.
2. Connect an audio cable between the front left RCA output of the RV-8 and the input of the Distortion Analyzer.
3. Using the Menu ▲/▼ arrows scroll through the Diagnostic Menu and select the AUDIO I/O TESTS.
4. In the AUDIO I/O TEST menu, highlight AUDIO INPUT 1 TEST. Press the remote control Menu ▶ arrow to engage the test. The RV-8 is now set to route audio from the left and right RCA inputs labeled 1 to all RCA analog outputs.

Gain Test (GAIN):

1. Apply a 997Hz signal @ +4Vrms to the RV-8 left RCA analog input 1.
2. Set the scale on the Distortion Analyzer to measure +8Vrms signal level.
3. Turn all the filters off on the Analyzer (Filter not required for this test).
4. Verify that the output level measurement from the RV-8 is between the range of +3.10Vrms and +3.70Vrms. Note this level.

Total Harmonic Distortion Test (THD):

1. Adjust the scale on the Distortion Analyzer to measure 0.01% THD+N and turn off the low-pass or audio band pass filter.
2. Verify that the THD+N measured on the Analyzer is less than 0.09%.

Frequency Response Test (FREQ):

1. Set the scale on the Distortion Analyzer to measure a +4Vrms signal level.
2. Using the output level from step 4 of the Gain Test, set the Distortion Analyzer for a 0dB reference to check frequency response of the RV-8.
3. Turn the filter on the Analyzer off.
4. Sweep the oscillator frequency from 10Hz to 40kHz.
5. Verify the signal levels are +0.10dBr to –0.8dBr (10Hz-20Hz), +0.10dBr to –0.25dBr (20Hz-20kHz), and +0.10dBr to –0.8dBr (20kHz-40kHz) of reference level over the entire sweep. Note these levels.

Signal to Noise Test (SNR):

1. Using the signal level from step 5 of the Frequency Response Test above, turn off the oscillator and verify a noise level measurement <-102dBr.
2. This procedure should be repeated to test Analog Inputs 2 through 8. To do this, move the cable from the output of the Low Distortion Oscillator to the next pair of inputs, and repeat the tests above to test the remaining Main Zone RCA outputs.

Analog Audio Inputs to Amplifier Outputs Tests

This test will verify the specifications of the Analog RCA inputs to the amplifier outputs.

Setup:

1. Connect an audio cable between the output of the Low Distortion Oscillator and the RV-8 Left RCA input 1.
2. Connect an audio cable between the front left amplifier output of the RV-8 and the input of the Distortion Analyzer.
3. Using the Menu ▲/▼ arrows, scroll through the Diagnostic Menu and select the AUDIO I/O TESTS.
4. In the AUDIO I/O TEST menu, highlight AUDIO INPUT 1 TEST. Press the Menu ▶ arrow on the RV-8 remote control to engage the test. The RV-8 is now set to route audio from the left and right RCA inputs labeled 1 to all amplifier outputs.

Gain Test (GAIN):

1. Apply a 1kHz signal @ +1Vrms to the RV-8 Left RCA analog input 1.
2. Set the scale on the Distortion Analyzer to measure +8Vrms signal level.
3. Turn all the filters off on the Analyzer (Filter not required for Gain Test).
4. Verify that the output level measurement from the RV-8 is between the range of +7.55Vrms and +8.35Vrms. Note this level.

Total Harmonic Distortion Test (THD):

1. Adjust the scale on the Distortion Analyzer to measure 0.01% THD+N and turn off the low pass or audio band pass filter.
2. Verify that the THD+N measured on the Analyzer is less than 0.05%.

Frequency Response Test (FREQ):

1. Set the scale on the Distortion Analyzer to measure +1Vrms signal level.
2. Using the output level from step 4 of the Gain Test, set the Distortion Analyzer for a 0dB reference to check frequency response of the RV-8.
3. Turn the filter on the Analyzer off.
4. Sweep the oscillator frequency from 10Hz to 100kHz.
5. Verify the signal levels are +0.10dBr to –0.5dBr (10/20Hz-20kHz), +0.10dBr to –0.2dBr (20Hz-20kHz), +0.10dBr to –0.5dBr (40kHz), and +0.10dBr to –3.0dBr (100kHz) of reference level over the entire sweep. Note these levels.

Signal to Noise Test (SNR):

1. Using the signal levels from step 5 of the Frequency Response Test, turn off the oscillator and verify a noise level measurement <-105dBr.
2. This procedure should be repeated to test analog inputs labeled 2 through 8. To do this, move the cable from the output of the Low Distortion Oscillator to the next pair of inputs, and repeat the tests above to test the remaining Main Zone RCA outputs. Repeat the above tests for the remaining Main Zone amplifier outputs.

Digital Optical Input to Analog Output Test

This test will verify the specifications of the digital input and analog output circuitry.

Setup:

1. Connect a digital audio cable from the output of the Digital Function Generator to the S/PDIF optical input 1 on the RV-8 rear panel.
2. Connect analog audio cable between the front left RCA output of the RV-8 and the input of the Distortion Analyzer.
3. Using the Menu ▲/▼ arrows, scroll through the Diagnostic Menu and select the AUDIO I/O TESTS.
4. In the AUDIO I/O TEST menu, highlight S/PDIF INPUT OP1 TEST. Press the Menu ▶ arrow to engage the test. The RV-8 is now set to route audio from the left and right RCA inputs labeled 1 to all RCA analog outputs.

Gain Test (GAIN):

1. Apply a 997Hz signal @ + 0dBFS to the S/PDIF coaxial 1 input of the RV-8.
2. Set the scale on the Distortion Analyzer to measure +8Vrms signal level.
3. Turn all the filters off on the Analyzer (Filter not required for Gain Test).
4. Verify that the output level measurement from the RV-8 is between the range of +3.28Vrms and +3.63Vrms. Note this level.

Total Harmonic Distortion Test (THD):

1. Adjust the scale on the Distortion Analyzer to measure 0.01% THD+N and turn off the low pass or audio band pass filter.
2. Verify that the THD+N measured on the Analyzer is less than 0.05%.

Frequency Response Test (FREQ):

1. Set the scale on the Distortion Analyzer to measure +1Vrms signal level.
2. Using the output level from step 4 of the Gain Test, set the Distortion Analyzer for a 0dB reference to check frequency response of the RV-8.
3. Turn the filter on the Analyzer off.
4. Sweep the oscillator frequency from 10Hz to 100kHz.
5. Verify the signal levels are +0.10dBr to –0.5dBr (10/20Hz-20kHz), +0.10dBr to –0.2dBr (20Hz-20kHz), +0.10dBr to –0.5dBr (40kHz), and +0.10dBr to –3.0dBr (100kHz) of reference level over the entire sweep.

Signal to Noise Test (SNR):

1. Using the signal levels from step 5 of the Frequency Response Test, turn off the oscillator and verify a noise level measurement <-105dBr.
2. This procedure should be repeated to test Analog Inputs labeled 2 through 8. To do this, move the cable from the output of the Low Distortion Oscillator to the next pair of inputs, and repeat the tests above to test the remaining Main Zone RCA outputs. Repeat the above tests for the remaining Main Zone amplifier outputs.

VIDEO INPUT/OUTPUT TESTS

These tests will verify that all thirteen video inputs and ten video outputs pass video. There are three different video paths to be tested in the RV-8: composite, S-video, and component. Composite paths have five inputs and five outputs. S-video paths have five inputs and four outputs. Component paths have three inputs and one output. The following tests will verify that the RV-8 is passing clear, undistorted video. It is not necessary to enter the Extended Diagnostics as was done in the Audio tests.

Composite Video Input to Composite Video Outputs Test

This test will verify the composite video switching function of the RV-8.

Setup:

1. Connect the composite video output from the DVD player to the RV-8's composite video input 1.
2. Connect the first main composite output of the RV-8 to the composite input of the video monitor.
3. Turn on the DVD player, monitor, and the RV-8.
4. The monitor should display a blue screen.
5. Press the remote control **MAIN** button, then press the **DVD1** button to select DVD1 as the input for testing the video paths.
6. Press the Menu ▸ arrow to display the Main Menu.
7. Using the Menu ▾ arrow button, scroll down to SETUP. Press the Menu ▸ arrow to select the SETUP menu.
8. The SETUP Menu will appear with INPUTS highlighted.
9. Press the Menu ▸ arrow again to open the INPUT SETUP menu.
10. DVD1 will be highlighted.
11. Press the Menu ▸ arrow. The DVD1 INPUT SETUP menu will now be displayed.
12. Using the Menu ▾ arrow, scroll to the VIDEO IN parameter. Select it by pressing the Menu ▸ arrow.
13. The DVD1 VIDEO IN menu will open and COMPOSITE-1 will be highlighted.
14. Press the Menu ▸ arrow to select COMPOSITE-1. This will assign the composite -1 video input to the main composite output of the RV-8.
15. Press the Menu ◂ arrow three times to exit to the SETUP menu.
16. Using the Menu ▾ down arrow, scroll down to the DISPLAYS parameter and select it by pressing the Menu ▸ arrow.
17. The DISPLAY SETUP menu will open with the ON-SCREEN DISPLAY parameter highlighted. Select it by pressing the Menu ▸ arrow. The ON-SCREEN DISPLAY menu will open with the STATUS parameter highlighted.

18. Select the STATUS parameter by pressing the Menu ▸ arrow and change the value of the parameter to “ALWAYS OFF.”
19. Press the Menu ◂ arrow to exit the menu structure.
20. The video path is now set for testing.

Test:

1. Load a disc into the DVD player and press play.
2. Verify a clean undistorted picture appears on the monitor.
3. Pause the DVD player.
4. To test the four remaining composite outputs (the other Main Zone output, the Zone 2 outputs and the Zone 3 output), switch the composite output cable on the back of the RV-8 to the next main composite video output connector and press Play on the DVD player.
5. Repeat the above procedure for the two Zone 2 composite video outputs.
6. To test the remaining composite inputs (2 through 5), reconnect the composite output cable to the first main composite output.
7. In steps 13 and 14 of the above Setup procedure, change the VIDEO IN parameter from COMPOSITE-1 to COMPOSITE-2. Repeat steps 1 to 3 of this test procedure.
8. Repeat step 7 above to test the remaining RV-8 composite inputs (3 through 5).

S-video Inputs to S-video Outputs Test

This test will verify the S-video switching function of the RV-8.

Setup:

1. Connect the S-video output from the DVD player to the RV-8 S-video input 1.
2. Connect the first main S-video output of the RV-8 to the S-video input of the video monitor.
3. Turn on the DVD player, monitor, and the RV-8.
4. The monitor should display a blue screen.
5. On the RV-8 remote control, press the **MAIN** button, then press the **DVD1** button to select DVD1 as the input for testing the video paths.
6. Press the remote Menu ▸ arrow to display the Main Menu.
7. Using the Menu ▾ arrow, scroll down to SETUP. Press the Menu ▸ arrow to select the SETUP menu.
8. The SETUP menu will appear with INPUTS highlighted.
9. Press the Menu ▸ right arrow again to open the INPUT SETUP menu.
10. DVD1 will be highlighted.
11. Press the Menu ▸ arrow. The DVD1 INPUT SETUP menu will now be displayed.
12. Using the Menu ▾ arrow, scroll to the VIDEO IN parameter. Select it by pressing the Menu ▸ arrow.
13. Using the Menu ▾ arrow, scroll to S-VIDEO-1.

14. Press the Menu ▸ arrow to select S-VIDEO-1. This will assign the S-video-1 video input to the Main S-video output of the RV-8.
15. Press the Menu ◂ arrow three times to exit to the SETUP menu.
16. Using the Menu ▾ arrow, scroll down to the DISPLAYS parameter and select it by pressing the Menu ▸ arrow.
17. The DISPLAY SETUP menu will open with the ON-SCREEN DISPLAY parameter highlighted. Select it by pressing the Menu ▸ arrow. The ON-SCREEN DISPLAY menu will open with the STATUS parameter highlighted.
18. Select the STATUS parameter by pressing the Menu ▸ arrow and change the value of the parameter to “ALWAYS OFF.” Press the Menu ◂ arrow to exit the menu structure.
19. The video path is now set for testing.

Test:

1. Load a disc into the DVD player and press play.
2. Verify a clean undistorted picture appears on the monitor.
3. Pause the DVD player.
4. To test the three remaining S-video outputs (other Main Zone output and the Zone 2 outputs), switch the S-video monitor output cable on the back of the RV-8 to the next main S-video output connector and press play on the DVD player.
5. Repeat the above procedure for the two Zone 2 S-video outputs.
6. To test the remaining S-video inputs (2 through 5), reconnect the S-video output cable to the first main S-video output.
7. In steps 13 and 14 of the above Setup procedure, change the VIDEO IN parameter from S-VIDEO-1 to S-VIDEO-2. Repeat steps 1 to 3 of this test procedure.
8. Repeat Step 7 above to test the remaining RV-8 S-video inputs (3 through 5).

Component Video Input to Component Video Output Test

This test will verify the component video switching function of the RV-8.

Setup*:*

1. Connect the component video output from the DVD player to the RV-8 component video input 1.
2. Connect the RV-8 main component video output to the component video input of the video monitor.
3. Turn on the DVD player, monitor, and the RV-8.
4. The monitor should display a blue screen.
5. On the RV-8 remote control, press the **MAIN** button, then press the **DVD1** button to select DVD1 as the input for testing the video paths.
6. Press the Menu ▸ arrow on the RV-8 remote control to display the Main Menu.
7. Using the Menu ▾ arrow on the remote, scroll down to SETUP. Press the Menu ▸ arrow to select the SETUP menu.
8. The SETUP Menu will appear with INPUTS highlighted.
9. Press the Menu ▸ arrow again to open the INPUT SETUP menu.

10. DVD1 will be highlighted.
11. Press the Menu ▸ arrow. The DVD1 INPUT SETUP menu will now be displayed.
12. Using the Menu ▾ arrow, scroll to the COMPONENT IN parameter. Select it by pressing the Menu ▸ arrow.
13. The DVD1 COMPONENT IN menu will be displayed with the COMPONENT-1 parameter highlighted.
14. Press the Menu ▸ arrow to select this video input. This will assign the RV-8 component 1 video input to the main component video output.
15. Press Menu ◂ arrow three times to exit to the SETUP menu.
16. Using the Menu ▾ arrow, scroll down to the DISPLAYS parameter and select it by pressing the Menu ▸ right arrow.
17. The DISPLAY SETUP menu will open with the ON-SCREEN DISPLAY parameter highlighted. Select it by pressing the Menu ▸ arrow.
18. The ON-SCREEN DISPLAY menu will open with the STATUS parameter highlighted. Select the STATUS parameter by pressing the Menu ▸ arrow and change the value of the parameter to "ALWAYS OFF". Press the Menu ◂ arrow to exit the menu structure.
19. The video path is now set for testing.

Test:

1. Load a disc into the DVD player and press play.
2. Verify a clean undistorted picture appears on the monitor.
3. Pause the DVD player.
4. In steps 13 and 14 of the above Setup procedure, change the COMPONENT IN parameter from COMPONENT-1 to COMPONENT-2. Repeat steps 1 to 3 of this test procedure.
5. Repeat step 4 above to test the remaining RV-8 component inputs.

Composite Video Input to Component Video Output Test

This test will verify the Video Up-Conversion functionality of the RV-8.

Setup:

1. Connect the composite video output from the DVD player to the RV-8's composite video input 1.
2. Connect the RV-8 main component video output to the component video input of the video monitor.
3. Turn on the DVD player, monitor, and the RV-8.
4. The monitor should display a blue screen.
5. On the RV-8 remote control, press the **MAIN** button, then press the **DVD1** button to select DVD1 as the input for testing the video paths.
6. Press the remote control Menu ▸ arrow to display the Main Menu.
7. Using the Menu ▾ arrow, scroll down to SETUP. Press the Menu ▸ right arrow to select the SETUP menu.
8. The SETUP menu will appear with INPUTS highlighted.
9. Press the Menu ▸ arrow again to open the INPUT SETUP menu.
10. DVD1 will be highlighted.

11. Press the Menu ▸ arrow. The DVD1 INPUT SETUP menu will now be displayed.
12. Using the Menu ▾ arrow, scroll to the VIDEO IN parameter and select it by pressing the Menu ▸ arrow.
13. The DVD1 VIDEO IN menu will be displayed. Using the Menu ▾ arrow, scroll to the COMPOSITE-1 parameter and select it by pressing the Menu ▸ arrow. Press the Menu ◂ arrow to exit the DVD1 VIDEO IN menu.
14. Using the Menu ▾ arrow, scroll to the COMPONENT IN parameter. Select it by pressing the Menu ▸ arrow.
15. The DVD1 COMPONENT IN menu will be displayed.
16. Using the Menu ▾ arrow, highlight the VIDEO parameter and press the Menu ▸ arrow to select it. This will set the RV-8 to up-convert composite and S-video inputs to component video.
17. Press the Menu ◂ arrow three times to exit to the SETUP menu.
18. Using the Menu ▾ arrow, scroll down to the DISPLAYS parameter and select it by pressing the Menu ▸ arrow.
19. The DISPLAY SETUP menu will open with the ON-SCREEN DISPLAY parameter highlighted. Select it by pressing the Menu ▸ arrow.
20. The ON-SCREEN DISPLAY menu will open with the STATUS parameter highlighted. Select the STATUS parameter by pressing the Menu ▸ arrow and change the value of the parameter to "ALWAYS OFF."
21. Press the Menu ◂ arrow to exit the menu structure.
22. The video path is now set for testing.

Test:

1. Load a disc into the DVD player and press Play.
2. Verify a clean undistorted picture appears on the monitor.

S-video Input to Component Video Output Test

This test will verify the Video Up-Conversion functionality of the RV-8.

Setup:

1. Connect the S-video output from the DVD player to the RV-8's S-video input 1.
2. Connect the RV-8 main component video output to the component video input of the video monitor.
3. Turn on the DVD player, monitor, and the RV-8.
4. The monitor should display a blue screen.
5. On the RV-8 remote control, press the **MAIN** button, then press the **DVD1** button to select DVD1 as the input for testing the video paths.
6. Press the remote control Menu ▸ arrow to display the Main Menu.
7. Using the Menu ▾ arrow, scroll down to SETUP. Press the Menu ▸ arrow to select the SETUP menu.
8. The SETUP Menu will appear with INPUTS highlighted.
9. Press the Menu ▸ arrow again to open the INPUT SETUP menu.

10. DVD1 will be highlighted.
11. Press the Menu ▸ arrow. The DVD1 INPUT SETUP menu will now be displayed.
12. Using the Menu ▾ arrow, scroll to the VIDEO IN parameter and select it by pressing the menu ▸ arrow.
13. The DVD1 VIDEO IN menu will be displayed. Using the Menu ▾ arrow, scroll to the S-VIDEO-1 parameter and select it by pressing the Menu ▸ arrow.
14. Press the Menu ◂ arrow to exit the DVD1 VIDEO IN menu.
15. Using the Menu ▾ arrow, scroll to the COMPONENT IN parameter. Select it by pressing the Menu ▸ arrow.
16. The DVD1 COMPONENT IN menu will be displayed.
17. Using the Menu ▾ arrow, highlight the VIDEO parameter and press the Menu ▸ arrow to select it. This will set the RV-8 to up-convert composite and S-video inputs to component video.
18. Press the Menu ◂ arrow three times to exit to the SETUP menu.
19. Using the Menu ▾ arrow, scroll down to the DISPLAYS parameter and select it by pressing the Menu ▸ arrow.
20. The DISPLAY SETUP menu will open with the ON-SCREEN DISPLAY parameter highlighted. Select it by pressing the Menu ▸ arrow.
21. The ON-SCREEN DISPLAY menu will open with the STATUS parameter highlighted. Select the STATUS parameter by pressing the Menu ▸ arrow and change the value of the parameter to “ALWAYS OFF.”
22. Press the Menu ◂ arrow to exit the menu structure.
23. The video path is now set for testing.

Test:

1. Load a disc into the DVD player and press play.
2. Verify a clean undistorted picture appears on the monitor.

Making The Bias Voltage Adjustment

WARNING

Dangerous voltages capable of causing death are present in this unit. Use extreme caution when handling, testing, or adjusting.

The bias voltage adjustment should only be performed while the amplifier module is at room temperature (25°C). The amplifier module must have power applied for at least one minute before the bias adjustment is performed.

If the amplifier is hot from prior testing, it should be set aside until it has cooled before continuing. Use caution and follow checkout procedures carefully to ensure correct results.

***Note**:*
It is recommended to use test clips when measuring voltages across pins.

***Note**:*
During this procedure all tests are performed with NO INPUT SIGNAL applied to the amplifier inputs and with NO RESISTIVE LOAD connected to the amplifier outputs.

Bias Adjustment On The 4 Channel Module:

Channel # 1

1. Measure the DC voltage across pins 1 & 2 of P11.
2. Adjust R84 until the voltage measured is 350mV, +/-12mV (338mV–362mV).

Channel # 2

1. Measure the DC voltage across pins 5 & 6 of P11.
2. Adjust R168 until the voltage measured is 350mV, +/-12mV (338mV–362mV).

Channel # 3

1. Measure the DC voltage across pins 1 & 2 of P12.
2. Adjust R252 until the voltage measured is 350mV, +/-12mV (338mV–362mV).

Channel # 4

1. Measure the DC voltage across pins 5 & 6 of P11.
2. Adjust R336 until the voltage measured is 350mV, +/-12mV (338mV–362mV).

Bias Adjustment On The 3 Channel Module:

***Note**:*
The reference designators on the 3 Channel Module are identical to the 4 Channel Module, except Channel #1 is eliminated.

Channel # 2

1. Measure the DC voltage across pins 5 & 6 of P11.
2. Adjust R168 until the voltage measured is 350mV, +/-12mV (338mV–362mV).

Channel # 3

1. Measure the DC voltage across pins 1 & 2 of P12.
2. Adjust R252 until the voltage measured is 350mV, +/-12mV (338mV–362mV).

Channel # 4

1. Measure the DC voltage across pins 5 & 6 of P11.
2. Adjust R336 until the voltage measured is 350mV, +/-12mV (338mV–362mV).

LEXICON AUDIO PRECISION ATE SUMMARY

This chart represents a summary of Audio Precision test settings and parameters used by Lexicon in production testing of all RV-8 products. The ATE chart and ATE summary are provided as a reference and supplement of bench test settings found in the rest of the Performance Verification chapter. The Audio ATE Test Chart is located on the next page.

A-D Tests		Analog Generator							Digital Analyzer								Switcher Module						
Test Name	See Note:	Left	Right	Freq (Hz)	EQ Curve	Z-out	Bal/ Unbal	Gnd/ Float	Level	Measure	Typical Reading	Upper Limit	Lower Limit	Imp.	Bandwidth	Filter	A In	B In	A Out	B Out	Clock Source	Sample Rate	Audio Source
ANLG_ZONE2_IN1_TO_DIG_ZONE2_COAX_OUT_96K																							
ANLG_ZONE2_IN1_TO_DIG_ZONE2_COAX_OUT_96K_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	dBFS	Level	-0.40	+0.00	-1.10	n/a	<10 - Fs/2	None	n/a	n/a	1	13	Internal	96000	Analog
ANLG_ZONE2_IN1_TO_DIG_ZONE2_COAX_OUT_96K_FREQ	1	2.00 Vrms	2.00 Vrms	10-20/20-40k	None	20	Unbal	Float	dBr	Level	-0.20/-0.00	+0.10	-0.50/-0.25	n/a	<10 - Fs/2	None	n/a	n/a	1	13	Internal	96000	Analog
ANLG_ZONE2_IN1_TO_DIG_ZONE2_COAX_OUT_96K_THD	1	3.80 Vrms	3.80 Vrms	20-1k/5k-40k	None	20	Unbal	Float	dBFS	THD+N	<-98.00/-86.00	-88.00/-75.00	-120.00	n/a	<10 - Fs/2	None	n/a	n/a	1	13	Internal	96000	Analog
ANLG_ZONE2_IN1_TO_DIG_ZONE2_COAX_OUT_96K_XTALK	1	4.00 Vrms	4.00 Vrms	15k	None	20	Unbal	Float	dB	Level	-86.00	-80.00	-130.00	n/a	<10 - Fs/2	None	n/a	n/a	1	13	Internal	96000	Analog
ANLG_ZONE2_IN1_TO_DIG_ZONE2_COAX_OUT_96K_DYNRNG	1	4.00 mVrms	4.00 mVrms	997	None	20	Unbal	Float	dBFS	THD+N	-107.00	-104.00	-130.00	n/a	<10Hz->20kHz LP	Narrow	n/a	n/a	1	13	Internal	96000	Analog
ANLG_ZONE2_IN2_TO_DIG_ZONE2_COAX_OUT_96K																							
ANLG_ZONE2_IN2_TO_DIG_ZONE2_COAX_OUT_96K_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	dBFS	Level	-0.40	+0.00	-1.10	n/a	<10 - Fs/2	None	n/a	n/a	2	14	Internal	96000	Analog
ANLG_ZONE2_IN2_TO_DIG_ZONE2_COAX_OUT_96K_FREQ	1	2.00 Vrms	2.00 Vrms	10-20/20-40k	None	20	Unbal	Float	dBr	Level	-0.20/-0.00	+0.10	-0.50/-0.25	n/a	<10 - Fs/2	None	n/a	n/a	2	14	Internal	96000	Analog
ANLG_ZONE2_IN2_TO_DIG_ZONE2_COAX_OUT_96K_THD	1	3.80 Vrms	3.80 Vrms	20-1k/5k-40k	None	20	Unbal	Float	dBFS	THD+N	<-98.00/-86.00	-88.00/-75.00	-120.00	n/a	<10 - Fs/2	None	n/a	n/a	2	14	Internal	96000	Analog
ANLG_ZONE2_IN2_TO_DIG_ZONE2_COAX_OUT_96K_XTALK	1	4.00 Vrms	4.00 Vrms	15k	None	20	Unbal	Float	dB	Level	-86.00	-80.00	-130.00	n/a	<10 - Fs/2	None	n/a	n/a	2	14	Internal	96000	Analog
ANLG_ZONE2_IN2_TO_DIG_ZONE2_COAX_OUT_96K_DYNRNG	1	4.00 mVrms	4.00 mVrms	997	None	20	Unbal	Float	dBFS	THD+N	-107.00	-104.00	-130.00	n/a	<10Hz->20kHz LP	Narrow	n/a	n/a	2	14	Internal	96000	Analog
ANLG_ZONE2_IN3_TO_DIG_ZONE2_COAX_OUT_96K																							
ANLG_ZONE2_IN3_TO_DIG_ZONE2_COAX_OUT_96K_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	dBFS	Level	-0.40	+0.00	-1.10	n/a	<10 - Fs/2	None	n/a	n/a	3	15	Internal	96000	Analog
ANLG_ZONE2_IN3_TO_DIG_ZONE2_COAX_OUT_96K_FREQ	1	2.00 Vrms	2.00 Vrms	10-20/20-40k	None	20	Unbal	Float	dBr	Level	-0.20/-0.00	+0.10	-0.50/-0.25	n/a	<10 - Fs/2	None	n/a	n/a	3	15	Internal	96000	Analog
ANLG_ZONE2_IN3_TO_DIG_ZONE2_COAX_OUT_96K_THD	1	3.80 Vrms	3.80 Vrms	20-1k/5k-40k	None	20	Unbal	Float	dBFS	THD+N	<-98.00/-86.00	-88.00/-75.00	-120.00	n/a	<10 - Fs/2	None	n/a	n/a	3	15	Internal	96000	Analog
ANLG_ZONE2_IN3_TO_DIG_ZONE2_COAX_OUT_96K_XTALK	1	4.00 Vrms	4.00 Vrms	15k	None	20	Unbal	Float	dB	Level	-86.00	-80.00	-130.00	n/a	<10 - Fs/2	None	n/a	n/a	3	15	Internal	96000	Analog
ANLG_ZONE2_IN3_TO_DIG_ZONE2_COAX_OUT_96K_DYNRNG	1	4.00 mVrms	4.00 mVrms	997	None	20	Unbal	Float	dBFS	THD+N	-107.00	-104.00	-130.00	n/a	<10Hz->20kHz LP	Narrow	n/a	n/a	3	15	Internal	96000	Analog
ANLG_ZONE2_IN4_TO_DIG_ZONE2_COAX_OUT_96K																							
ANLG_ZONE2_IN4_TO_DIG_ZONE2_COAX_OUT_96K_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	dBFS	Level	-0.40	+0.00	-1.10	n/a	<10 - Fs/2	None	n/a	n/a	4	16	Internal	96000	Analog
ANLG_ZONE2_IN4_TO_DIG_ZONE2_COAX_OUT_96K_FREQ	1	2.00 Vrms	2.00 Vrms	10-20/20-40k	None	20	Unbal	Float	dBr	Level	-0.20/-0.00	+0.10	-0.50/-0.25	n/a	<10 - Fs/2	None	n/a	n/a	4	16	Internal	96000	Analog
ANLG_ZONE2_IN4_TO_DIG_ZONE2_COAX_OUT_96K_THD	1	3.80 Vrms	3.80 Vrms	20-1k/5k-40k	None	20	Unbal	Float	dBFS	THD+N	<-98.00/-86.00	-88.00/-75.00	-120.00	n/a	<10 - Fs/2	None	n/a	n/a	4	16	Internal	96000	Analog
ANLG_ZONE2_IN4_TO_DIG_ZONE2_COAX_OUT_96K_XTALK	1	4.00 Vrms	4.00 Vrms	15k	None	20	Unbal	Float	dB	Level	-86.00	-80.00	-130.00	n/a	<10 - Fs/2	None	n/a	n/a	4	16	Internal	96000	Analog
ANLG_ZONE2_IN4_TO_DIG_ZONE2_COAX_OUT_96K_DYNRNG	1	4.00 mVrms	4.00 mVrms	997	None	20	Unbal	Float	dBFS	THD+N	-107.00	-104.00	-130.00	n/a	<10Hz->20kHz LP	Narrow	n/a	n/a	4	16	Internal	96000	Analog
ANLG_ZONE2_IN5_TO_DIG_ZONE2_COAX_OUT_96K																							
ANLG_ZONE2_IN5_TO_DIG_ZONE2_COAX_OUT_96K_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	dBFS	Level	-0.40	+0.00	-1.10	n/a	<10 - Fs/2	None	n/a	n/a	5	17	Internal	96000	Analog
ANLG_ZONE2_IN5_TO_DIG_ZONE2_COAX_OUT_96K_FREQ	1	2.00 Vrms	2.00 Vrms	10-20/20-40k	None	20	Unbal	Float	dBr	Level	-0.20/-0.00	+0.10	-0.50/-0.25	n/a	<10 - Fs/2	None	n/a	n/a	5	17	Internal	96000	Analog
ANLG_ZONE2_IN5_TO_DIG_ZONE2_COAX_OUT_96K_THD	1	3.80 Vrms	3.80 Vrms	20-1k/5k-40k	None	20	Unbal	Float	dBFS	THD+N	<-98.00/-86.00	-88.00/-75.00	-120.00	n/a	<10 - Fs/2	None	n/a	n/a	5	17	Internal	96000	Analog
ANLG_ZONE2_IN5_TO_DIG_ZONE2_COAX_OUT_96K_XTALK	1	4.00 Vrms	4.00 Vrms	15k	None	20	Unbal	Float	dB	Level	-86.00	-80.00	-130.00	n/a	<10 - Fs/2	None	n/a	n/a	5	17	Internal	96000	Analog
ANLG_ZONE2_IN5_TO_DIG_ZONE2_COAX_OUT_96K_DYNRNG	1	4.00 mVrms	4.00 mVrms	997	None	20	Unbal	Float	dBFS	THD+N	-107.00	-104.00	-130.00	n/a	<10Hz->20kHz LP	Narrow	n/a	n/a	5	17	Internal	96000	Analog
ANLG_ZONE2_IN6_TO_DIG_ZONE2_COAX_OUT_96K																							
ANLG_ZONE2_IN6_TO_DIG_ZONE2_COAX_OUT_96K_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	dBFS	Level	-0.40	+0.00	-1.10	n/a	<10 - Fs/2	None	n/a	n/a	6	18	Internal	96000	Analog
ANLG_ZONE2_IN6_TO_DIG_ZONE2_COAX_OUT_96K_FREQ	1	2.00 Vrms	2.00 Vrms	10-20/20-40k	None	20	Unbal	Float	dBr	Level	-0.20/-0.00	+0.10	-0.50/-0.25	n/a	<10 - Fs/2	None	n/a	n/a	6	18	Internal	96000	Analog
ANLG_ZONE2_IN6_TO_DIG_ZONE2_COAX_OUT_96K_THD	1	3.80 Vrms	3.80 Vrms	20-1k/5k-40k	None	20	Unbal	Float	dBFS	THD+N	<-98.00/-86.00	-88.00/-75.00	-120.00	n/a	<10 - Fs/2	None	n/a	n/a	6	18	Internal	96000	Analog
ANLG_ZONE2_IN6_TO_DIG_ZONE2_COAX_OUT_96K_XTALK	1	4.00 Vrms	4.00 Vrms	15k	None	20	Unbal	Float	dB	Level	-86.00	-80.00	-130.00	n/a	<10 - Fs/2	None	n/a	n/a	6	18	Internal	96000	Analog
ANLG_ZONE2_IN6_TO_DIG_ZONE2_COAX_OUT_96K_DYNRNG	1	4.00 mVrms	4.00 mVrms	997	None	20	Unbal	Float	dBFS	THD+N	-107.00	-104.00	-130.00	n/a	<10Hz->20kHz LP	Narrow	n/a	n/a	6	18	Internal	96000	Analog
ANLG_ZONE2_IN7_TO_DIG_ZONE2_COAX_OUT_96K																							
ANLG_ZONE2_IN7_TO_DIG_ZONE2_COAX_OUT_96K_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	dBFS	Level	-0.40	+0.00	-1.10	n/a	<10 - Fs/2	None	n/a	n/a	7	19	Internal	96000	Analog
ANLG_ZONE2_IN7_TO_DIG_ZONE2_COAX_OUT_96K_FREQ	1	2.00 Vrms	2.00 Vrms	10-20/20-40k	None	20	Unbal	Float	dBr	Level	-0.20/-0.00	+0.10	-0.50/-0.25	n/a	<10 - Fs/2	None	n/a	n/a	7	19	Internal	96000	Analog
ANLG_ZONE2_IN7_TO_DIG_ZONE2_COAX_OUT_96K_THD	1	3.80 Vrms	3.80 Vrms	20-1k/5k-40k	None	20	Unbal	Float	dBFS	THD+N	<-98.00/-86.00	-88.00/-75.00	-120.00	n/a	<10 - Fs/2	None	n/a	n/a	7	19	Internal	96000	Analog
ANLG_ZONE2_IN7_TO_DIG_ZONE2_COAX_OUT_96K_XTALK	1	4.00 Vrms	4.00 Vrms	15k	None	20	Unbal	Float	dB	Level	-86.00	-80.00	-130.00	n/a	<10 - Fs/2	None	n/a	n/a	7	19	Internal	96000	Analog
ANLG_ZONE2_IN7_TO_DIG_ZONE2_COAX_OUT_96K_DYNRNG	1	4.00 mVrms	4.00 mVrms	997	None	20	Unbal	Float	dBFS	THD+N	-107.00	-104.00	-130.00	n/a	<10Hz->20kHz LP	Narrow	n/a	n/a	7	19	Internal	96000	Analog
ANLG_ZONE2_IN8_TO_DIG_ZONE2_COAX_OUT_96K																							
ANLG_ZONE2_IN8_TO_DIG_ZONE2_COAX_OUT_96K_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	dBFS	Level	-0.40	+0.00	-1.10	n/a	<10 - Fs/2	None	n/a	n/a	8	20	Internal	96000	Analog
ANLG_ZONE2_IN8_TO_DIG_ZONE2_COAX_OUT_96K_FREQ	1	2.00 Vrms	2.00 Vrms	10-20/20-40k	None	20	Unbal	Float	dBr	Level	-0.20/-0.00	+0.10	-0.50/-0.25	n/a	<10 - Fs/2	None	n/a	n/a	8	20	Internal	96000	Analog
ANLG_ZONE2_IN8_TO_DIG_ZONE2_COAX_OUT_96K_THD	1	3.80 Vrms	3.80 Vrms	20-1k/5k-40k	None	20	Unbal	Float	dBFS	THD+N	<-98.00/-86.00	-88.00/-75.00	-120.00	n/a	<10 - Fs/2	None	n/a	n/a	8	20	Internal	96000	Analog
ANLG_ZONE2_IN8_TO_DIG_ZONE2_COAX_OUT_96K_XTALK	1	4.00 Vrms	4.00 Vrms	15k	None	20	Unbal	Float	dB	Level	-86.00	-80.00	-130.00	n/a	<10 - Fs/2	None	n/a	n/a	8	20	Internal	96000	Analog
ANLG_ZONE2_IN8_TO_DIG_ZONE2_COAX_OUT_96K_DYNRNG	1	4.00 mVrms	4.00 mVrms	997	None	20	Unbal	Float	dBFS	THD+N	-107.00	-104.00	-130.00	n/a	<10Hz->20kHz LP	Narrow	n/a	n/a	8	20	Internal	96000	Analog
ANLG_ZONE2_IN1_TO_DIG_ZONE2_OPT_OUT_48K																							
ANLG_ZONE2_IN1_TO_DIG_ZONE2_OPT_OUT_48K_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	dBFS	Level	-0.40	+0.00	-1.10	n/a	<10 - Fs/2	None	n/a	n/a	1	13	Internal	48000	Analog
ANLG_ZONE2_IN1_TO_DIG_ZONE2_OPT_OUT_48K_THD	1	3.80 Vrms	3.80 Vrms	997	None	20	Unbal	Float	dBFS	THD+N	<-99.00	-88.00	-120.00	n/a	<10 - Fs/2	None	n/a	n/a	1	13	Internal	48000	Analog
ANLG_ZONE2_IN1_TO_DIG_ZONE2_OPT_OUT_48K_DYNRNG	1	4.00 mVrms	4.00 mVrms	997	None	20	Unbal	Float	dBFS	THD+N	-107.00	-104.00	-130.00	n/a	<10Hz->20kHz LP	Narrow	n/a	n/a	1	13	Internal	48000	Analog
ANLG_ZONE2_IN1_TO_DIG_ZONE2_OPT_OUT_44K																							
ANLG_ZONE2_IN1_TO_DIG_ZONE2_OPT_OUT_44K_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	dBFS	Level	-0.40	+0.00	-1.10	n/a	<10 - Fs/2	None	n/a	n/a	1	13	Internal	44100	Analog
ANLG_ZONE2_IN1_TO_DIG_ZONE2_OPT_OUT_44K_THD	1	3.80 Vrms	3.80 Vrms	997	None	20	Unbal	Float	dBFS	THD+N	<-99.00	-88.00	-120.00	n/a	<10 - Fs/2	None	n/a	n/a	1	13	Internal	44100	Analog
ANLG_ZONE2_IN1_TO_DIG_ZONE2_OPT_OUT_44K_DYNRNG	1	4.00 mVrms	4.00 mVrms	997	None	20	Unbal	Float	dBFS	THD+N	-107.00	-104.00	-130.00	n/a	<10Hz->20kHz LP	Narrow	n/a	n/a	1	13	Internal	44100	Analog
ANLG_ZONE2_PHONO75_IN_TO_DIG_ZONE2_OPT_OUT_44K																							
ANLG_ZONE2_PHONO75_IN_TO_DIG_ZONE2_OPT_OUT_44K_GAIN	1	4.70 mVrms	50.00 mVrms	997	None	20	Unbal	Float	dBFS	Level	-37.40	-36.40	-38.40	n/a	<10 - Fs/2	None	n/a	n/a	11	23	Internal	96000	Analog
ANLG_ZONE2_PHONO75_IN_TO_DIG_ZONE2_OPT_OUT_44K_FREQ	1	16.00 mVrms	16.00 mVrms	20-20k	RIAA-PRE	20	Unbal	Float	dBr	Level	+0.00	+1.00	-1.00	n/a	<10 - Fs/2	None	n/a	n/a	11	23	Internal	96000	Analog
ANLG_ZONE2_PHONO75_IN_TO_DIG_ZONE2_OPT_OUT_44K_THD	1	16.00 mVrms	16.00 mVrms	20-20k	RIAA-PRE	20	Unbal	Float	%	THD+N	<0.01	-0.02	0.0002	n/a	100 - Fs/2	None	n/a	n/a	11	23	Internal	96000	Analog
ANLG_ZONE2_PHONO75_IN_TO_DIG_ZONE2_OPT_OUT_44K_XTALK	1	16.00 mVrms	16.00 mVrms	15k	RIAA-PRE	20	Unbal	Float	dB	Level	<-75.00	-70.00	-120.00	n/a	<10 - Fs/2	None	n/a	n/a	11	23	Internal	96000	Analog
ANLG_ZONE2_PHONO75_IN_TO_DIG_ZONE2_OPT_OUT_44K_DYNRNG	1	4.70 mVrms	16.00 uVrms	997	None	20	Unbal	Float	dBFS	THD+N	-106.00	-100.00	-130.00	n/a	100Hz->20kHz LP	Narrow	n/a	n/a	11	23	Internal	96000	Analog
ANLG_ZONE2_MIC_IN1&2_TO_DIG_ZONE2_OPT_OUT_96K																							
ANLG_ZONE2_MIC_IN1&2_TO_DIG_ZONE2_OPT_OUT_96K_GAIN	1	10.00 mVrms	10.00 mVrms	997	None	40	Bal	Float	dBFS	Level	-26.25	-25.75	-26.75	n/a	<10 - Fs/2	None	n/a	n/a	9	21	Internal	96000	Analog
ANLG_ZONE2_MIC_IN1&2_TO_DIG_ZONE2_OPT_OUT_96K_FREQ	1	10.00 mVrms	10.00 mVrms	20-20k	None	40	Bal	Float	dBr	Level	0.00	+0.10	-0.20	n/a	<10 - Fs/2	None	n/a	n/a	9	21	Internal	96000	Analog
ANLG_ZONE2_MIC_IN1&2_TO_DIG_ZONE2_OPT_OUT_96K_THD	1	10.00 mVrms	10.00 mVrms	997	None	40	Bal	Float	dBFS	THD+N Ampl	>0.25	0.50	0.0005	n/a	<10Hz->20kHz LP	None	n/a	n/a	9	21	Internal	96000	Analog
ANLG_FRONT_IN1_TO_DIG_ZONE2_OPT_OUT_96K																							
ANLG_FRONT_IN1_TO_DIG_ZONE2_OPT_OUT_96K_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	dBFS	Level	-0.38	+0.00	-1.10	n/a	<10 - Fs/2	None	n/a	n/a	1	13	Internal	96000	Analog
ANLG_FRONT_IN1_TO_DIG_ZONE2_OPT_OUT_96K_FREQ	1	2.00 Vrms	2.00 Vrms	10-40k	None	20	Unbal	Float	dBr	Level	-0.20/-0.00	+0.10	-0.50/-0.25	n/a	<10 - Fs/2	None	n/a	n/a	1	13	Internal	96000	Analog
ANLG_FRONT_IN1_TO_DIG_ZONE2_OPT_OUT_96K_THD	1	3.80 Vrms	3.80 Vrms	20-1k/5k-40k	None	20	Unbal	Float	dBFS	THD+N	<-98.00/-86.00	-88.00/-75.00	-120.00	n/a	<10 - Fs/2	None	n/a	n/a	1	13	Internal	96000	Analog
ANLG_FRONT_IN1_TO_DIG_ZONE2_OPT_OUT_96K_XTALK	1	4.00 Vrms	4.00 Vrms	15k	None	20	Unbal	Float	dB	Level	<-115.00	-80.00	-130.00	n/a	<10 - Fs/2	None	n/a	n/a	1	13	Internal	96000	Analog
ANLG_FRONT_IN1_TO_DIG_ZONE2_OPT_OUT_96K_DYNRNG	1	4.00 mVrms	4.00 mVrms	997	None	20	Unbal	Float	dBFS	THD+N	-108.00	-104.00	-130.00	n/a	<10Hz->20kHz LP	Narrow	n/a	n/a	1	13	Internal	96000	Analog
ANLG_FRONT_IN2_TO_DIG_ZONE2_OPT_OUT_96K																							
ANLG_FRONT_IN2_TO_DIG_ZONE2_OPT_OUT_96K_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	dBFS	Level	-0.38	+0.00	-1.10	n/a	<10 - Fs/2	None	n/a	n/a	2	14	Internal	96000	Analog
ANLG_FRONT_IN2_TO_DIG_ZONE2_OPT_OUT_96K_FREQ	1	2.00 Vrms	2.00 Vrms	10-40k	None	20	Unbal	Float	dBr	Level	-0.20/-0.00	+0.10	-0.50/-0.25	n/a	<10 - Fs/2	None	n/a	n/a	2	14	Internal	96000	Analog
ANLG_FRONT_IN2_TO_DIG_ZONE2_OPT_OUT_96K_THD	1	3.80 Vrms	3.80 Vrms	20-1k/5k-40k	None	20	Unbal	Float	dBFS	THD+N	<-98.00/-86.00	-88.00/-75.00	-120.00	n/a	<10 - Fs/2	None	n/a	n/a	2	14	Internal	96000	Analog
ANLG_FRONT_IN2_TO_DIG_ZONE2_OPT_OUT_96K_XTALK	1	4.00 Vrms	4.00 Vrms	15k	None	20	Unbal	Float	dB	Level	<-115.00	-80.00	-130.00	n/a	<10 - Fs/2	None	n/a	n/a	2	14	Internal	96000	Analog
ANLG_FRONT_IN2_TO_DIG_ZONE2_OPT_OUT_96K_DYNRNG	1	4.00 mVrms	4.00 mVrms	997	None	20	Unbal	Float	dBFS	THD+N	-108.00	-104.00	-130.00	n/a	<10Hz->20kHz LP	Narrow	n/a	n/a	2	14	Internal	96000	Analog
ANLG_FRONT_IN3_TO_DIG_ZONE2_OPT_OUT_96K																							
ANLG_FRONT_IN3_TO_DIG_ZONE2_OPT_OUT_96K_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	dBFS	Level	-0.38	+0.00	-1.10	n/a	<10 - Fs/2	None	n/a	n/a	3	15	Internal	96000	Analog
ANLG_FRONT_IN3_TO_DIG_ZONE2_OPT_OUT_96K_FREQ	1	2.00 Vrms	2.00 Vrms	10-40k	None	20	Unbal	Float	dBr	Level	-0.20/-0.00	+0.10	-0.50/-0.25	n/a	<10 - Fs/2	None	n/a	n/a	3	15	Internal	96000	Analog
ANLG_FRONT_IN3_TO_DIG_ZONE2_OPT_OUT_96K_THD	1	3.80 Vrms	3.80 Vrms	20-1k/5k-40k	None	20	Unbal	Float	dBFS	THD+N	<-98.00/-86.00	-88.00/-75.00	-120.00	n/a	<10 - Fs/2	None	n/a	n/a	3	15	Internal	96000	Analog
ANLG_FRONT_IN3_TO_DIG_ZONE2_OPT_OUT_96K_XTALK	1	4.00 Vrms	4.00 Vrms	15k	None	20	Unbal	Float	dB	Level	<-115.00	-80.00	-130.00	n/a	<10 - Fs/2	None	n/a	n/a	3	15	Internal	96000	Analog
ANLG_FRONT_IN3_TO_DIG_ZONE2_OPT_OUT_96K_DYNRNG	1	4.00 mVrms	4.00 mVrms	997	None	20	Unbal	Float	dBFS	THD+N	-108.00	-104.00	-130.00	n/a	<10Hz->20kHz LP	Narrow	n/a	n/a	3	15	Internal	96000	Analog

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A-D Tests		Analog Generator							Digital Analyzer								Switcher Module						
Test Name	See Note:	Left	Right	Freq (Hz)	EQ Curve	Z-out	Bal/ Unbal	Gnd/ Float	Level	Measure	Typical Reading	Upper Limit	Lower Limit	Imp.	Bandwidth	Filter	A In	B In	A Out	B Out	Clock Source	Sample Rate	Audio Source
ANLG_FRONT_IN4_TO_DIG_ZONE2_OPT_OUT_96K																							
ANLG_FRONT_IN4_TO_DIG_ZONE2_OPT_OUT_96K_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	dBFS	Level	-0.38	+0.00	-1.10	n/a	<10 - Fs/2	None	n/a	n/a	4	16	Internal	96000	Analog
ANLG_FRONT_IN4_TO_DIG_ZONE2_OPT_OUT_96K_FREQ	1	2.00 Vrms	2.00 Vrms	10-40k	None	20	Unbal	Float	dBr	Level	-0.20/-0.00	+0.10	-0.50/-0.25	n/a	<10 - Fs/2	None	n/a	n/a	4	16	Internal	96000	Analog
ANLG_FRONT_IN4_TO_DIG_ZONE2_OPT_OUT_96K_THD	1	3.80 Vrms	3.80 Vrms	20-1k/5k-40k	None	20	Unbal	Float	dBFS	THD+N	<-98.00/-86.00	-88.00/-75.00	-120.00	n/a	<10 - Fs/2	None	n/a	n/a	4	16	Internal	96000	Analog
ANLG_FRONT_IN4_TO_DIG_ZONE2_OPT_OUT_96K_XTALK	1	4.00 Vrms	4.00 Vrms	15k	None	20	Unbal	Float	dB	Level	<-115.00	-80.00	-130.00	n/a	<10 - Fs/2	None	n/a	n/a	4	16	Internal	96000	Analog
ANLG_FRONT_IN4_TO_DIG_ZONE2_OPT_OUT_96K_DYNRNG	1	4.00 mVrms	4.00 mVrms	997	None	20	Unbal	Float	dBFS	THD+N	-108.00	-104.00	-130.00	n/a	<10Hz->20kHz LP	Narrow	n/a	n/a	4	16	Internal	96000	Analog
ANLG_FRONT_IN5_TO_DIG_ZONE2_OPT_OUT_96K																							
ANLG_FRONT_IN5_TO_DIG_ZONE2_OPT_OUT_96K_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	dBFS	Level	-0.38	+0.00	-1.10	n/a	<10 - Fs/2	None	n/a	n/a	5	17	Internal	96000	Analog
ANLG_FRONT_IN5_TO_DIG_ZONE2_OPT_OUT_96K_FREQ	1	2.00 Vrms	2.00 Vrms	10-40k	None	20	Unbal	Float	dBr	Level	-0.20/-0.00	+0.10	-0.50/-0.25	n/a	<10 - Fs/2	None	n/a	n/a	5	17	Internal	96000	Analog
ANLG_FRONT_IN5_TO_DIG_ZONE2_OPT_OUT_96K_THD	1	3.80 Vrms	3.80 Vrms	20-1k/5k-40k	None	20	Unbal	Float	dBFS	THD+N	<-98.00/-86.00	-88.00/-75.00	-120.00	n/a	<10 - Fs/2	None	n/a	n/a	5	17	Internal	96000	Analog
ANLG_FRONT_IN5_TO_DIG_ZONE2_OPT_OUT_96K_XTALK	1	4.00 Vrms	4.00 Vrms	15k	None	20	Unbal	Float	dB	Level	<-115.00	-80.00	-130.00	n/a	<10 - Fs/2	None	n/a	n/a	5	17	Internal	96000	Analog
ANLG_FRONT_IN5_TO_DIG_ZONE2_OPT_OUT_96K_DYNRNG	1	4.00 mVrms	4.00 mVrms	997	None	20	Unbal	Float	dBFS	THD+N	-108.00	-104.00	-130.00	n/a	<10Hz->20kHz LP	Narrow	n/a	n/a	5	17	Internal	96000	Analog
ANLG_FRONT_IN6_TO_DIG_ZONE2_OPT_OUT_96K																							
ANLG_FRONT_IN6_TO_DIG_ZONE2_OPT_OUT_96K_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	dBFS	Level	-0.38	+0.00	-1.10	n/a	<10 - Fs/2	None	n/a	n/a	6	18	Internal	96000	Analog
ANLG_FRONT_IN6_TO_DIG_ZONE2_OPT_OUT_96K_FREQ	1	2.00 Vrms	2.00 Vrms	10-40k	None	20	Unbal	Float	dBr	Level	-0.20/-0.00	+0.10	-0.50/-0.25	n/a	<10 - Fs/2	None	n/a	n/a	6	18	Internal	96000	Analog
ANLG_FRONT_IN6_TO_DIG_ZONE2_OPT_OUT_96K_THD	1	3.80 Vrms	3.80 Vrms	20-1k/5k-40k	None	20	Unbal	Float	dBFS	THD+N	<-98.00/-86.00	-88.00/-75.00	-120.00	n/a	<10 - Fs/2	None	n/a	n/a	6	18	Internal	96000	Analog
ANLG_FRONT_IN6_TO_DIG_ZONE2_OPT_OUT_96K_XTALK	1	4.00 Vrms	4.00 Vrms	15k	None	20	Unbal	Float	dB	Level	<-115.00	-80.00	-130.00	n/a	<10 - Fs/2	None	n/a	n/a	6	18	Internal	96000	Analog
ANLG_FRONT_IN6_TO_DIG_ZONE2_OPT_OUT_96K_DYNRNG	1	4.00 mVrms	4.00 mVrms	997	None	20	Unbal	Float	dBFS	THD+N	-108.00	-104.00	-130.00	n/a	<10Hz->20kHz LP	Narrow	n/a	n/a	6	18	Internal	96000	Analog
ANLG_FRONT_IN7_TO_DIG_ZONE2_OPT_OUT_96K																							
ANLG_FRONT_IN7_TO_DIG_ZONE2_OPT_OUT_96K_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	dBFS	Level	-0.38	+0.00	-1.10	n/a	<10 - Fs/2	None	n/a	n/a	7	19	Internal	96000	Analog
ANLG_FRONT_IN7_TO_DIG_ZONE2_OPT_OUT_96K_FREQ	1	2.00 Vrms	2.00 Vrms	10-40k	None	20	Unbal	Float	dBr	Level	-0.20/-0.00	+0.10	-0.50/-0.25	n/a	<10 - Fs/2	None	n/a	n/a	7	19	Internal	96000	Analog
ANLG_FRONT_IN7_TO_DIG_ZONE2_OPT_OUT_96K_THD	1	3.80 Vrms	3.80 Vrms	20-1k/5k-40k	None	20	Unbal	Float	dBFS	THD+N	<-98.00/-86.00	-88.00/-75.00	-120.00	n/a	<10 - Fs/2	None	n/a	n/a	7	19	Internal	96000	Analog
ANLG_FRONT_IN7_TO_DIG_ZONE2_OPT_OUT_96K_XTALK	1	4.00 Vrms	4.00 Vrms	15k	None	20	Unbal	Float	dB	Level	<-115.00	-80.00	-130.00	n/a	<10 - Fs/2	None	n/a	n/a	7	19	Internal	96000	Analog
ANLG_FRONT_IN7_TO_DIG_ZONE2_OPT_OUT_96K_DYNRNG	1	4.00 mVrms	4.00 mVrms	997	None	20	Unbal	Float	dBFS	THD+N	-108.00	-104.00	-130.00	n/a	<10Hz->20kHz LP	Narrow	n/a	n/a	7	19	Internal	96000	Analog
ANLG_FRONT_IN8_TO_DIG_ZONE2_OPT_OUT_96K																							
ANLG_FRONT_IN8_TO_DIG_ZONE2_OPT_OUT_96K_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	dBFS	Level	-0.38	+0.00	-1.10	n/a	<10 - Fs/2	None	n/a	n/a	8	20	Internal	96000	Analog
ANLG_FRONT_IN8_TO_DIG_ZONE2_OPT_OUT_96K_FREQ	1	2.00 Vrms	2.00 Vrms	10-40k	None	20	Unbal	Float	dBr	Level	-0.20/-0.00	+0.10	-0.50/-0.25	n/a	<10 - Fs/2	None	n/a	n/a	8	20	Internal	96000	Analog
ANLG_FRONT_IN8_TO_DIG_ZONE2_OPT_OUT_96K_THD	1	3.80 Vrms	3.80 Vrms	20-1k/5k-40k	None	20	Unbal	Float	dBFS	THD+N	<-98.00/-86.00	-88.00/-75.00	-120.00	n/a	<10 - Fs/2	None	n/a	n/a	8	20	Internal	96000	Analog
ANLG_FRONT_IN8_TO_DIG_ZONE2_OPT_OUT_96K_XTALK	1	4.00 Vrms	4.00 Vrms	15k	None	20	Unbal	Float	dB	Level	<-115.00	-80.00	-130.00	n/a	<10 - Fs/2	None	n/a	n/a	8	20	Internal	96000	Analog
ANLG_FRONT_IN8_TO_DIG_ZONE2_OPT_OUT_96K_DYNRNG	1	4.00 mVrms	4.00 mVrms	997	None	20	Unbal	Float	dBFS	THD+N	-108.00	-104.00	-130.00	n/a	<10Hz->20kHz LP	Narrow	n/a	n/a	8	20	Internal	96000	Analog
ANLG_FRONT_IN1_TO_DIG_ZONE2_OPT_OUT_48K																							
ANLG_FRONT_IN1_TO_DIG_ZONE2_OPT_OUT_48K_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	dBFS	Level	-0.40	+0.00	-1.10	n/a	<10 - Fs/2	None	n/a	n/a	1	13	Internal	48000	Analog
ANLG_FRONT_IN1_TO_DIG_ZONE2_OPT_OUT_48K_THD	1	3.80 Vrms	3.80 Vrms	997	None	20	Unbal	Float	dBFS	THD+N	<-99.00	-88.00	-120.00	n/a	<10 - Fs/2	None	n/a	n/a	1	13	Internal	48000	Analog
ANLG_FRONT_IN1_TO_DIG_ZONE2_OPT_OUT_48K_DYNRNG	1	4.00 mVrms	4.00 mVrms	997	None	20	Unbal	Float	dBFS	THD+N	-107.00	-104.00	-130.00	n/a	<10Hz->20kHz LP	Narrow	n/a	n/a	1	13	Internal	48000	Analog
ANLG_FRONT_IN1_TO_DIG_ZONE2_OPT_OUT_44K																							
ANLG_FRONT_IN1_TO_DIG_ZONE2_OPT_OUT_44K_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	dBFS	Level	-0.40	+0.00	-1.10	n/a	<10 - Fs/2	None	n/a	n/a	1	13	Internal	44100	Analog
ANLG_FRONT_IN1_TO_DIG_ZONE2_OPT_OUT_44K_THD	1	3.80 Vrms	3.80 Vrms	997	None	20	Unbal	Float	dBFS	THD+N	<-99.00	-88.00	-120.00	n/a	<10 - Fs/2	None	n/a	n/a	1	13	Internal	44100	Analog
ANLG_FRONT_IN1_TO_DIG_ZONE2_OPT_OUT_44K_DYNRNG	1	4.00 mVrms	4.00 mVrms	997	None	20	Unbal	Float	dBFS	THD+N	-107.00	-104.00	-130.00	n/a	<10Hz->20kHz LP	Narrow	n/a	n/a	1	13	Internal	44100	Analog
ANLG_FRONT_PHONO75_IN_TO_DIG_ZONE2_OPT_OUT_44K																							
ANLG_FRONT_PHONO75_IN_TO_DIG_ZONE2_OPT_OUT_44K_GAIN	1	4.70 mVrms	50.00 mVrms	997	None	20	Unbal	Float	dBFS	Level	-37.40	-36.40	-38.40	n/a	<10 - Fs/2	None	n/a	n/a	11	23	Internal	96000	Analog
ANLG_FRONT_PHONO75_IN_TO_DIG_ZONE2_OPT_OUT_44K_FREQ	1	16.00 mVrms	16.00 mVrms	20-20k	RIAA-PRE	20	Unbal	Float	dBr	Level	+0.00	+1.00	-1.00	n/a	<10 - Fs/2	None	n/a	n/a	11	23	Internal	96000	Analog
ANLG_FRONT_PHONO75_IN_TO_DIG_ZONE2_OPT_OUT_44K_THD	1	16.00 mVrms	16.00 mVrms	20-20k	RIAA-PRE	20	Unbal	Float	%	THD+N	<0.01	-0.02	0.0002	n/a	100 - Fs/2	None	n/a	n/a	11	23	Internal	96000	Analog
ANLG_FRONT_PHONO75_IN_TO_DIG_ZONE2_OPT_OUT_44K_XTALK	1	16.00 mVrms	16.00 mVrms	15k	RIAA-PRE	20	Unbal	Float	dB	Level	<-75.00	-70.00	-120.00	n/a	<10 - Fs/2	None	n/a	n/a	11	23	Internal	96000	Analog
ANLG_FRONT_PHONO75_IN_TO_DIG_ZONE2_OPT_OUT_44K_DYNRNG	1	4.70 mVrms	16.00 uVrms	997	None	20	Unbal	Float	dBFS	THD+N	-106.00	-100.00	-130.00	n/a	100Hz->20kHz LP	Narrow	n/a	n/a	11	23	Internal	96000	Analog
ANLG_FRONT_MIC_IN1&2_TO_DIG_ZONE2_OPT_OUT_96K																							
ANLG_FRONT_MIC_IN1&2_TO_DIG_ZONE2_OPT_OUT_96K_GAIN	1	10.00 mVrms	10.00 mVrms	997	None	40	Bal	Float	dBFS	Level	-26.25	-25.75	-26.75	n/a	<10 - Fs/2	None	n/a	n/a	9	21	Internal	96000	Analog
ANLG_FRONT_MIC_IN1&2_TO_DIG_ZONE2_OPT_OUT_96K_FREQ	1	10.00 mVrms	10.00 mVrms	20-20k	None	40	Bal	Float	dBr	Level	0.00	+0.10	-0.20	n/a	<10 - Fs/2	None	n/a	n/a	9	21	Internal	96000	Analog
ANLG_FRONT_MIC_IN1&2_TO_DIG_ZONE2_OPT_OUT_96K_THD	1	10.00 mVrms	10.00 mVrms	997	None	40	Bal	Float	dBFS	THD+N Ampl	>0.25	0.50	0.0005	n/a	<10Hz->20kHz LP	None	n/a	n/a	9	21	Internal	96000	Analog
ANLG_CENTER_LFE_IN4_TO_DIG_ZONE2_OPT_OUT_96K																							
ANLG_CENTER_LFE_IN4_TO_DIG_ZONE2_OPT_OUT_96K_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	dBFS	Level	-0.38	+0.00	-1.10	n/a	<10 - Fs/2	None	n/a	n/a	4	16	Internal	96000	Analog
ANLG_CENTER_LFE_IN4_TO_DIG_ZONE2_OPT_OUT_96K_FREQ	1	2.00 Vrms	2.00 Vrms	10-40k	None	20	Unbal	Float	dBr	Level	-0.20/-0.00	+0.10	-0.50/-0.25	n/a	<10 - Fs/2	None	n/a	n/a	4	16	Internal	96000	Analog
ANLG_CENTER_LFE_IN4_TO_DIG_ZONE2_OPT_OUT_96K_THD	1	3.80 Vrms	3.80 Vrms	20-1k/5k-40k	None	20	Unbal	Float	dBFS	THD+N	<-98.00/-86.00	-88.00/-75.00	-120.00	n/a	<10 - Fs/2	None	n/a	n/a	4	16	Internal	96000	Analog
ANLG_CENTER_LFE_IN4_TO_DIG_ZONE2_OPT_OUT_96K_XTALK	1	4.00 Vrms	4.00 Vrms	15k	None	20	Unbal	Float	dB	Level	<-115.00	-80.00	-130.00	n/a	<10 - Fs/2	None	n/a	n/a	4	16	Internal	96000	Analog
ANLG_CENTER_LFE_IN4_TO_DIG_ZONE2_OPT_OUT_96K_DYNRNG	1	4.00 mVrms	4.00 mVrms	997	None	20	Unbal	Float	dBFS	THD+N	-108.00	-104.00	-130.00	n/a	<10Hz->20kHz LP	Narrow	n/a	n/a	4	16	Internal	96000	Analog
ANLG_CENTER_LFE_IN7_TO_DIG_ZONE2_OPT_OUT_44K																							
ANLG_CENTER_LFE_IN7_TO_DIG_ZONE2_OPT_OUT_44K_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	dBFS	Level	-0.38	+0.00	-1.10	n/a	<10 - Fs/2	None	n/a	n/a	7	19	Internal	44100	Analog
ANLG_CENTER_LFE_IN7_TO_DIG_ZONE2_OPT_OUT_44K_FREQ	1	2.00 Vrms	2.00 Vrms	10-20k	None	20	Unbal	Float	dBr	Level	-0.20/-0.00	+0.10	-0.50/-0.25	n/a	<10 - Fs/2	None	n/a	n/a	7	19	Internal	44100	Analog
ANLG_CENTER_LFE_IN7_TO_DIG_ZONE2_OPT_OUT_44K_THD	1	3.80 Vrms	3.80 Vrms	20-1k/5k-40k	None	20	Unbal	Float	dBFS	THD+N	<-98.00/-86.00	-88.00/-75.00	-120.00	n/a	<10 - Fs/2	None	n/a	n/a	7	19	Internal	44100	Analog
ANLG_CENTER_LFE_IN7_TO_DIG_ZONE2_OPT_OUT_44K_DYNRNG	1	4.00 mVrms	4.00 mVrms	997	None	20	Unbal	Float	dBFS	THD+N	-108.00	-104.00	-130.00	n/a	<10Hz->20kHz LP	Narrow	n/a	n/a	7	19	Internal	44100	Analog
ANLG_SIDE_IN5_TO_DIG_ZONE2_OPT_OUT_96K																							
ANLG_SIDE_IN5_TO_DIG_ZONE2_OPT_OUT_96K_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	dBFS	Level	-0.38	+0.00	-1.10	n/a	<10 - Fs/2	None	n/a	n/a	5	17	Internal	96000	Analog
ANLG_SIDE_IN5_TO_DIG_ZONE2_OPT_OUT_96K_FREQ	1	2.00 Vrms	2.00 Vrms	10-40k	None	20	Unbal	Float	dBr	Level	-0.20/-0.00	+0.10	-0.50/-0.25	n/a	<10 - Fs/2	None	n/a	n/a	5	17	Internal	96000	Analog
ANLG_SIDE_IN5_TO_DIG_ZONE2_OPT_OUT_96K_THD	1	3.80 Vrms	3.80 Vrms	20-1k/5k-40k	None	20	Unbal	Float	dBFS	THD+N	<-98.00/-86.00	-88.00/-75.00	-120.00	n/a	<10 - Fs/2	None	n/a	n/a	5	17	Internal	96000	Analog
ANLG_SIDE_IN5_TO_DIG_ZONE2_OPT_OUT_96K_XTALK	1	4.00 Vrms	4.00 Vrms	15k	None	20	Unbal	Float	dB	Level	<-115.00	-80.00	-130.00	n/a	<10 - Fs/2	None	n/a	n/a	5	17	Internal	96000	Analog
ANLG_SIDE_IN5_TO_DIG_ZONE2_OPT_OUT_96K_DYNRNG	1	4.00 mVrms	4.00 mVrms	997	None	20	Unbal	Float	dBFS	THD+N	-108.00	-104.00	-130.00	n/a	<10Hz->20kHz LP	Narrow	n/a	n/a	5	17	Internal	96000	Analog
ANLG_SIDE_IN8_TO_DIG_ZONE2_OPT_OUT_44K																							
ANLG_SIDE_IN8_TO_DIG_ZONE2_OPT_OUT_44K_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	dBFS	Level	-0.38	+0.00	-1.10	n/a	<10 - Fs/2	None	n/a	n/a	8	20	Internal	44100	Analog
ANLG_SIDE_IN8_TO_DIG_ZONE2_OPT_OUT_44K_FREQ	1	2.00 Vrms	2.00 Vrms	10-20k	None	20	Unbal	Float	dBr	Level	-0.20/-0.00	+0.10	-0.50/-0.25	n/a	<10 - Fs/2	None	n/a	n/a	8	20	Internal	44100	Analog
ANLG_SIDE_IN8_TO_DIG_ZONE2_OPT_OUT_44K_THD	1	3.80 Vrms	3.80 Vrms	20-1k/5k-40k	None	20	Unbal	Float	dBFS	THD+N	<-98.00/-86.00	-88.00/-75.00	-120.00	n/a	<10 - Fs/2	None	n/a	n/a	8	20	Internal	44100	Analog
ANLG_SIDE_IN8_TO_DIG_ZONE2_OPT_OUT_44K_DYNRNG	1	4.00 mVrms	4.00 mVrms	997	None	20	Unbal	Float	dBFS	THD+N	-108.00	-104.00	-130.00	n/a	<10Hz->20kHz LP	Narrow	n/a	n/a	8	20	Internal	44100	Analog
ANLG_SIDE_MIC_IN1&2_TO_DIG_ZONE2_OPT_OUT_96K																							
ANLG_SIDE_MIC_IN1&2_TO_DIG_ZONE2_OPT_OUT_96K_GAIN	1	10.00 mVrms	10.00 mVrms	997	None	40	Bal	Float	dBFS	Level	-26.25	-25.75	-26.75	n/a	<10 - Fs/2	None	n/a	n/a	9	21	Internal	96000	Analog
ANLG_SIDE_MIC_IN1&2_TO_DIG_ZONE2_OPT_OUT_96K_FREQ	1	10.00 mVrms	10.00 mVrms	20-20k	None	40	Bal	Float	dBr	Level	0.00	+0.10	-0.20	n/a	<10 - Fs/2	None	n/a	n/a	9	21	Internal	96000	Analog
ANLG_SIDE_MIC_IN1&2_TO_DIG_ZONE2_OPT_OUT_96K_THD	1	10.00 mVrms	10.00 mVrms	997	None	40	Bal	Float	dBFS	THD+N Ampl	>0.25	0.50	0.0005	n/a	<10Hz->20kHz LP	None	n/a	n/a	9	21	Internal	96000	Analog

D-A Tests		Digital Generator							Analog Analyzer								Switcher Module						
Test Name	See Note:	Left	Right	Freq (Hz)	EQ Curve	Z-out	Bal/ Unbal	Gnd/ Float	Level	Measure	Typical Reading	Upper Limit	Lower Limit	Imp.	Bandwidth	Filter	A In	B In	A Out	B Out	Clock Source	Sample Rate	Audio Source
DIG_ZONE2_COAX1_IN_96K_TO_ANLG_ZONE2_FIX_OUT																							
DIG_ZONE2_COAX1_IN_96K_TO_ANLG_ZONE2_FIX_OUT_GAIN	1	+0.00 dBFS	+0.00 dBFS	997	None	n/a	n/a	n/a	Vrms	Level	+4.20	+4.50	+3.50	100k	<10 - >500k	None	6	18	n/a	n/a	External	96000	Digital
DIG_ZONE2_COAX1_IN_96K_TO_ANLG_ZONE2_FIX_OUT_FREQ	1	-1.00 dBFS	-1.00 dBFS	10-20k/20k-40k	None	n/a	n/a	n/a	dBr	Level	<-0.10/-.10	+0.10	-0.25/-0.75	100k	<10 - >500k	None	6	18	n/a	n/a	External	96000	Digital
DIG_ZONE2_COAX1_IN_96K_TO_ANLG_ZONE2_FIX_OUT_THD	1	-12.00 dBFS	-12.00 dBFS	20-1k/1k-40k	None	n/a	n/a	n/a	%	THD+N	<.0025/.004	.005/.010	.0002	100k	<10 - 22k	None	6	18	n/a	n/a	External	96000	Digital
DIG_ZONE2_COAX1_IN_96K_TO_ANLG_ZONE2_FIX_OUT_XTALK	1	-1.00 dBFS	-1.00 dBFS	15k	None	n/a	n/a	n/a	dB	Level	>-98.00	-75.00	-150.00	100k	<10 - 22k	None	6	18	n/a	n/a	External	96000	Digital
DIG_ZONE2_COAX1_IN_96K_TO_ANLG_ZONE2_FIX_OUT_DYNRNG	1	-60.00 dBFS	-60.00 dBFS	997	None	n/a	n/a	n/a	dBr	THD+N	>-112.00	-105.00	-1000.00	100k	<10 - 22k	None	6	18	n/a	n/a	External	96000	Digital
DIG_ZONE2_COAX1_IN_96K_TO_ANLG_ZONE2_FIX_OUT_CLKRNG	1	-12.00 dBFS	-12.00 dBFS	997	None	n/a	n/a	n/a	%	THD+N	>-100.00	-86.00	-130.00	100k	<10 - 22k	None	6	18	n/a	n/a	External	95000-97000	Digital
DIG_ZONE2_COAX1_IN_48K_TO_ANLG_ZONE2_FIX_OUT																							
DIG_ZONE2_COAX1_IN_48K_TO_ANLG_ZONE2_FIX_OUT_GAIN	1	+0.00 dBFS	+0.00 dBFS	997	None	n/a	n/a	n/a	Vrms	Level	+4.20	+4.50	+3.500	100k	<10 - >500k	None	6	18	n/a	n/a	External	48000	Digital
DIG_ZONE2_COAX1_IN_48K_TO_ANLG_ZONE2_FIX_OUT_THD	1	-12.00 dBFS	-12.00 dBFS	997	None	n/a	n/a	n/a	%	THD+N	<.002	.005	.0002	100k	<10 - 22k	None	6	18	n/a	n/a	External	48000	Digital
DIG_ZONE2_COAX1_IN_48K_TO_ANLG_ZONE2_FIX_OUT_DYNRNG	1	-60.00 dBFS	-60.00 dBFS	997	None	n/a	n/a	n/a	dBr	THD+N	>-112.00	-105.00	-1000.00	100k	<10 - 22k	None	6	18	n/a	n/a	External	96000	Digital
DIG_ZONE2_COAX1_IN_44K_TO_ANLG_ZONE2_FIX_OUT																							
DIG_ZONE2_COAX1_IN_44K_TO_ANLG_ZONE2_FIX_OUT_GAIN	1	+0.00 dBFS	+0.00 dBFS	997	None	n/a	n/a	n/a	Vrms	Level	+4.20	+4.50	+3.500	100k	<10 - >500k	None	6	18	n/a	n/a	External	44100	Digital
DIG_ZONE2_COAX1_IN_44K_TO_ANLG_ZONE2_FIX_OUT_THD	1	-12.00 dBFS	-12.00 dBFS	997	None	n/a	n/a	n/a	%	THD+N	<.002	.005	.0002	100k	<10 - 22k	None	6	18	n/a	n/a	External	44100	Digital
DIG_ZONE2_COAX1_IN_44K_TO_ANLG_ZONE2_FIX_OUT_DYNRNG	1	-60.00 dBFS	-60.00 dBFS	997	None	n/a	n/a	n/a	dBr	THD+N	>-112.00	-105.00	-1000.00	100k	<10 - 22k	None	6	18	n/a	n/a	External	96000	Digital
DIG_ZONE2_COAX1_IN_44K_TO_ANLG_ZONE2_FIX_OUT_CLKRNG	1	-1.00 dBFS	-1.00 dBFS	997	None	n/a	n/a	n/a	%	THD+N	>-94.50	-70.00	-120.00	100k	<10 - 22k	None	6	18	n/a	n/a	External	43650-44550	Digital
DIG_ZONE2_COAX1_IN_44K_TO_ANLG_ZONE2_VAR_OUT																							
DIG_ZONE2_COAX1_IN_44K_TO_ANLG_ZONE2_VAR_OUT_GAIN	1	+0.00 dBFS	+0.00 dBFS	997	None	n/a	n/a	n/a	Vrms	Level	+4.20	+4.50	+3.500	100k	<10 - >500k	None	7	19	n/a	n/a	External	44100	Digital
DIG_ZONE2_COAX1_IN_44K_TO_ANLG_ZONE2_VAR_OUT_FREQ	1	-1.00 dBFS	-1.00 dBFS	10-20k/20k-40k	None	n/a	n/a	n/a	dBr	Level	<-0.10/-.10	+0.10	-0.25/-0.75	100k	<10 - >500k	None	7	19	n/a	n/a	External	44100	Digital
DIG_ZONE2_COAX1_IN_44K_TO_ANLG_ZONE2_VAR_OUT_THD	1	-12.00 dBFS	-12.00 dBFS	20-1k/1k-20k	None	n/a	n/a	n/a	%	THD+N	<.0025/.004	.005/.010	.0002	100k	<10 - 22k	None	7	19	n/a	n/a	External	44100	Digital
DIG_ZONE2_COAX1_IN_44K_TO_ANLG_ZONE2_VAR_OUT_XTALK	1	-1.00 dBFS	-1.00 dBFS	15k	None	n/a	n/a	n/a	dB	Level	>-90.00	-86.00	-130.00	100k	<10 - 22k	None	7	19	n/a	n/a	External	44100	Digital
DIG_ZONE2_COAX1_IN_44K_TO_ANLG_ZONE2_VAR_OUT_DYNRNG	1	-60.00 dBFS	-60.00 dBFS	997	None	n/a	n/a	n/a	dBr	THD+N	>-112.00	-105.00	-1000.00	100k	<10 - 22k	None	6	18	n/a	n/a	External	96000	Digital
DIG_ZONE2_COAX1_IN_44K_TO_ANLG_ZONE2_VAR_OUT_CLKRNG	1	-12.00 dBFS	-12.00 dBFS	997	None	n/a	n/a	n/a	%	THD+N	>-100.00	-86.00	-130.00	100k	<10 - 22k	None	6	18	n/a	n/a	External	95000-97000	Digital
DIG_ZONE2_COAX2_IN_44K_TO_ANLG_ZONE2_VAR_OUT																							
DIG_ZONE2_COAX2_IN_44K_TO_ANLG_ZONE2_VAR_OUT_GAIN	1	+0.00 dBFS	+0.00 dBFS	997	None	n/a	n/a	n/a	Vrms	Level	+4.20	+4.50	+3.590	100k	<10 - >500k	None	7	19	n/a	n/a	External	44100	Digital
DIG_ZONE2_COAX2_IN_44K_TO_ANLG_ZONE2_VAR_OUT_THD	1	-12.00 dBFS	-12.00 dBFS	997	None	n/a	n/a	n/a	%	THD+N	<.002	.005	.0002	100k	<10 - 22k	None	7	19	n/a	n/a	External	44100	Digital
DIG_ZONE2_COAX3_IN_44K_TO_ANLG_ZONE2_VAR_OUT																							
DIG_ZONE2_COAX3_IN_44K_TO_ANLG_ZONE2_VAR_OUT_GAIN	1	+0.00 dBFS	+0.00 dBFS	997	None	n/a	n/a	n/a	Vrms	Level	+4.20	+4.50	+3.590	100k	<10 - >500k	None	7	19	n/a	n/a	External	44100	Digital
DIG_ZONE2_COAX3_IN_44K_TO_ANLG_ZONE2_VAR_OUT_THD	1	-12.00 dBFS	-12.00 dBFS	997	None	n/a	n/a	n/a	%	THD+N	<.002	.005	.0002	100k	<10 - 22k	None	7	19	n/a	n/a	External	44100	Digital
DIG_ZONE2_COAX4_IN_44K_TO_ANLG_ZONE2_VAR_OUT																							
DIG_ZONE2_COAX4_IN_44K_TO_ANLG_ZONE2_VAR_OUT_GAIN	1	+0.00 dBFS	+0.00 dBFS	997	None	n/a	n/a	n/a	Vrms	Level	+4.20	+4.50	+3.590	100k	<10 - >500k	None	7	19	n/a	n/a	External	44100	Digital
DIG_ZONE2_COAX4_IN_44K_TO_ANLG_ZONE2_VAR_OUT_THD	1	-12.00 dBFS	-12.00 dBFS	997	None	n/a	n/a	n/a	%	THD+N	<.002	.005	.0002	100k	<10 - 22k	None	7	19	n/a	n/a	External	44100	Digital
DIG_ZONE2_OPT1_IN_44K_TO_ANLG_ZONE2_VAR_OUT																							
DIG_ZONE2_OPT1_IN_44K_TO_ANLG_ZONE2_VAR_OUT_GAIN	1	+0.00 dBFS	+0.00 dBFS	997	None	n/a	n/a	n/a	Vrms	Level	+4.20	+4.50	+3.590	100k	<10 - >500k	None	7	19	n/a	n/a	External	44100	Digital
DIG_ZONE2_OPT1_IN_44K_TO_ANLG_ZONE2_VAR_OUT_THD	1	-12.00 dBFS	-12.00 dBFS	997	None	n/a	n/a	n/a	%	THD+N	<.002	.005	.0002	100k	<10 - 22k	None	7	19	n/a	n/a	External	44100	Digital
DIG_ZONE2_OPT2_IN_44K_TO_ANLG_ZONE2_VAR_OUT																							
DIG_ZONE2_OPT2_IN_44K_TO_ANLG_ZONE2_VAR_OUT_GAIN	1	+0.00 dBFS	+0.00 dBFS	997	None	n/a	n/a	n/a	Vrms	Level	+4.20	+4.50	+3.590	100k	<10 - >500k	None	7	19	n/a	n/a	External	44100	Digital
DIG_ZONE2_OPT2_IN_44K_TO_ANLG_ZONE2_VAR_OUT_THD	1	-12.00 dBFS	-12.00 dBFS	997	None	n/a	n/a	n/a	%	THD+N	<.002	.005	.0002	100k	<10 - 22k	None	7	19	n/a	n/a	External	44100	Digital
DIG_ZONE2_OPT3_IN_44K_TO_ANLG_ZONE2_VAR_OUT																							
DIG_ZONE2_OPT3_IN_44K_TO_ANLG_ZONE2_VAR_OUT_GAIN	1	+0.00 dBFS	+0.00 dBFS	997	None	n/a	n/a	n/a	Vrms	Level	+4.20	+4.50	+3.590	100k	<10 - >500k	None	7	19	n/a	n/a	External	44100	Digital
DIG_ZONE2_OPT3_IN_44K_TO_ANLG_ZONE2_VAR_OUT_THD	1	-12.00 dBFS	-12.00 dBFS	997	None	n/a	n/a	n/a	%	THD+N	<.002	.005	.0002	100k	<10 - 22k	None	7	19	n/a	n/a	External	44100	Digital
DIG_ZONE2_OPT4_IN_44K_TO_ANLG_ZONE2_VAR_OUT																							
DIG_ZONE2_OPT4_IN_44K_TO_ANLG_ZONE2_VAR_OUT_GAIN	1	+0.00 dBFS	+0.00 dBFS	997	None	n/a	n/a	n/a	Vrms	Level	+4.20	+4.50	+3.590	100k	<10 - >500k	None	7	19	n/a	n/a	External	44100	Digital
DIG_ZONE2_OPT4_IN_44K_TO_ANLG_ZONE2_VAR_OUT_THD	1	-12.00 dBFS	-12.00 dBFS	997	None	n/a	n/a	n/a	%	THD+N	<.002	.005	.0002	100k	<10 - 22k	None	7	19	n/a	n/a	External	44100	Digital
DIG_ZONE2_OPT1_IN_96K_TO_ANLG_ZONE3_VAR_OUT																							
DIG_ZONE2_OPT1_IN_96K_TO_ANLG_ZONE3_VAR_OUT_GAIN	1	+0.00 dBFS	+0.00 dBFS	997	None	n/a	n/a	n/a	Vrms	Level	+4.20	+4.50	+3.590	100k	<10 - >500k	None	9	21	n/a	n/a	External	96000	Digital
DIG_ZONE2_OPT1_IN_96K_TO_ANLG_ZONE3_VAR_OUT_FREQ	1	-1.00 dBFS	-1.00 dBFS	10-20k/20k-40k	None	n/a	n/a	n/a	dBr	Level	<-0.10/-.10	+0.10	-0.25/-0.75	100k	<10 - >500k	None	9	21	n/a	n/a	External	96000	Digital
DIG_ZONE2_OPT1_IN_96K_TO_ANLG_ZONE3_VAR_OUT_THD	1	-12.00 dBFS	-12.00 dBFS	20-1k/1k-40k	None	n/a	n/a	n/a	%	THD+N	<.0025/.004	.005/.010	.0002	100k	<10 - 22k	None	9	21	n/a	n/a	External	96000	Digital
DIG_ZONE2_OPT1_IN_96K_TO_ANLG_ZONE3_VAR_OUT_XTALK	1	-1.00 dBFS	-1.00 dBFS	15k	None	n/a	n/a	n/a	dB	Level	>-98.00	-75.00	-150.00	100k	<10 - 22k	None	9	21	n/a	n/a	External	96000	Digital
DIG_ZONE2_OPT1_IN_96K_TO_ANLG_ZONE3_VAR_OUT_DYNRNG	1	-60.00 dBFS	-60.00 dBFS	997	None	n/a	n/a	n/a	dBr	THD+N	>-112.00	-105.00	-1000.00	100k	<10 - 22k	None	9	21	n/a	n/a	External	96000	Digital
DIG_MAIN_OPT1_IN_96K_TO_ANLG_MAIN_OUT																							
DIG_MAIN_OPT1_IN_96K_TO_ANLG_MAIN_OUT_GAIN	1	+0.00 dBFS	+0.00 dBFS	997	None	n/a	n/a	n/a	Vrms	Level	+3.57	+3.63	+3.28	100k	<10 - >500k	None	1-6	13-18	n/a	n/a	External	96000	Digital
DIG_MAIN_OPT1_IN_96K_TO_ANLG_MAIN_OUT_FREQ	1	-1.00 dBFS	-1.00 dBFS	10-20/20-20k/20k-40k	None	n/a	n/a	n/a	dBr	Level	<-0.20/0.0/-0.20	+0.10	-0.5/-0.2/-0.75	100k	<10 - >500k	None	1-6	13-18	n/a	n/a	External	96000	Digital
DIG_MAIN_OPT1_IN_96K_TO_ANLG_MAIN_OUT_THD	1	-10.00 dBFS	-10.00 dBFS	20-20k	None	n/a	n/a	n/a	%	THD+N	<.002	.005	.0002	100k	<10 - 22k	None	1-6	13-18	n/a	n/a	External	96000	Digital
DIG_MAIN_OPT1_IN_96K_TO_ANLG_MAIN_OUT_XTALK	1	-1.00 dBFS	-1.00 dBFS	15k	None	n/a	n/a	n/a	dB	Level	>-85.00	-70.00	-150.00	100k	<10 - 22k	None	1-6	13-18	n/a	n/a	External	96000	Digital
DIG_MAIN_OPT1_IN_96K_TO_ANLG_MAIN_OUT_DYNRNG	1	-61.20 dBFS	-61.20 dBFS	997	None	n/a	n/a	n/a	dBr	THD+N	>-109.00	-105.00	-1000.00	100k	<10 - 22k	None	1-6	13-18	n/a	n/a	External	96000	Digital
DIG_MAIN_OPT1_IN_96K_TO_ANLG_MAIN_OUT_CLKRNG	1	-10.00 dBFS	-10.00 dBFS	997	None	n/a	n/a	n/a	%	THD+N	>-100.00	-86.00	-130.00	100k	<10 - 22k	None	1	n/a	n/a	n/a	External	95000-97000	Digital
DIG_MAIN_OPT1_IN_48K_TO_ANLG_MAIN_OUT																							
DIG_MAIN_OPT1_IN_48K_TO_ANLG_MAIN_OUT_GAIN	1	+0.00 dBFS	+0.00 dBFS	997	None	n/a	n/a	n/a	Vrms	Level	+3.57	+3.63	+3.28	100k	<10 - >500k	None	1-6	13-18	n/a	n/a	External	48000	Digital
DIG_MAIN_OPT1_IN_48K_TO_ANLG_MAIN_OUT_THD	1	-10.00 dBFS	-10.00 dBFS	20-20k	None	n/a	n/a	n/a	%	THD+N	<.002	.005	.0002	100k	<10 - 22k	None	1-6	13-18	n/a	n/a	External	48000	Digital
DIG_MAIN_OPT1_IN_48K_TO_ANLG_MAIN_OUT_DYNRNG	1	-61.20 dBFS	-61.20 dBFS	997	None	n/a	n/a	n/a	dBr	THD+N	>-109.00	-105.00	-1000.00	100k	<10 - 22k	None	1-6	13-18	n/a	n/a	External	48000	Digital
DIG_MAIN_OPT1_IN_44K_TO_ANLG_MAIN_OUT																							
DIG_MAIN_OPT1_IN_44K_TO_ANLG_MAIN_OUT_GAIN	1	+0.00 dBFS	+0.00 dBFS	997	None	n/a	n/a	n/a	Vrms	Level	+3.57	+3.63	+3.28	100k	<10 - >500k	None	1-6	13-18	n/a	n/a	External	44100	Digital
DIG_MAIN_OPT1_IN_44K_TO_ANLG_MAIN_OUT_THD	1	-10.00 dBFS	-10.00 dBFS	20-20k	None	n/a	n/a	n/a	%	THD+N	<.002	.005	.0002	100k	<10 - 22k	None	1-6	13-18	n/a	n/a	External	44100	Digital
DIG_MAIN_OPT1_IN_44K_TO_ANLG_MAIN_OUT_DYNRNG	1	-61.20 dBFS	-61.20 dBFS	997	None	n/a	n/a	n/a	dBr	THD+N	>-109.00	-105.00	-1000.00	100k	<10 - 22k	None	1-6	13-18	n/a	n/a	External	44100	Digital
DIG_MAIN_OPT1_IN_44K_TO_ANLG_MAIN_OUT_CLKRNG	1	-10.00 dBFS	-10.00 dBFS	997	None	n/a	n/a	n/a	%	THD+N	>-96.00	-86.00	-130.00	100k	<10 - 22k	None	1	n/a	n/a	n/a	External	43650-44550	Digital

A-A Tests		Analog Generator							Analog Analyzer								Switcher Module						
Test Name	See Note:	Left	Right	Freq (Hz)	EQ Curve	Z-out	Bal/ Unbal	Gnd/ Float	Level	Measure	Typical Reading	Upper Limit	Lower Limit	Imp.	Bandwidth	Filter	A In	B In	A Out	B Out	Clock Source	Sample Rate	Audio Source
ANLG_ZONE2_IN1_TO_ANLG_ZONE2_DIR_VAR_OUT																							
ANLG_ZONE2_IN1_TO_ANLG_ZONE2_DIR_VAR_OUT_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	Vrms	Level	+3.80	+4.17	+3.40	100k	<10 - >500k	None	7	19	1	13	Internal	n/a	Analog
ANLG_ZONE2_IN1_TO_ANLG_ZONE2_DIR_VAR_OUT_FREQ	1	2.00 Vrms	2.00 Vrms	10-20k/20k-40k	None	20	Unbal	Float	dBr	Level	<-0.10	+0.10	-0.25/-0.75	100k	<10 - >500k	None	7	19	1	13	Internal	n/a	Analog
ANLG_ZONE2_IN1_TO_ANLG_ZONE2_DIR_VAR_OUT_THD	1	3.80 Vrms	3.80 Vrms	20-1k/5-40k	None	20	Unbal	Float	%	THD+N	<.003	.005	.00005	100k	<10 - >22k	None	7	19	1	13	Internal	n/a	Analog
ANLG_ZONE2_IN1_TO_ANLG_ZONE2_DIR_VAR_OUT_XTALK	1	4.00 Vrms	4.00 Vrms	15k	None	20	Unbal	Float	dB	Level	>-85.00	-75.00	-150.00	100k	<10 - >22k	None	7	19	1	13	Internal	n/a	Analog
ANLG_ZONE2_IN1_TO_ANLG_ZONE2_DIR_VAR_OUT_SNR	1	OFF	OFF	997	None	20	Unbal	Float	dBr	Level	<-110.00	-105.00	-140.00	100k	<10 - >22k	None	7	19	1	13	Internal	n/a	Analog
ANLG_ZONE2_IN1_TO_ANLG_ZONE2_DIR_VAR_OUT_VC_MUTE																							
ANLG_ZONE2_IN1_TO_ANLG_ZONE2_DIR_VAR_OUT_VC_MUTE	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	Vrms	Level	>-115.00	-108.00	1001.00	100k	<10 - 22k	None	7	19	1	13	Internal	n/a	Analog
ANLG_ZONE2_IN1_TO_ANLG_ZONE2_DIR_VAR_OUT_RELAY_MUTE																							
ANLG_ZONE2_IN1_TO_ANLG_ZONE2_DIR_VAR_OUT_RELAY_MUTE	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	Vrms	Level	>-115.00	-108.00	1001.00	100k	<10 - 22k	None	7	19	1	13	Internal	n/a	Analog
ANLG_ZONE2_IN1_TO_ANLG_ZONE2_DIR_FIX_OUT																							
ANLG_ZONE2_IN1_TO_ANLG_ZONE2_DIR_FIX_OUT_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	Vrms	Level	+3.80	+4.17	+3.40	100k	<10 - >500k	None	6	18	1	13	Internal	n/a	Analog
ANLG_ZONE2_IN1_TO_ANLG_ZONE2_DIR_FIX_OUT_RELAY_MUTE																							
ANLG_ZONE2_IN1_TO_ANLG_ZONE2_DIR_FIX_OUT_RELAY_MUTE	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	Vrms	Level	>-115.00	-108.00	1001.00	100k	<10 - 22k	None	6	18	1	13	Internal	n/a	Analog
ANLG_ZONE2_PHONO_IN_TO_ANLG_ZONE2_DIR_FIX_OUT																							
ANLG_ZONE2_PHONO_IN_TO_ANLG_ZONE2_DIR_FIX_OUT_GAIN	1	4.70 mVrms	4.70 mVrms	997	None	20	Unbal	Float	Vrms	Level	+.260	+.300	+.220	100k	<10 - >500k	None	6	18	11	23	Internal	n/a	Analog
ANLG_ZONE2_PHONO_IN_TO_ANLG_ZONE2_DIR_FIX_OUT_FREQ	1	16.00 mVrms	16.00 mVrms	20-50/50-20k	RIAA-PRE	20	Unbal	Float	dBr	Level	<-0.10	-0.50/+0.50	-1.50/-0.50	100k	<10 - >500k	None	6	18	11	23	Internal	n/a	Analog
ANLG_ZONE2_PHONO_IN_TO_ANLG_ZONE2_DIR_FIX_OUT_THD	1	4.70 mVrms	4.70 mVrms	20-20k	RIAA-PRE	20	Unbal	Float	%	THD+N	<.015	.020	.001	100k	100 - >22k	None	6	18	11	23	Internal	n/a	Analog
ANLG_ZONE2_PHONO_IN_TO_ANLG_ZONE2_DIR_FIX_OUT_XTALK	1	16.00 mVrms	16.00 mVrms	15k	RIAA-PRE	20	Unbal	Float	dB	Level	>-80.00	-70.00	-150.00	100k	<10 - >22k	None	6	18	11	23	Internal	n/a	Analog
ANLG_ZONE2_PHONO_IN_TO_ANLG_ZONE2_DIR_FIX_OUT_SNR	1	4.70 mVrms	4.70 mVrms	997	None	20	Unbal	Float	dBr	Level	>-76.00	-72.00	-140.00	100k	100 - >500k	None	6	18	11	23	Internal	n/a	Analog
ANLG_ZONE3_IN1_TO_ANLG_ZONE3_DIR_VAR_OUT																							
ANLG_ZONE3_IN1_TO_ANLG_ZONE3_DIR_VAR_OUT_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	Vrms	Level	+3.80	+4.17	+3.40	100k	<10 - >500k	None	5	17	1	13	Internal	n/a	Analog
ANLG_ZONE3_IN1_TO_ANLG_ZONE3_DIR_VAR_OUT_FREQ	1	2.00 Vrms	2.00 Vrms	10-20k/20k-40k	None	20	Unbal	Float	dBr	Level	<-0.10	+0.10	-0.25/-0.75	100k	<10 - >500k	None	5	17	1	13	Internal	n/a	Analog
ANLG_ZONE3_IN1_TO_ANLG_ZONE3_DIR_VAR_OUT_THD	1	3.80 Vrms	3.80 Vrms	20-1k/5-40k	None	20	Unbal	Float	%	THD+N	<.003	.005	.00005	100k	<10 - >22k	None	5	17	1	13	Internal	n/a	Analog
ANLG_ZONE3_IN1_TO_ANLG_ZONE3_DIR_VAR_OUT_XTALK	1	4.00 Vrms	4.00 Vrms	15k	None	20	Unbal	Float	dB	Level	>-95.00	-75.00	-150.00	100k	<10 - >22k	None	5	17	1	13	Internal	n/a	Analog
ANLG_ZONE3_IN1_TO_ANLG_ZONE3_DIR_VAR_OUT_SNR	1	OFF	OFF	997	None	20	Unbal	Float	dBr	Level	<-110.00	-105.00	-140.00	100k	<10 - >22k	None	5	17	1	13	Internal	n/a	Analog
ANLG_ZONE3_IN2_TO_ANLG_ZONE3_DIR_VAR_OUT																							
ANLG_ZONE3_IN2_TO_ANLG_ZONE3_DIR_VAR_OUT_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	Vrms	Level	+3.80	+4.17	+3.40	100k	<10 - >500k	None	5	17	2	14	Internal	n/a	Analog
ANLG_ZONE3_IN2_TO_ANLG_ZONE3_DIR_VAR_OUT_FREQ	1	2.00 Vrms	2.00 Vrms	10-20k/20k-40k	None	20	Unbal	Float	dBr	Level	<-0.10	+0.10	-0.25/-0.75	100k	<10 - >500k	None	5	17	2	14	Internal	n/a	Analog
ANLG_ZONE3_IN2_TO_ANLG_ZONE3_DIR_VAR_OUT_THD	1	3.80 Vrms	3.80 Vrms	20-1k/5-40k	None	20	Unbal	Float	%	THD+N	<.003	.005	.00005	100k	<10 - >22k	None	5	17	2	14	Internal	n/a	Analog
ANLG_ZONE3_IN2_TO_ANLG_ZONE3_DIR_VAR_OUT_XTALK	1	4.00 Vrms	4.00 Vrms	15k	None	20	Unbal	Float	dB	Level	>-95.00	-75.00	-150.00	100k	<10 - >22k	None	5	17	2	14	Internal	n/a	Analog
ANLG_ZONE3_IN2_TO_ANLG_ZONE3_DIR_VAR_OUT_SNR	1	OFF	OFF	997	None	20	Unbal	Float	dBr	Level	<-110.00	-105.00	-140.00	100k	<10 - >22k	None	5	17	2	14	Internal	n/a	Analog
ANLG_ZONE3_IN3_TO_ANLG_ZONE3_DIR_VAR_OUT																							
ANLG_ZONE3_IN3_TO_ANLG_ZONE3_DIR_VAR_OUT_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	Vrms	Level	+3.80	+4.17	+3.40	100k	<10 - >500k	None	5	17	3	14	Internal	n/a	Analog
ANLG_ZONE3_IN3_TO_ANLG_ZONE3_DIR_VAR_OUT_FREQ	1	2.00 Vrms	2.00 Vrms	10-20k/20k-40k	None	20	Unbal	Float	dBr	Level	<-0.10	+0.10	-0.25/-0.75	100k	<10 - >500k	None	5	17	3	14	Internal	n/a	Analog
ANLG_ZONE3_IN3_TO_ANLG_ZONE3_DIR_VAR_OUT_THD	1	3.80 Vrms	3.80 Vrms	20-1k/5-40k	None	20	Unbal	Float	%	THD+N	<.003	.005	.00005	100k	<10 - >22k	None	5	17	3	14	Internal	n/a	Analog
ANLG_ZONE3_IN3_TO_ANLG_ZONE3_DIR_VAR_OUT_XTALK	1	4.00 Vrms	4.00 Vrms	15k	None	20	Unbal	Float	dB	Level	>-95.00	-75.00	-150.00	100k	<10 - >22k	None	5	17	3	14	Internal	n/a	Analog
ANLG_ZONE3_IN3_TO_ANLG_ZONE3_DIR_VAR_OUT_SNR	1	OFF	OFF	997	None	20	Unbal	Float	dBr	Level	<-110.00	-105.00	-140.00	100k	<10 - >22k	None	5	17	3	14	Internal	n/a	Analog
ANLG_ZONE3_IN4_TO_ANLG_ZONE3_DIR_VAR_OUT																							
ANLG_ZONE3_IN4_TO_ANLG_ZONE3_DIR_VAR_OUT_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	Vrms	Level	+3.80	+4.17	+3.40	100k	<10 - >500k	None	5	17	4	16	Internal	n/a	Analog
ANLG_ZONE3_IN4_TO_ANLG_ZONE3_DIR_VAR_OUT_FREQ	1	2.00 Vrms	2.00 Vrms	10-20k/20k-40k	None	20	Unbal	Float	dBr	Level	<-0.10	+0.10	-0.25/-0.75	100k	<10 - >500k	None	5	17	4	16	Internal	n/a	Analog
ANLG_ZONE3_IN4_TO_ANLG_ZONE3_DIR_VAR_OUT_THD	1	3.80 Vrms	3.80 Vrms	20-1k/5-40k	None	20	Unbal	Float	%	THD+N	<.003	.005	.00005	100k	<10 - >22k	None	5	17	4	16	Internal	n/a	Analog
ANLG_ZONE3_IN4_TO_ANLG_ZONE3_DIR_VAR_OUT_XTALK	1	4.00 Vrms	4.00 Vrms	15k	None	20	Unbal	Float	dB	Level	>-95.00	-75.00	-150.00	100k	<10 - >22k	None	5	17	4	16	Internal	n/a	Analog
ANLG_ZONE3_IN4_TO_ANLG_ZONE3_DIR_VAR_OUT_SNR	1	OFF	OFF	997	None	20	Unbal	Float	dBr	Level	<-110.00	-105.00	-140.00	100k	<10 - >22k	None	5	17	4	16	Internal	n/a	Analog
ANLG_ZONE3_IN5_TO_ANLG_ZONE3_DIR_VAR_OUT																							
ANLG_ZONE3_IN5_TO_ANLG_ZONE3_DIR_VAR_OUT_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	Vrms	Level	+3.80	+4.17	+3.40	100k	<10 - >500k	None	5	17	5	17	Internal	n/a	Analog
ANLG_ZONE3_IN5_TO_ANLG_ZONE3_DIR_VAR_OUT_FREQ	1	2.00 Vrms	2.00 Vrms	10-20k/20k-40k	None	20	Unbal	Float	dBr	Level	<-0.10	+0.10	-0.25/-0.75	100k	<10 - >500k	None	5	17	5	17	Internal	n/a	Analog
ANLG_ZONE3_IN5_TO_ANLG_ZONE3_DIR_VAR_OUT_THD	1	3.80 Vrms	3.80 Vrms	20-1k/5-40k	None	20	Unbal	Float	%	THD+N	<.003	.005	.00005	100k	<10 - >22k	None	5	17	5	17	Internal	n/a	Analog
ANLG_ZONE3_IN5_TO_ANLG_ZONE3_DIR_VAR_OUT_XTALK	1	4.00 Vrms	4.00 Vrms	15k	None	20	Unbal	Float	dB	Level	>-95.00	-75.00	-150.00	100k	<10 - >22k	None	5	17	5	17	Internal	n/a	Analog
ANLG_ZONE3_IN5_TO_ANLG_ZONE3_DIR_VAR_OUT_SNR	1	OFF	OFF	997	None	20	Unbal	Float	dBr	Level	<-110.00	-105.00	-140.00	100k	<10 - >22k	None	5	17	5	17	Internal	n/a	Analog
ANLG_ZONE3_IN6_TO_ANLG_ZONE3_DIR_VAR_OUT																							
ANLG_ZONE3_IN6_TO_ANLG_ZONE3_DIR_VAR_OUT_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	Vrms	Level	+3.80	+4.17	+3.40	100k	<10 - >500k	None	5	17	6	18	Internal	n/a	Analog
ANLG_ZONE3_IN6_TO_ANLG_ZONE3_DIR_VAR_OUT_FREQ	1	2.00 Vrms	2.00 Vrms	10-20k/20k-40k	None	20	Unbal	Float	dBr	Level	<-0.10	+0.10	-0.25/-0.75	100k	<10 - >500k	None	5	17	6	18	Internal	n/a	Analog
ANLG_ZONE3_IN6_TO_ANLG_ZONE3_DIR_VAR_OUT_THD	1	3.80 Vrms	3.80 Vrms	20-1k/5-40k	None	20	Unbal	Float	%	THD+N	<.003	.005	.00005	100k	<10 - >22k	None	5	17	6	18	Internal	n/a	Analog
ANLG_ZONE3_IN6_TO_ANLG_ZONE3_DIR_VAR_OUT_XTALK	1	4.00 Vrms	4.00 Vrms	15k	None	20	Unbal	Float	dB	Level	>-95.00	-75.00	-150.00	100k	<10 - >22k	None	5	17	6	18	Internal	n/a	Analog
ANLG_ZONE3_IN6_TO_ANLG_ZONE3_DIR_VAR_OUT_SNR	1	OFF	OFF	997	None	20	Unbal	Float	dBr	Level	<-110.00	-105.00	-140.00	100k	<10 - >22k	None	5	17	6	18	Internal	n/a	Analog
ANLG_ZONE3_IN7_TO_ANLG_ZONE3_DIR_VAR_OUT																							
ANLG_ZONE3_IN7_TO_ANLG_ZONE3_DIR_VAR_OUT_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	Vrms	Level	+3.80	+4.17	+3.40	100k	<10 - >500k	None	5	17	7	19	Internal	n/a	Analog
ANLG_ZONE3_IN7_TO_ANLG_ZONE3_DIR_VAR_OUT_FREQ	1	2.00 Vrms	2.00 Vrms	10-20k/20k-40k	None	20	Unbal	Float	dBr	Level	<-0.10	+0.10	-0.25/-0.75	100k	<10 - >500k	None	5	17	7	19	Internal	n/a	Analog
ANLG_ZONE3_IN7_TO_ANLG_ZONE3_DIR_VAR_OUT_THD	1	3.80 Vrms	3.80 Vrms	20-1k/5-40k	None	20	Unbal	Float	%	THD+N	<.003	.005	.00005	100k	<10 - >22k	None	5	17	7	19	Internal	n/a	Analog
ANLG_ZONE3_IN7_TO_ANLG_ZONE3_DIR_VAR_OUT_XTALK	1	4.00 Vrms	4.00 Vrms	15k	None	20	Unbal	Float	dB	Level	>-95.00	-75.00	-150.00	100k	<10 - >22k	None	5	17	7	19	Internal	n/a	Analog
ANLG_ZONE3_IN7_TO_ANLG_ZONE3_DIR_VAR_OUT_SNR	1	OFF	OFF	997	None	20	Unbal	Float	dBr	Level	<-110.00	-105.00	-140.00	100k	<10 - >22k	None	5	17	7	19	Internal	n/a	Analog
ANLG_ZONE3_IN8_TO_ANLG_ZONE3_DIR_VAR_OUT																							
ANLG_ZONE3_IN8_TO_ANLG_ZONE3_DIR_VAR_OUT_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	Vrms	Level	+3.80	+4.17	+3.40	100k	<10 - >500k	None	5	17	8	20	Internal	n/a	Analog
ANLG_ZONE3_IN8_TO_ANLG_ZONE3_DIR_VAR_OUT_FREQ	1	2.00 Vrms	2.00 Vrms	10-20k/20k-40k	None	20	Unbal	Float	dBr	Level	<-0.10	+0.10	-0.25/-0.75	100k	<10 - >500k	None	5	17	8	20	Internal	n/a	Analog
ANLG_ZONE3_IN8_TO_ANLG_ZONE3_DIR_VAR_OUT_THD	1	3.80 Vrms	3.80 Vrms	20-1k/5-40k	None	20	Unbal	Float	%	THD+N	<.003	.005	.00005	100k	<10 - >22k	None	5	17	8	20	Internal	n/a	Analog
ANLG_ZONE3_IN8_TO_ANLG_ZONE3_DIR_VAR_OUT_XTALK	1	4.00 Vrms	4.00 Vrms	15k	None	20	Unbal	Float	dB	Level	>-95.00	-75.00	-150.00	100k	<10 - >22k	None	5	17	8	20	Internal	n/a	Analog
ANLG_ZONE3_IN8_TO_ANLG_ZONE3_DIR_VAR_OUT_SNR	1	OFF	OFF	997	None	20	Unbal	Float	dBr	Level	<-110.00	-105.00	-140.00	100k	<10 - >22k	None	5	17	8	20	Internal	n/a	Analog
ANLG_ZONE3_IN1_TO_ANLG_ZONE3_DIR_VAR_OUT_VC_MUTE																							
ANLG_ZONE3_IN1_TO_ANLG_ZONE3_DIR_VAR_OUT_VC_MUTE	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	Vrms	Level	>-110.00	-108.00	1001.00	100k	<10 - 22k	None	5	17	1	13	Internal	n/a	Analog
ANLG_ZONE3_IN1_TO_ANLG_ZONE3_DIR_VAR_OUT_RELAY_MUTE																							
ANLG_ZONE3_IN1_TO_ANLG_ZONE3_DIR_VAR_OUT_RELAY_MUTE	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	Vrms	Level	-115.00	-108.00	1001.00	100k	<10 - 22k	None	5	17	1	13	Internal	n/a	Analog
ANLG_ZONE3_PHONO_IN_TO_ANLG_ZONE3_DIR_VAR_OUT																							
ANLG_ZONE3_PHONO_IN_TO_ANLG_ZONE3_DIR_VAR_OUT_GAIN	1	4.70 mVrms	4.70 mVrms	997	None	20	Unbal	Float	Vrms	Level	+0.260	+0.300	+0.220	100k	<10 - >500k	None	5	17	11	23	Internal	n/a	Analog
ANLG_ZONE3_PHONO_IN_TO_ANLG_ZONE3_DIR_VAR_OUT_FREQ	1	16.00 mVrms	16.00 mVrms	20-50/50-20k	RIAA-PRE	20	Unbal	Float	dBr	Level	<-0.10	-0.50/+0.50	-1.50/-0.50	100k	<10 - >500k	None	5	17	11	23	Internal	n/a	Analog
ANLG_ZONE3_PHONO_IN_TO_ANLG_ZONE3_DIR_VAR_OUT_THD	1	4.70 mVrms	4.70 mVrms	20-20k	RIAA-PRE	20	Unbal	Float	%	THD+N	<.015	.020	.001	100k	100 - >22k	None	5	17	11	23	Internal	n/a	Analog
ANLG_ZONE3_PHONO_IN_TO_ANLG_ZONE3_DIR_VAR_OUT_XTALK	1	16.00 mVrms	16.00 mVrms	15k	RIAA-PRE	20	Unbal	Float	dB	Level	>-80.00	-70.00	-150.00	100k	<10 - >22k	None	5	17	11	23	Internal	n/a	Analog
ANLG_ZONE3_PHONO_IN_TO_ANLG_ZONE3_DIR_VAR_OUT_SNR	1	OFF	OFF	997	None	20	Unbal	Float	dBr	Level	>-76.00	-72.00	-140.00	100k	100 - >500k	None	5	17	11	23	Internal	n/a	Analog
ANLG_FRONT_IN1_TO_ANLG_MAIN_OUT																							
ANLG_FRONT_IN1_TO_ANLG_MAIN_OUT_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	Vrms	Level	+3.40	+3.70	+3.10	100k	<10 - >500k	None	1-4	13-16	1	13	Internal	n/a	Analog
ANLG_FRONT_IN1_TO_ANLG_MAIN_OUT_FREQ	1	2.00 Vrms	2.00 Vrms	10-20/20-20k/20k-40k	None	20	Unbal	Float	dBr	Level	<-0.05/0.0/-0.25	+0.10	-0.8/-0.25/-0.8	100k	<10 - >500k	None	1-4	13-16	1	13	Internal	n/a	Analog
ANLG_FRONT_IN1_TO_ANLG_MAIN_OUT_THD	1	2.00 Vrms	2.00 Vrms	20-40k	None	20	Unbal	Float	%	THD+N	<.004	.009	.00005	100k	<10 - >22k	None	1-4	13-16	1	13	Internal	n/a	Analog
ANLG_FRONT_IN1_TO_ANLG_MAIN_OUT_XTALK	1	4.00 Vrms	4.00 Vrms	15k	None	20	Unbal	Float	dB	Level	>-85.00	-75.00	-150.00	100k	<10 - >22k	None	1-4	13-16	1	13	Internal	n/a	Analog
ANLG_FRONT_IN1_TO_ANLG_MAIN_OUT_SNR	1	OFF	OFF	997	None	20	Unbal	Float	dBr	Level	-106.00	-102.00	-140.00	100k	<10 - >22k	None	1-4	13-16	1	13	Internal	n/a	Analog
ANLG_FRONT_IN1_TO_ANLG_MAIN_OUT_VC_MUTE																							
ANLG_FRONT_IN1_TO_ANLG_MAIN_OUT_VC_MUTE	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	Vrms	Level	>-34.00	-30.00	-45.00	100k	<10 - 22k	None	1-4	13-16	1	13	Internal	n/a	Analog
ANLG_FRONT_IN1_TO_ANLG_MAIN_OUT_RELAY_MUTE																							
ANLG_FRONT_IN1_TO_ANLG_MAIN_OUT_RELAY_MUTE	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	Vrms	Level	-108.00	-102.00	1001.00	100k	<10 - 22k	None	1-4	13-16	1	13	Internal	n/a	Analog

A-A Tests		Analog Generator							Analog Analyzer								Switcher Module						
Test Name	See Note:	Left	Right	Freq (Hz)	EQ Curve	Z-out	Bal/ Unbal	Gnd/ Float	Level	Measure	Typical Reading	Upper Limit	Lower Limit	Imp.	Bandwidth	Filter	A In	B In	A Out	B Out	Clock Source	Sample Rate	Audio Source
ANLG_MAIN_IN345_TO_ANLG_MAIN_DIR_OUT																							
ANLG_MAIN_IN345_TO_ANLG_MAIN_DIR_OUT_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	Vrms	Level	+3.50	+3.68	+3.32	100k	<10 - >500k	None	1,2,3,4	13,14,15,16	3,4,5,5	13,14,15,15	Internal	n/a	Analog
ANLG_MAIN_IN345_TO_ANLG_MAIN_DIR_OUT_FREQ	1	2.00 Vrms	2.00 Vrms	10-20/20-20k/20k-40k	None	20	Unbal	Float	dBr	Level	<-0.05/0.0/-0.25	+0.10	-0.8/-0.25/-0.8	100k	<10 - >500k	None	1,2,3,4	13,14,15,16	3,4,5,5	13,14,15,15	Internal	n/a	Analog
ANLG_MAIN_IN345_TO_ANLG_MAIN_DIR_OUT_THD	1	3.80 Vrms	3.80 Vrms	20-40k	None	20	Unbal	Float	%	THD+N	<.006	.009	.00005	100k	<10 - >500k	40kHz LP	1,2,3,4	13,14,15,16	3,4,5,5	13,14,15,15	Internal	n/a	Analog
ANLG_MAIN_IN345_TO_ANLG_MAIN_DIR_OUT_SNR	1	OFF	OFF	997	None	20	Unbal	Float	dBr	Level	>-108.00	-105.00	-140.00	100k	<10 - >22k	None	1,2,3,4	13,14,15,16	3,4,5,5	13,14,15,15	Internal	n/a	Analog
ANLG_MAIN_IN678_TO_ANLG_MAIN_DIR_OUT																							
ANLG_MAIN_IN678_TO_ANLG_MAIN_DIR_OUT_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	Vrms	Level	+3.50	+3.68	+3.32	100k	<10 - >500k	None	1,2,3,4	13,14,15,16	6,7,8,8	19,20,21,21	Internal	n/a	Analog
ANLG_MAIN_IN678_TO_ANLG_MAIN_DIR_OUT_FREQ	1	2.00 Vrms	2.00 Vrms	10-20/20-20k/20k-40k	None	20	Unbal	Float	dBr	Level	<-0.05/0.0/-0.25	+0.10	-0.8/-0.25/-0.8	100k	<10 - >500k	None	1,2,3,4	13,14,15,16	6,7,8,8	19,20,21,21	Internal	n/a	Analog
ANLG_MAIN_IN678_TO_ANLG_MAIN_DIR_OUT_THD	1	3.80 Vrms	3.80 Vrms	20-40k	None	20	Unbal	Float	%	THD+N	<.006	.009	.00005	100k	<10 - >500k	40kHz LP	1,2,3,4	13,14,15,16	6,7,8,8	19,20,21,21	Internal	n/a	Analog
ANLG_MAIN_IN678_TO_ANLG_MAIN_DIR_OUT_SNR	1	OFF	OFF	997	None	20	Unbal	Float	dBr	Level	>-108.00	-105.00	-140.00	100k	<10 - >22k	None	1,2,3,4	13,14,15,16	6,7,8,8	19,20,21,21	Internal	n/a	Analog
ANLG_FRONT_PHONO_IN_TO_ANLG_FRONT_DIR_OUT																							
ANLG_FRONT_PHONO_IN_TO_ANLG_FRONT_DIR_OUT_GAIN	1	4.70 mVrms	4.70 mVrms	997	None	20	Unbal	Float	Vrms	Level	+0.442	+0.465	+0.420	100k	<10 - >500k	None	1	13	11	23	Internal	n/a	Analog
ANLG_FRONT_PHONO_IN_TO_ANLG_FRONT_DIR_OUT_FREQ	1	16.00 mVrms	16.00 mVrms	20-50/50-20k	RIAA-PRE	20	Unbal	Float	dBr	Level	<-0.10	-0.50/+0.50	-1.50/-0.50	100k	<10 - >500k	None	1	13	11	23	Internal	n/a	Analog
ANLG_FRONT_PHONO_IN_TO_ANLG_FRONT_DIR_OUT_THD	1	4.70 mVrms	4.70 mVrms	20-20k	RIAA-PRE	20	Unbal	Float	%	THD+N	<..015	.020	.001	100k	100 - >22k	None	1	13	11	23	Internal	n/a	Analog
ANLG_FRONT_PHONO_IN_TO_ANLG_FRONT_DIR_OUT_XTALK	1	16.00 mVrms	16.00 mVrms	15k	RIAA-PRE	20	Unbal	Float	dB	Level	>-80.00	-70.00	-150.00	100k	<10 - >22k	None	1	13	11	23	Internal	n/a	Analog
ANLG_FRONT_PHONO_IN_TO_ANLG_FRONT_DIR_OUT_SNR	1	OFF	OFF	997	None	20	Unbal	Float	dBr	Level	>-76.00	-72.00	-140.00	100k	100 - >500k	None	1	13	11	23	Internal	n/a	Analog
ANLG_FRONT_IN3_TO_ANLG_FRONT_HEADPHONE_OUT																							
ANLG_FRONT_IN3_TO_ANLG_FRONT_HEADPHONE_OUT_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	Vrms	Level	+4.00	+4.20	+3.80	600	<10 - >500k	None	11	23	3	15	Internal	n/a	Analog
ANLG_FRONT_IN3_TO_ANLG_FRONT_HEADPHONE_OUT_FREQ	1	2.00 Vrms	2.00 Vrms	10-20/20-20k/20k-40k	None	20	Unbal	Float	dBr	Level	<-0.35/0.0/-0.40	+0.10	-0.8/-0.25/-0.8	600	<10 - >500k	None	11	23	3	15	Internal	n/a	Analog
ANLG_FRONT_IN3_TO_ANLG_FRONT_HEADPHONE_OUT_THD	1	3.80 Vrms	3.80 Vrms	20-40k	None	20	Unbal	Float	%	THD+N	<.005	.009	.00005	600	<10 - >500k	40kHz LP	11	23	3	15	Internal	n/a	Analog
ANLG_FRONT_IN3_TO_ANLG_FRONT_HEADPHONE_OUT_XTALK	1	4.00 Vrms	4.00 Vrms	15k	None	20	Unbal	Float	dB	Level	>-73.00	-70.00	-150.00	600	<10 - >22k	None	11	23	3	15	Internal	n/a	Analog
ANLG_FRONT_IN3_TO_ANLG_FRONT_HEADPHONE_OUT_SNR	1	OFF	OFF	997	None	20	Unbal	Float	dBr	Level	-112.00	-102.00	-140.00	600	<10 - >22k	None	11	23	3	15	Internal	n/a	Analog
ANLG_ZONE2_IN1_TO_ANLG_ZONE2_HEADPHONE_OUT																							
ANLG_ZONE2_IN1_TO_ANLG_ZONE2_HEADPHONE_OUT_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	Vrms	Level	+4.36	+4.60	+4.14	600	<10 - >500k	None	11	23	1	13	Internal	n/a	Analog
ANLG_ZONE2_IN1_TO_ANLG_ZONE2_HEADPHONE_OUT_FREQ	1	2.00 Vrms	2.00 Vrms	10-20/20-20k/20k-40k	None	20	Unbal	Float	dBr	Level	<-0.45/0.0/-0.40	+0.10	-0.8/-0.25/-0.8	600	<10 - >500k	None	11	23	1	13	Internal	n/a	Analog
ANLG_ZONE2_IN1_TO_ANLG_ZONE2_HEADPHONE_OUT_THD	1	3.80 Vrms	3.80 Vrms	20-40k	None	20	Unbal	Float	%	THD+N	<.002	.009	.00005	600	<10 - >500k	40kHz LP	11	23	1	13	Internal	n/a	Analog
ANLG_ZONE2_IN1_TO_ANLG_ZONE2_HEADPHONE_OUT_XTALK	1	4.00 Vrms	4.00 Vrms	15k	None	20	Unbal	Float	dB	Level	>-73.00	-70.00	-150.00	600	<10 - >22k	None	11	23	1	13	Internal	n/a	Analog
ANLG_ZONE2_IN1_TO_ANLG_ZONE2_HEADPHONE_OUT_SNR	1	OFF	OFF	997	None	20	Unbal	Float	dBr	Level	-112.00	-102.00	-140.00	600	<10 - >22k	None	11	23	1	13	Internal	n/a	Analog
ANLG_ZONE3_IN1_TO_ANLG_ZONE3_HEADPHONE_OUT																							
ANLG_ZONE3_IN1_TO_ANLG_ZONE3_HEADPHONE_OUT_GAIN	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	Vrms	Level	+4.36	+4.60	+4.14	600	<10 - >500k	None	11	23	3	15	Internal	n/a	Analog
ANLG_ZONE3_IN1_TO_ANLG_ZONE3_HEADPHONE_OUT_FREQ	1	2.00 Vrms	2.00 Vrms	10-20/20-20k/20k-40k	None	20	Unbal	Float	dBr	Level	<-0.45/0.0/-0.40	+0.10	-0.8/-0.25/-0.8	600	<10 - >500k	None	11	23	3	15	Internal	n/a	Analog
ANLG_ZONE3_IN1_TO_ANLG_ZONE3_HEADPHONE_OUT_THD	1	3.80 Vrms	3.80 Vrms	20-40k	None	20	Unbal	Float	%	THD+N	<.002	.009	.00005	600	<10 - >500k	40kHz LP	11	23	3	15	Internal	n/a	Analog
ANLG_ZONE3_IN1_TO_ANLG_ZONE3_HEADPHONE_OUT_XTALK	1	4.00 Vrms	4.00 Vrms	15k	None	20	Unbal	Float	dB	Level	>-73.00	-70.00	-150.00	600	<10 - >22k	None	11	23	3	15	Internal	n/a	Analog
ANLG_ZONE3_IN1_TO_ANLG_ZONE3_HEADPHONE_OUT_SNR	1	OFF	OFF	997	None	20	Unbal	Float	dBr	Level	-112.00	-102.00	-140.00	600	<10 - >22k	None	11	23	3	15	Internal	n/a	Analog
ANLG_ZONE3_IN1_TO_ANLG_ZONE3_HEADPHONE_OUT_RELAY_MUTE																							
ANLG_ZONE3_IN1_TO_ANLG_ZONE3_HEADPHONE_OUT_RELAY_MUTE	1	4.00 Vrms	4.00 Vrms	997	None	20	Unbal	Float	Vrms	Level	-115.00	-105.00	1001.00	600	<10 - 22k	None	11	23	3	15	Internal	n/a	Analog

A-A FM Tuner Tests		Analog Generator							Analog Analyzer								Switcher Module						
Test Name	See Note:	Left	Right	Freq (Hz)	EQ Curve	Z-out	Bal/ Unbal	Gnd/ Float	Level	Measure	Typical Reading	Upper Limit	Lower Limit	Imp.	Bandwidth	Filter	A In	B In	A Out	B Out	Clock Source	Sample Rate	Audio Source
ANLG_ZONE2_TUNER_FM98_TO_ANLG_ZONE2_DIR_HEADPHONE_OUT																							
ANLG_ZONE2_TUNER_FM98_TO_ANLG_ZONE2_DIR_HEADPHONE_OUT_GAIN	1	150 mVrms	150 mVrms	997	None	25	Unbal	Float	Vrms	Level	+1.73	+1.94	+1.52	100k	<10 - >500k	None	11	23	12	24	Internal	n/a	Analog
ANLG_ZONE2_TUNER_FM98_TO_ANLG_ZONE2_DIR_HEADPHONE_OUT_FREQ	1	100 mVrms	100 mVrms	50-2k/2k-16k	75US-PRE	25	Unbal	Float	dBr	Level	0.00/-1.75	+0.50	0.50/-2.00	100k	<10 - >500k	None	11	23	12	24	Internal	n/a	Analog
ANLG_ZONE2_TUNER_FM98_TO_ANLG_ZONE2_DIR_HEADPHONE_OUT_THD	1	150 mVrms	150 mVrms	50-16k	75US-PRE	25	Unbal	Float	%	THD+N	>0.80	2.25	0.10	100k	<10 - >500k	None	11	23	12	24	Internal	n/a	Analog
ANLG_ZONE2_TUNER_FM98_TO_ANLG_ZONE2_DIR_HEADPHONE_OUT_SNR	1	OFF	OFF	997	None	25	Unbal	Float	dBr	Level	-55.00	-50.00	-60.00	100k	22 - >22k	A-Wtg	11	23	12	24	Internal	n/a	Analog
ANLG_ZONE3_TUNER_FM98_TO_ANLG_ZONE3_DIR_HEADPHONE_OUT																							
ANLG_ZONE3_TUNER_FM98_TO_ANLG_ZONE3_DIR_HEADPHONE_OUT_GAIN	1	150 mVrms	150 mVrms	997	None	25	Unbal	Float	Vrms	Level	+1.73	+1.94	+1.52	100k	<10 - >500k	None	11	23	12	24	Internal	n/a	Analog
ANLG_ZONE3_TUNER_FM98_TO_ANLG_ZONE3_DIR_HEADPHONE_OUT_FREQ	1	100 mVrms	100 mVrms	50-2k/2k-16k	None	25	Unbal	Float	dBr	Level	0.00/-1.75	+0.50	0.50/-2.00	100k	<10 - >500k	None	11	23	12	24	Internal	n/a	Analog
ANLG_ZONE3_TUNER_FM98_TO_ANLG_ZONE3_DIR_HEADPHONE_OUT_THD	1	150 mVrms	150 mVrms	50-16k	None	25	Unbal	Float	%	THD+N	>0.80	2.25	0.10	100k	<10 - >500k	None	11	23	12	24	Internal	n/a	Analog
ANLG_ZONE3_TUNER_FM98_TO_ANLG_ZONE3_DIR_HEADPHONE_OUT_SNR	1	OFF	OFF	997	None	25	Unbal	Float	dBr	Level	-55.00	-50.00	-60.00	100k	22 - >22k	A-Wtg	11	23	12	24	Internal	n/a	Analog
ANLG_FRONT_TUNER_FM98_TO_ANLG_FRONT_DIR_HEADPHONE_OUT																							
ANLG_FRONT_TUNER_FM98_TO_ANLG_FRONT_DIR_HEADPHONE_OUT_GAIN	1	150 mVrms		997	None	25	Unbal	Float	Vrms	Level	+1.55	+1.74	+1.36	100k	<10 - >500k	None	11	23	12	24	Internal	n/a	Analog
ANLG_FRONT_TUNER_FM98_TO_ANLG_FRONT_DIR_HEADPHONE_OUT_FREQ	1	100 mVrms	100 mVrms	50-2k/2k-16k	None	25	Unbal	Float	dBr	Level	0.00/-1.75	+0.50	0.50/-2.00	100k	<10 - >500k	None	11	23	12	24	Internal	n/a	Analog
ANLG_FRONT_TUNER_FM98_TO_ANLG_FRONT_DIR_HEADPHONE_OUT_THD	1	150 mVrms	150 mVrms	50-16k	None	25	Unbal	Float	%	THD+N	>0.80	2.25	0.10	100k	<10 - >500k	None	11	23	12	24	Internal	n/a	Analog
ANLG_FRONT_TUNER_FM98_TO_ANLG_FRONT_DIR_HEADPHONE_OUT_SNR	1	OFF	OFF	997	None	25	Unbal	Float	dBr	Level	-55.00	-50.00	-60.00	100k	22 - >22k	A-Wtg	11	23	12	24	Internal	n/a	Analog

A-A AM Tuner Tests		Analog Generator							Analog Analyzer								Switcher Module						
Test Name	See Note:	Left	Right	Freq (Hz)	EQ Curve	Z-out	Bal/ Unbal	Gnd/ Float	Level	Measure	Typical Reading	Upper Limit	Lower Limit	Imp.	Bandwidth	Filter	A In	B In	A Out	B Out	Clock Source	Sample Rate	Audio Source
ANLG_FRONT_TUNER_AM1050_TO_ANLG_FRONT_DIR_HEADPHONE_OUT																							
ANLG_FRONT_TUNER_AM1050_TO_ANLG_FRONT_DIR_HEADPHONE_OUT_GAIN	1	OFF	150 mVrms	997	None	25	Unbal	Float	Vrms	Level	+1.285	+1.35	+1.20	100k	<10 - >500k	None	11	23	12	24	Internal	n/a	Analog
ANLG_FRONT_TUNER_AM1050_TO_ANLG_FRONT_DIR_HEADPHONE_OUT_FREQ	1	150 mVrms	150 mVrms	50-1k/1k-2.3k/2/3k-5k	None	25	Unbal	Float	dBr	Level	0.0/-4.0/-25.0	+1.0/-2.0/-21.0	-1.5/-6.0/-35.0	100k	<10 - >500k	None	11	23	12	24	Internal	n/a	Analog
ANLG_FRONT_TUNER_AM1050_TO_ANLG_FRONT_DIR_HEADPHONE_OUT_THD	1	400 mVrms	400 mVrms	1k	None	25	Unbal	Float	%	THD+N	>0.46	3.16	0.10	100k	<10 - >500k	None	11	23	12	24	Internal	n/a	Analog

A-A Amplifier Tests		Analog Generator							Analog Analyzer								Switcher Module						
Test Name	See Note:	Left	Right	Freq (Hz)	EQ Curve	Z-out	Bal/ Unbal	Gnd/ Float	Level	Measure	Typical Reading	Upper Limit	Lower Limit	Imp.	Bandwidth	Filter	A In	B In	A Out	B Out	Clock Source	Sample Rate	Audio Source
ANLG_SIDE_IN5_TO_ANLG_REAR_DIR_AMP3&7_OUT																							
ANLG_SIDE_IN5_TO_ANLG_REAR_DIR_AMP3&7_OUT_GAIN	2	1.00 Vrms	1.00 Vrms	1k	None	25	Unbal	Float	Vrms	Level	+7.95	+8.35	+7.55	100k	<10 - >22k	None	7	3	5	6	Internal	n/a	Analog
ANLG_SIDE_IN5_TO_ANLG_REAR_DIR_AMP3&7_OUT_FREQ	2	1.00 Vrms	1.00 Vrms	10/20-20k/40k/100k	None	25	Unbal	Float	dBr	Level	-.03/0/-.02/-2.5	+0.10	-.5/-.2/-.5/-3.0	100k	<10 - >500k	None	7	3	5	6	Internal	n/a	Analog
ANLG_SIDE_IN5_TO_ANLG_REAR_DIR_AMP3&7_OUT_THD	2	1.00 Vrms	1.00 Vrms	20 - 20k	None	25	Unbal	Float	%	THD+N	< 0.0010	0.05	0.0001	100k	<10 - >22k	None	7	3	5	6	Internal	n/a	Analog
ANLG_SIDE_IN5_TO_ANLG_REAR_DIR_AMP3&7_OUT_XTALK	2	1.00 Vrms	1.00 Vrms	20 - 20k	None	25	Unbal	Float	dB	Level	<-65.00	-50.00	-150.00	100k	<10 - >22k	None	7	3	5	6	Internal	n/a	Analog
ANLG_SIDE_IN5_TO_ANLG_REAR_DIR_AMP3&7_OUT_SNR	2	OFF	OFF	997	None	25	Unbal	Float	dBr	Level	-107.00	-105.00	-140.00	100k	22 - >22k	A-Wtg	7	3	5	6	Internal	n/a	Analog
ANLG_ZONE2_IN5_TO_ANLG_ZONE2_DIR_AMP3&7_OUT																							
ANLG_ZONE2_IN5_TO_ANLG_ZONE2_DIR_AMP3&7_OUT_GAIN	2	1.00 Vrms	1.00 Vrms	1k	None	25	Unbal	Float	Vrms	Level	+7.95	+8.35	+7.55	100k	<10 - >22k	None	7	3	5	6	Internal	n/a	Analog
ANLG_ZONE2_IN5_TO_ANLG_ZONE2_DIR_AMP3&7_OUT_FREQ	2	1.00 Vrms	1.00 Vrms	10/20-20k/40k/100k	None	25	Unbal	Float	dBr	Level	-.03/0/-.02/-2.5	+0.10	-.5/-.2/-.5/-3.0	100k	<10 - >500k	None	7	3	5	6	Internal	n/a	Analog
ANLG_ZONE2_IN5_TO_ANLG_ZONE2_DIR_AMP3&7_OUT_THD	2	1.00 Vrms	1.00 Vrms	20 - 20k	None	25	Unbal	Float	%	THD+N	< 0.0010	0.05	0.0001	100k	<10 - >22k	None	7	3	5	6	Internal	n/a	Analog
ANLG_ZONE2_IN5_TO_ANLG_ZONE2_DIR_AMP3&7_OUT_XTALK	2	1.00 Vrms	1.00 Vrms	20 - 20k	None	25	Unbal	Float	dB	Level	<-65.00	-50.00	-150.00	100k	<10 - >22k	None	7	3	5	6	Internal	n/a	Analog
ANLG_ZONE2_IN5_TO_ANLG_ZONE2_DIR_AMP3&7_OUT_SNR	2	OFF	OFF	997	None	25	Unbal	Float	dBr	Level	-107.00	-105.00	-140.00	100k	22 - >22k	A-Wtg	7	3	5	6	Internal	n/a	Analog
ANLG_ZONE3_IN5_TO_ANLG_ZONE3_DIR_AMP3&7_OUT																							
ANLG_ZONE3_IN5_TO_ANLG_ZONE3_DIR_AMP3&7_OUT_GAIN	2	1.00 Vrms	1.00 Vrms	1k	None	25	Unbal	Float	Vrms	Level	+7.95	+8.35	+7.55	100k	<10 - >22k	None	7	3	5	6	Internal	n/a	Analog
ANLG_ZONE3_IN5_TO_ANLG_ZONE3_DIR_AMP3&7_OUT_FREQ	2	1.00 Vrms	1.00 Vrms	10/20-20k/40k/100k	None	25	Unbal	Float	dBr	Level	-.03/0/-.02/-2.5	+0.10	-.5/-.2/-.5/-3.0	100k	<10 - >500k	None	7	3	5	6	Internal	n/a	Analog
ANLG_ZONE3_IN5_TO_ANLG_ZONE3_DIR_AMP3&7_OUT_THD	2	1.00 Vrms	1.00 Vrms	20 - 20k	None	25	Unbal	Float	%	THD+N	< 0.0010	0.05	0.0001	100k	<10 - >22k	None	7	3	5	6	Internal	n/a	Analog
ANLG_ZONE3_IN5_TO_ANLG_ZONE3_DIR_AMP3&7_OUT_XTALK	2	1.00 Vrms	1.00 Vrms	20 - 20k	None	25	Unbal	Float	dB	Level	<-65.00	-50.00	-150.00	100k	<10 - >22k	None	7	3	5	6	Internal	n/a	Analog
ANLG_ZONE3_IN5_TO_ANLG_ZONE3_DIR_AMP3&7_OUT_SNR	2	OFF	OFF	997	None	25	Unbal	Float	dBr	Level	-107.00	-105.00	-140.00	100k	22 - >22k	A-Wtg	7	3	5	6	Internal	n/a	Analog
ANLG_MAIN_DIR_IN345_TO_ANLG_MAIN_AMP1-7_OUT																							
ANLG_MAIN_DIR_IN345_TO_ANLG_MAIN_AMP1-7_OUT_GAIN	2	1.00 Vrms	1.00 Vrms	1k	None	25	Unbal	Float	Vrms	Level	+7.95	+8.35	+7.55	100k	<10 - >22k	None	5,1,4,6,2,7,3	0	1,2,3,5,6,5,6	0	Internal	n/a	Analog
ANLG_MAIN_DIR_IN345_TO_ANLG_MAIN_AMP1-7_OUT_FREQ	2	1.00 Vrms	1.00 Vrms	10/20-20k/40k/100k	None	25	Unbal	Float	dBr	Level	-.03/0/-.02/-2.5	+0.10	-.5/-.2/-.5/-3.0	100k	<10 - >500k	None	5,1,4,6,2,7,3	0	1,2,3,5,6,5,6	0	Internal	n/a	Analog
ANLG_MAIN_DIR_IN345_TO_ANLG_MAIN_AMP1-7_OUT_SMPTE_IMD	2	1.00 Vrms	1.20 Vrms	7k / 60	None	25	Unbal	Float	%	SMPTE	0.0018	0.030	0.0001	100k	n/a	None	5,1,4,6,2,7,3	0	1,2,3,5,6,5,6	0	Internal	n/a	Analog
ANLG_MAIN_DIR_IN345_TO_ANLG_MAIN_ANLG_MAIN_AMP1-7_OUT_SNR	2	OFF	OFF	997	None	25	Unbal	Float	dBr	Level	-107.00	-105.00	-140.00	100k	22 - >22k	A-Wtg	5,1,4,6,2,7,3	0	1,2,3,5,6,5,6	0	Internal	n/a	Analog
ANLG_MAIN_DIR_IN345_TO_ANLG_MAIN_AMP1_OUT_XTALK	2	1.00 Vrms	1.00 Vrms	1k, 20k	None	25	Unbal	Float	dB	Level	<-58.00	-55.00	-150.00	100k	<10 - >22k	None	2,3,4	0	2	0	Internal	n/a	Analog
ANLG_MAIN_DIR_IN345_TO_ANLG_MAIN_AMP2_OUT_XTALK	2	1.00 Vrms	1.00 Vrms	1k, 20k	None	25	Unbal	Float	dB	Level	<-58.00	-55.00	-150.00	100k	<10 - >22k	None	1,3,4	0	6	0	Internal	n/a	Analog
ANLG_MAIN_DIR_IN345_TO_ANLG_MAIN_AMP3_OUT_XTALK	2	1.00 Vrms	1.00 Vrms	1k, 20k	None	25	Unbal	Float	dB	Level	<-58.00	-55.00	-150.00	100k	<10 - >22k	None	1,2,4	0	6	0	Internal	n/a	Analog
ANLG_MAIN_DIR_IN345_TO_ANLG_MAIN_AMP4_OUT_XTALK	2	1.00 Vrms	1.00 Vrms	1k, 20k	None	25	Unbal	Float	dB	Level	<-58.00	-55.00	-150.00	100k	<10 - >22k	None	1,2,3	0	3	0	Internal	n/a	Analog
ANLG_MAIN_DIR_IN345_TO_ANLG_MAIN_AMP5_OUT_XTALK	2	1.00 Vrms	1.00 Vrms	1k, 20k	None	25	Unbal	Float	dB	Level	<-58.00	-55.00	-150.00	100k	<10 - >22k	None	6,7	0	1	0	Internal	n/a	Analog
ANLG_MAIN_DIR_IN345_TO_ANLG_MAIN_AMP6_OUT_XTALK	2	1.00 Vrms	1.00 Vrms	1k, 20k	None	25	Unbal	Float	dB	Level	<-58.00	-55.00	-150.00	100k	<10 - >22k	None	5,7	0	5	0	Internal	n/a	Analog
ANLG_MAIN_DIR_IN345_TO_ANLG_MAIN_AMP7_OUT_XTALK	2	1.00 Vrms	1.00 Vrms	1k, 20k	None	25	Unbal	Float	dB	Level	<-58.00	-55.00	-150.00	100k	<10 - >22k	None	5,6	0	5	0	Internal	n/a	Analog
ANLG_MAIN_DIR_IN345_TO_ANLG_MAIN_AMP1-7_OUT_PWR_VS_THD																							
ANLG_MAIN_DIR_IN345_TO_ANLG_MAIN_AMP1_OUT_PWR_VS_THD	2	+0.75 - +1.00	+0.75 - +1.00	1k	None	600	Unbal	Float	W	Level	> 140.50	180.00	140.00	100k	22 - >22k	None	1	0	2	0	Internal	n/a	Analog
	2	+0.75 - +1.00	+0.75 - +1.00	1k	None	600	Unbal	Float	%	THD+N	< 0.010	0.020	0.0001	100k	22 - >22k	None	1	0	2	0	Internal	n/a	Analog
ANLG_MAIN_DIR_IN345_TO_ANLG_MAIN_AMP2_OUT_PWR_VS_THD	2	+0.75 - +1.00	+0.75 - +1.00	1k	None	600	Unbal	Float	W	Level	> 140.50	180.00	140.00	100k	22 - >22k	None	2	0	6	0	Internal	n/a	Analog
	2	+0.75 - +1.00	+0.75 - +1.00	1k	None	600	Unbal	Float	%	THD+N	< 0.010	0.020	0.0001	100k	22 - >22k	None	2	0	6	0	Internal	n/a	Analog
ANLG_MAIN_DIR_IN345_TO_ANLG_MAIN_AMP3_OUT_PWR_VS_THD	2	+0.75 - +1.00	+0.75 - +1.00	1k	None	600	Unbal	Float	W	Level	> 140.50	180.00	140.00	100k	22 - >22k	None	3	0	6	0	Internal	n/a	Analog
	2	+0.75 - +1.00	+0.75 - +1.00	1k	None	600	Unbal	Float	%	THD+N	< 0.010	0.020	0.0001	100k	22 - >22k	None	3	0	6	0	Internal	n/a	Analog
ANLG_MAIN_DIR_IN345_TO_ANLG_MAIN_AMP4_OUT_PWR_VS_THD	2	+0.75 - +1.00	+0.75 - +1.00	1k	None	600	Unbal	Float	W	Level	> 140.50	180.00	140.00	100k	22 - >22k	None	4	0	3	0	Internal	n/a	Analog
	2	+0.75 - +1.00	+0.75 - +1.00	1k	None	600	Unbal	Float	%	THD+N	< 0.010	0.020	0.0001	100k	22 - >22k	None	4	0	3	0	Internal	n/a	Analog
ANLG_MAIN_DIR_IN345_TO_ANLG_MAIN_AMP5_OUT_PWR_VS_THD	2	+0.75 - +1.00	+0.75 - +1.00	1k	None	600	Unbal	Float	W	Level	> 140.50	180.00	140.00	100k	22 - >22k	None	5	0	1	0	Internal	n/a	Analog
	2	+0.75 - +1.00	+0.75 - +1.00	1k	None	600	Unbal	Float	%	THD+N	< 0.010	0.020	0.0001	100k	22 - >22k	None	5	0	1	0	Internal	n/a	Analog
ANLG_MAIN_DIR_IN345_TO_ANLG_MAIN_AMP6_OUT_PWR_VS_THD	2	+0.75 - +1.00	+0.75 - +1.00	1k	None	600	Unbal	Float	W	Level	> 140.50	180.00	140.00	100k	22 - >22k	None	6	0	5	0	Internal	n/a	Analog
	2	+0.75 - +1.00	+0.75 - +1.00	1k	None	600	Unbal	Float	%	THD+N	< 0.010	0.020	0.0001	100k	22 - >22k	None	6	0	5	0	Internal	n/a	Analog
ANLG_MAIN_DIR_IN345_TO_ANLG_MAIN_AMP7_OUT_PWR_VS_THD	2	+0.75 - +1.00	+0.75 - +1.00	1k	None	600	Unbal	Float	W	Level	> 140.50	180.00	140.00	100k	22 - >22k	None	7	0	5	0	Internal	n/a	Analog
	2	+0.75 - +1.00	+0.75 - +1.00	1k	None	600	Unbal	Float	%	THD+N	< 0.010	0.020	0.0001	100k	22 - >22k	None	7	0	5	0	Internal	n/a	Analog
ANLG_MAIN_DIR_IN345_TO_ANLG_MAIN_AMP_OUT_PWR_VS_THD																							
ANLG_MAIN_DIR_IN345_TO_ANLG_MAIN_AMP1-7_OUT_POWER_VS_THD	2	+0.75 - +1.00	+0.75 - +1.00	1k	None	600	Unbal	Float	W	Level	> 140.50	180.00	140.00	100k	22 - >22k	None	1	0	1,2,3,5,6,5,6	0	Internal	n/a	Analog
	2	+0.75 - +1.00	+0.75 - +1.00	1k	None	600	Unbal	Float	%	THD+N	< 0.02	0.050	0.0001	100k	22 - >22k	None	1	0	1,2,3,5,6,5,6	0	Internal	n/a	Analog

D-A Amplifier Tests		Digital Generator (fftgen)							Digital Analyzer (Spectrum analyzer)								Switcher Module						
Test Name	See Note:	Left	Right	Freq (Hz)	EQ Curve	Z-out	Bal/ Unbal	Gnd/ Float	Level	Measure	Typical Reading	Upper Limit	Lower Limit	Imp.	Bandwidth	Freq	A In	B In	A Out	B Out	Clock Source	Sample Rate	Audio Source
DIG_MAIN_COAX1_IN_44K_TO_ANLG_MAIN_AMP567_OUT_NOISE																							
DIG_MAIN_COAX1_IN_44K_TO_ANLG_MAIN_AMP567_OUT_NOISE		OFF	OFF	1k	None	n/a	n/a	n/a	dBV	A/D Level	-90.00	-87.00	107.00	100k	22 - >22k	5512	5	0	0	0	External	44100	Digital
		OFF	OFF	1k	None	n/a	n/a	n/a	dBV	A/D Level	-91.00	-88.00	107.00	100k	22 - >22k	5512	6	0	0	0	External	44100	Digital
		OFF	OFF	1k	None	n/a	n/a	n/a	dBV	A/D Level	-92.00	-92.00	107.00	100k	22 - >22k	5512	7	0	0	0	External	44100	Digital

NOTES

1. Tests are performed using the Audio Precision System Two Cascade
2. Tests are performed using the Audio Precision System One

AMPLIFIER INPUT SOURCE:	CONFIGURATION OUTPUT CHANNEL:
Main DIR IN3 Left	Front Left (#5)
Main DIR IN3 Right	Front Right (#1)
Main DIR IN4 Left	Center (#4)
Main DIR IN5 Left	Side Left (#6)
Main DIR IN5 Right	Side Right (#2)
Main DIR IN5 Left	Rear Left (#7)
Main DIR IN5 Right	Rear Right (#3)

FM SIGNAL GENERATOR CONFIGURATION														
Ext Mod Input		Modulation										Program	Frequency	Pre-Emph	Amplitude
Left	Right	FM	AM	FM (kHz)	Pilot (kHz)	AM (%)	Display	Mod	Pilot	Mono		Address	(MHz)	(75µS)	(dBµ)
n/a	EXT	OFF	ON	n/a	n/a	30.0	AM	ON	OFF	n/a		0	1.050	n/a	60.0
EXT	EXT	ON	OFF	67.5	7.5	n/a	FM	ON	OFF	OFF		1	97.900	OFF	60.0

CHAPTER 5 – TROUBLESHOOTING

This chapter contains a complete description of the diagnostic tests for the RV-8. The diagnostics in the RV-8 are used to verify functionality of the unit and to aid in troubleshooting defective units. Familiarity is assumed with the RV-8 structure, all applicable assembly drawings, FAT process, and Audio ATE processes.

DIAGNOSTIC CATEGORIES

There are two types of diagnostics in the RV-8: power-on and extended. The entire set of power-on diagnostics is executed every time a unit is powered on using the rear panel power switch. The power-on diagnostic tests can be run individually in the extended diagnostics. The extended diagnostics contain the tests that are used to verify functionality and to aid in troubleshooting. The extended diagnostics also contain additional tests used to verify all the front panel controls, infrared communications, audio and video performance, etc. The troubleshooting or repair diagnostics are utilized to troubleshoot an RV-8 if any test fails.

POWER-ON MODES

There are two power-on modes available: power on via the rear panel power switch, and by bringing the RV-8 out of standby mode. The power-on diagnostics are executed every time the rear panel power switch is switched on. When an RV-8 is in normal operating mode, pressing the front panel standby button or the remote control (SYSTEM) OFF button will put the unit into a low power/standby mode. When the RV-8 is in standby mode, pressing any of the front panel or remote control Main, Zone 2 or Zone 3 input select buttons, and/or pressing the front panel standby button or the remote control POWER button will bring the RV-8 out of standby mode. No diagnostics are run when the unit is brought out of standby.

DIAGNOSTICS USER INTERFACE

Various combinations of button pushes are used to control diagnostic activity. The table below summarizes the options available, followed by more detailed descriptions.

Action	Buttons to be Held
Enter Diagnostics	ZONE2 DVD2 & ZONE3 DVD2
Restore Defaults	MODE RIGHT
Waiting For Download	MODE RIGHT & ZONE2 DVD2 & ZONE3 DVD2

To enter extended diagnostics via front panel:

1. Press and hold the front panel **ZONE2 DVD2** and **ZONE3 DVD2** buttons when powering on a RV-8.
2. Continue to hold both buttons until the “DIAGS MENU” appears on the front panel display.

   This operation normally takes approximately thirty seconds to complete.

To enter extended diagnostics via serial debug port:

Type “debug” when connected to the serial port to access the debug program (The debug program is case sensitive). In addition, the extended diagnostics can also be entered by sending “ed”, (stands for extended diagnostics), to the unit via the serial debug port during the first ten seconds after powering on the unit. For more information, see the section on the Serial Debug program.

To restore factory default settings:

1. Press and hold the front panel **Mode ▸** button while powering on the RV-8 to restore the factory default settings.
2. Continue to hold both buttons until the unit has restarted and the amplifier status LEDs have turned on.

   This operation normally takes approximately forty-five seconds to complete.

To enter the Download mode:

1. Press and hold the front panel **Mode ▸, ZONE2 DVD2** and **ZONE3 DVD2** buttons when powering on a RV-8 to put the unit into the mode used for downloading the software application.
2. Continue to hold both buttons until “WAITING FOR DOWNLOAD" appears on the front panel display.

   This operation normally takes approximately twenty-five seconds to complete.

DIAGNOSTIC REPORTING

All diagnostic functionality is reported to the Vacuum Fluorescent Display (VFD). They report on what test is being executed, and if the test passed or failed.

Diagnostic status and data is also available on an external PC or a terminal, via the serial debug port located at the D9 connector labeled RS 232 on the rear panel of the RV-8. In the event a diagnostic failure occurs for those diagnostic tests that report additional failure information, such as data sent, data received, address location, etc., can be viewed on the VFD display, or it can be sent to the serial debug port.

Vacuum Fluorescent Display (VFD)

The VFD is the primary source of information during diagnostics. The exact display information will depend on the test(s) being executed. When an individual diagnostic test is executed, the VFD will display the name of that test. Groups of tests, such as the power-on diagnostics, have a generic message on the top line of the VFD. For example, “DIAGNOSTIC TESTS” is on the VFD while the power-on diagnostics are being run. An “E” followed by a number that indicates which test failed displays failure messages.

Front Panel LEDs

The front panel LEDs for the Main input select buttons are also used to display the diagnostic test number. The LEDs are used in binary format with the Main Tuner LED as the LSB and the Main DVD2 LED as the MSB as shown in the table below:

Test Number:

Main LED:	Phono	Tuner	CD	TV	VCR	Sat	DVD2	DVD1
BIT:	0	1	2	3	4	5	6	7

Running test number 1 would illuminate the Main Phono LED only with all the others off. Running test number 3 would illuminate the Main Phono LED and Main Tuner LEDs only with all others off, etc. If a failure occurs, the front panel LEDs indicating the test number that was running when the failure occurred will also continue to be illuminated.

The diagnostics will attempt to continuously execute the failed test, a test loop, to keep the signal lines active as an aid in debugging the failure.

Serial Debug Port

The Serial Debug Port is available to provide diagnostic status to be viewed on an external PC from the D9 connector labeled RS232. Using a terminal or a PC running a terminal program, the progress of the diagnostics can be monitored and test failure information is reported. The serial protocol is 19200bps, 8, O, 1, (8 data bits, Odd Parity, 1 Stop Bit).

Serial Debug Cable

The cable required to connect the RS232 serial debug port to the computer is a straight-through serial interface cable. A null modem adapter or cable should not be used. The RV-8 RS232 connector on the rear panel is a D9 female; so one end of the serial cable must be a D9 male. The other connector on the cable depends upon the RS232 connector used on the computer. The computer may have a D9 or a D25 male connector. Typically computers have a D9 for COM 1 and a D25 for COM 2. However, some newer computers use a D9 for both COM 1 and COM 2. The COM port used on the computer does not matter, however you must ensure that whatever serial communications program is being used has the correct computer COM port selected.

Serial Debug Program

The serial debug program controls the communication from an RV-8 to a computer. This program allows a user to view activity of the unit and to control and configure the unit for testing. The debug program is used extensively to perform audio and video testing of a unit in the audio and video ATE programs.

Error Codes

The error codes for the diagnostic tests that report additional failure information consist of six parts as described below:
“E## tXX aYYYYYY
wZZZZZZ rQQQQQQ”

E##: Failure Number

The E stands for error and the hexadecimal number after the E indicates test number from the list below.

tXX: Error Codes List

NO_ERROR	0x0
ADDR_FAILURE	0x1
DATA_FAILURE	0x2
TIMEOUT_FAILURE	0x3
COUNTER_FAILURE	0x4
NON_VOL_DATA_FAILURE	0x5
OPCODE_FAILURE	0x6
AVRX_FPGA_ID_NO_MATCH	0x7
DAR_FPGA_ID_NO_MATCH	0x8
AUDIO_FPGA_ID_NO_MATCH	0x9
ANALOG_FPGA_ID_NO_MATCH	0xA
VFD_TIME_OUT	0xB

VFD_RAM_ERROR	0xC
TEST_INCOMPLETE	0xD
RS232_WRAP_FAILURE	0xE
SRAM_PREBURNIN_FAILURE	0x13
SRAM_BURN_IN_FAILURE	0x14
EPROM_CHKSUM_FROM_FLASH	0x15
DRAM_FAILURE	0x16
FIFO_ERROR_OVERRUN	0x17
PIC_SN_INVALID	0x18
FLASH_BURN_FAIL	0x19
FLASH_BURN_NO_ROOM_LEFT	0x1A
FLASH_BURN_NOT_FLASH_PART	0x1B
SHARC_TIMEOUT_REBOOT	0x1C
DSP_FPGA_ID_NO_MATCH	0x1D
DEC_FPGA_ID_NO_MATCH	0x1E
DIAG_TEST_NOT_EXIST	0x20
THERMOSTAT_FAILURE	0x21
EXPANSION_BRD_FAILURE	0x22
ERROR_ID_BAD_VALUE	0x40
ERROR_PARAM_SEMA_CREATE	0x60
CS49400_NO_BOOT_START_MESSAGE	0x100
CS49400_NO_BOOT_SUCCESS_MESSAGE	0x101
CS49400_INIT_ERROR	0x102
CS49400_ERR_WRITE_TIMEOUT	0x103
CS49400_ERR_READ_TIMEOUT	0x104
CS49400_INTREQ_TIMEOUT	0x105
CS49400_AUTO_BOOT_FAILURE	0x106
CS49400_ENQ_MSG_FAILURE	0x107
CS49400_DEQ_MSG_FAILURE	0x108
CS49400_FINTREQ_TIMEOUT	0x109
CS49400_NO_APP_START_MESSAGE	0x110
CS49400_AB_SPI_TIMEOUT	0x111
CS49400_C_SPI_TIMEOUT	0x112
CS49400_HOST_BOOT_FAILURE	0x113
CS49400_FLASH_WRITE_TIMEOUT	0x114
CS49400_BAD_FLASH_DATA	0x115
CS49400_BAD_RESP_OPCODE	0x116
CS49400_FLASH_READ_TIMEOUT	0x117
CS49400_MASTER_BOOT_FAILURE	0x118
CS49400_BAD_FLASH_VERSION	0x119
CS49400_ERASED_FLASH	0x11A

CS49400_CHECKSUM_FAIL	0x11B
CS8420_INIT_ERROR	0x200
CS8420_ISC_WR_TIMEOUT	0x201
CS8420_ISC_RD_TIMEOUT	0x202
CS8420_WRONG_VERSION	0x203
CS8420_WRONG_ID	0x204

These codes are used to interpret the diagnostic results from the Extended Diagnostic Repair Menu. The Error code is 16-bits with the most significant byte always being 0x03.

The least significant byte is broken into bits as shown below:

(MSBit) B7 B6 B5 B4 B3 B2 B1 B0 (LSBit)

- B7 - not used. Should always be 0.
- B6 - GPIO LED failure, 1 indicates that neither LED lit up from the test.
- B5 - Read Back Register Fail, 1 indicates the Read back register failed.
- B4 - Test Fail, 1 indicates the test failed, 0 indicates success.
- B3 - SHARC Test Completed. 1 indicates that the SHARC was able to finish executing the test.
- B2 - READ Time out, 1 means that Hitachi could not read back from the SHARC. 1 indicates time out.
- B1 - WRITE Time out, 1 is means there was a time out.
- B0 - SHARC processor id 0 is for Processor A and 1 for Processor B.
- Bits B2, B1 and B0 are read together. If a time out occurs then B2 or B1 will indicate what operation caused the fault, B0 will indicate which processor failed, Processor A or B.
- Bit B3 is used to indicate whether the SHARC was able to run the code. If this bit is zero, the code was not able to run; a 1 indicates the SHARC was able to run.
- Bit B4 indicates whether the test passed or failed. This bit is only valid if B3 is a 1.
- Bit B5 indicates that the read back register failed. There is a fault in the read back register circuitry if this bit is a 1.
- Bit B6 indicates whether the circuitry around the SHARC LEDS failed. A 1 indicates a failure.

When the SHARC passes these tests, it will return a value of 0x0300.

aYYYYYY: Failing address location

The address (in hexadecimal) where the failure occurred.

wZZ: Value Written

The target value (in hexadecimal) that was written to the address where the failure occurred.

rQQ: Value Read

The actual value (in hexadecimal) that was read from the address where the failure occurred.

POWER ON DIAGNOSTICS

As described earlier there are two power-on modes in the RV-8. You can power on via the rear panel power switch or by bringing the RV-8 out of standby mode. Power-on diagnostics are executed every time the rear panel power switch is switched on. Diagnostics are not run when the unit is brought out of standby.

The power-on diagnostics take approximately fifty seconds to complete. The power-on diagnostics are intended to verify basic hardware functionality of an RV-8. Additional diagnostic tests are available to completely test the hardware, and for debugging failures.

Initially, an attempt is made to illuminate the VFD and front panel LEDs for approximately five seconds. However, during the first four tests the VFD will not be considered functional due to it not being tested. During these tests, Trap Op Code, SH Flash Checksum, SH DRAM, and VFD RAM, the unit will attempt to use the standby LED to indicate if a failure occurs. As soon as these tests are completed the VFD will display:
“DIAGNOSTIC TESTS
… …”

The dots increment in number from both sides simultaneously, as the rest of the power-on diagnostic tests are completed. This informs you that the unit is still functioning. The audio outputs (digital and analog) will be muted during this sequence.

The following is a list of test explanations. The front panel display is shown only for the first test that can use the VFD. The reference designators used are from Revision 5 Main Board 710-15550 used on BOM 023-15615. The schematics for the main board are 060-15559.

Trap Opcode

The Trap Opcode error occurs if during the initial boot sequence an undefined Opcode is fetched. The INT/TRAP Control register can be used to determine the starting address of the undefined instruction. If the trap error occurs, an attempt will be made to blink the standby LED using a rate of a single blink per several seconds, and the test will attempt to enter a loop to exercise signal lines to aid in debugging.

SH Flash Checksum Test

The SH Flash Checksum test verifies U26 on the Main Board, has the correct program by adding up all the values in memory and checking it against the value stored. The checksum is reported to the Serial Debug Port. The test verifies that the calculated checksum matches the checksum value stored in the flash. If an error occurs an attempt will be made to blink the standby LED using a rate of a two blinks per several seconds, and the test will attempt to enter a loop to exercise signal lines to aid in debugging.

SH DRAM Test

The SH DRAM test performs write and read testing on the DRAM. The test uses patterns 0x00, 0xFFFF, 0x5555, and 0xAAAA. Once each location in the DRAM is verified, a walking 1s check is done to test address buss integrity. If an error occurs, an attempt will be made to blink the STANDBY LED using a rate of three blinks per several seconds, and the test will attempt to enter a loop to exercise signal lines to aid in debugging.

VFD Test

The VFD (vacuum fluorescent display) performs a busy test and a memory test. The busy test sends information to the VFD and verifies that the VFD asserts then de-asserts its busy status. The VFD memory test consists of writing 55h, AAh, a walking 1 and finally a 0 to the character generator memory and display memory space of the VFD and reading them back. After the RV-8 has passed the VFD Test, for the rest of the power on diagnostics, the VFD displays:
“DIAGNOSTIC TESTS
… …”

The dots increment in number from both sides simultaneously, as the rest of the power-on diagnostic tests are completed. This keeps you informed as to the functioning of the RV-8. If a failure occurs, the test will attempt to enter a loop to exercise signal lines to aid in debugging.

Display for the Remaining Tests

If any of the following tests fail the VFD display and LED matrix will display the test and error fault, as previously discussed. The VFD will display the test number and the error code. In the event that the VFD is not operable, the same information will be written to the LED matrix. The test number will be read out as in the top row. The error number can be read out in the second row (Most Significant Byte) and third row (Least Significant Byte).

AVRX FPGA Test

The AVRX FPGA test verifies the ID register can be read from the XC2S200 on the main board. If a failure occurs, the test will attempt to write the test number and the error number to the VFD.

CS49400 Test

This test verifies that the Crystal 49400 Decoder can communicate with the Host Hitachi processor through the AVRX FPGA. If a failure occurs, the test will attempt to write the test number and the error number to the VFD.

Power On Diagnostics Completed

After the power-on diagnostics are completed, the VFD will display the appropriate power up message:
“MANUFACTURER MODEL VX.XX
(c) 200X OPTIONS”

At this point the normal operating software takes over the functioning of the RV-8.

Debug Terminal Monitor Test (optional)

If the unit is not powering up correctly, monitor the boot sequence using a debug terminal monitor.

Test:

1. Power off the unit.
2. Connect a debug terminal monitor to the RV-8 RS232 serial port 2.
3. Power on the unit and monitor the boot sequence.

***Note**:*
In order to see data on the debug port, use the following serial protocol:19200bps, 8, O, 1, (8 data bits, Odd Parity, 1 Stop Bit).

EXTENDED DIAGNOSTIC TESTS

The extended diagnostic tests are accessible by pressing and holding the ZONE2 DVD2 & ZONE3 DVD2 front panel buttons when powering on a RV-8. The audio outputs (analog and digital) are muted. When the VFD on the unit displays “LEXICON,” the front panel buttons can be released. After the model banner is briefly displayed on the VFD, the display will indicate:
“DIAGS MENU
FUNCTIONAL TESTS”

The extended diagnostics can also be entered via the serial debug port by first entering the debug program. Typing “debug” when connected to the serial port accesses the debug program. The debug program is case sensitive. In addition the extended diagnostics can be entered by sending “ed,” which stands for extended diagnostics, to the unit via the serial debug port during the first ten seconds after powering on the unit.

After extended diagnostics are entered, use the front panel encoder, Mode ▸ and Mode ◂ buttons to navigate through the diagnostics. The front panel encoder is rotated to display the desired tests. The Mode ▸ button is pressed to move down through the menu selections and to execute the desired diagnostic test. The Mode ◂ button is used to move back through menu selections similar to an escape button (Esc) on a computer keyboard.

Types of Diagnostic Tests

The extended diagnostic tests fall into two categories. The first category is for tests required to functionally verify the RV-8. These tests are performed on every unit. These will be referred to as Functional Diagnostic tests. The second category is for troubleshooting defective units. These tests are only utilized if there is a failure. The troubleshooting tests can be used to help isolate the source of failures so that units can be cost effectively fixed. These tests are referred to as Repair diagnostics.

Two groups of tests are executed for every RV-8. These are the Loop Tests and the Functional Test Suite. The Loop Tests and the Functional suite comprise the automated sets of tests used to verify proper operation of every unit. Each of the tests in these suites are run in order unless there is a failure. The failing test will loop to allow the electrical signals to be active for troubleshooting. You can optionally continue to run the other diagnostic tests in the suite. The Repair suite allows you to run particular tests for troubleshooting.

User Interface

The user interface consists of a set of menus. The top menu is the "DIAGS MENU" and is shown in the top line of the VFD display. To view the available menu items, turn the encoder knob in either direction and the menu choices will appear in the second row. When the desired menu item is shown, press the Mode ▸ button. This selects the menu item. If the item is another menu, the menu's title now appears in the top line of the VFD and its menu items are in the second row. If a test is selected, the test name will appear in the top line and the results or information to run the test will be on the second row. Once a test is finished, or to get out of a menu, press the Mode ◂ button.

The group tests are the diagnostics, in which if a test passes, the diagnostics automatically execute the next test. Group tests are the Power-On Diagnostics and the Functional Test suite. If one of the group tests is selected, each test in the group is automatically run if the current test passes. Upon successful completion of the group tests, the VFD will either display "Pass" or "Fail" and come out of the test group to the menu, or it will continuously loop.

If a test fails, the VFD, and front panel LEDs, will attempt to indicate the failed test. The test will attempt to loop to keep the signal lines active for debugging purposes. If an individual test is selected, it will continuously run and report if it passes every time it successfully completes the test. If the test fails, it will attempt to loop to keep the signal lines active for debugging purposes. In addition, test progress and failure information is available via the serial debug port. Specific failure information will depend on the test

being executed. Pressing and holding the Mode ▸ button returns the user to the top-level diagnostic menu.

Repair Diagnostics Suite

The repair tests suite is the section where every diagnostic test can be executed individually. Additionally, the repair test suite allows you to run any single diagnostic test infinitely. The encoder knob is used to scroll through each diagnostic test. To run any particular test or to move into a sub-menu, use the Mode ▸ button. To back out of a sub-menu or to return out of a test, use the Mode ◂ button.

Sub-menus can be used to partition off groups of tests that deal with a portion of the board. For example, the SHARC tests and the Trigger tests can be placed in sub-menus. In the repair suite, the SHARC tests will also include tests as outlined below.

- SHARC WCLK
  - SHARC BOOT
    - PAIR 0
    - PAIR 1
  - SHARC SDRAM
    - PAIR 0
    - PAIR 1
  - SHARC WCLK
    - PAIR 0
    - PAIR 1

In the repair suite the ability to set each trigger on and off will be available.

- SET TRIGGERS
  - Trigger 0 ON
  - Trigger 1 ON
  - Trigger 0 OFF
  - Trigger 1 OFF

The following diagnostic selections are available in the repair tests suite:

- SH FLASH CHECKSUM
- SH DRAM
- AVRX FPGA VERIFY
- RS232 WRAP TEST
- SHARC TESTS
  - SHARC BOOT
    - PAIR 0/1
  - SHARC SDRAM
    - PAIR 0/1
  - SHARC WCLK
    - PAIR 0/1
- CS49400 TESTS
  - BOOT TEST
  - SHOW FLASH VERSION
  - FLASH CHECKSUM TEST
  - LOAD FLASH
- IR REMOTE
- VFD MEMORY TEST
- VFD CHAR TEST
- VFD BLOCK TEST

OSD CHAR TEST
    PAGE: (0-11)
SWITCH TEST
LED TEST
ENCODER TEST
SET TRIGGERS
    TRIGGER 0
        TRIGGER: OFF/ON
    TRIGGER 1
        TRIGGER: OFF/ON
AMP RELAY TESTS
    MAIN RELAY
        RELAY: OFF/ON
    CHANNEL 1
        RELAY: OFF/ON
    CHANNEL 2
        RELAY: OFF/ON
    CHANNEL 3
        RELAY: OFF/ON
    CHANNEL 4
        RELAY: OFF/ON
    CHANNEL 5
        RELAY: OFF/ON
    CHANNEL 6
        RELAY: OFF/ON
    CHANNEL 7
        RELAY: OFF/ON
    ALL RELAYS
        RELAY: OFF/ON
SET FAN TEST
    FAN SPEED: (0-3)
THERMOSTAT TEST
    AMP: (1-7)
HEADPHN INSERTION
EXPANSION BRD TEST
DIG RCVR LOCK TEST
SHUT OFF HV AMP PWR
SET CONSTANT CYCLE
NORMAL OPERATION

The repair diagnostic tests that are the same as in the power-on diagnostic tests and functional diagnostic tests are not described here.

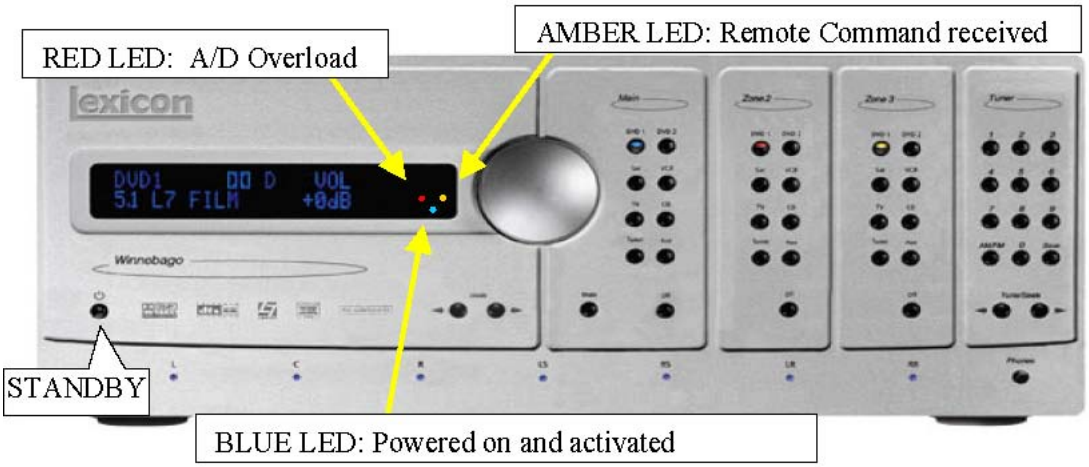
FUNCTIONAL DIAGNOSTICS DESCRIPTIONS

Diagnostic Tests

This section describes the RV-8 power-on and diagnostics process.

Setup:

1. Connect the RV-8 to a 120VAC (220VAC for European model) power source.
2. Set the rear panel power switch of the RV-8 to the "1" (ON) position.



Test:

1. Verify the three LEDS at the right side of the VFD display light: RED, AMBER and BLUE.
2. In approximately three seconds, verify the display indicates: "**LEXICON **"
3. When the "** LEXICON **" display appears, within eight seconds press and hold the **Zone 2 DVD2** and **Zone 3 DVD2** buttons.
4. The display indicates a display similar to the following. Note that the BOOTROM revision date "XX/XX" and time "XX:XX" will contain valid digits:
   "LEXICON RV-8 BOOTROM
   ©200X XX/XX XX:XX"
5. Continue to hold the buttons for another seven seconds until the display indicates:
   "DIAGS MENU
   FUNCTIONAL TESTS"

FUNCTIONAL TESTS

The automated Functional Tests will execute the suite of tests. This takes approximately forty-five seconds to complete. When the automated Functional Tests have completed, you will be prompted to perform certain tasks to complete the rest of the functional tests.

Setup:

Press the **Mode** ▸ button. The display should indicate:
“FUNCTIONAL TESTS
START ALL TESTS”

Test:

Press the **Mode** ▸ button again to start the tests. When the test has completed the front panel display should indicate:
“RS232 WRAP TEST
Insert Wrap Plugs”

RS232 Wrap Test

This test verifies that the unit can communicate with the rear panel serial communication connectors.

Setup:

1. Create two (2) RS 232 wrap around plugs by connecting pins 2 & 3 of a female DB9 connector.
2. Install the two RS 232 wrap around plugs onto the RS 232 1 and 2 ports located on the RV-8 rear panel.

Test:

1. Press the **Mode** ▸ button to run the test. Verify the display indicates:
   “SERIAL PORT 1 PASSED
   SERIAL PORT 2 PASSED”
2. Press the **Mode** ◂ button.
3. Remove the two (2) RS 232 wrap around plugs when prompted by the RV-8 display.
4. Press the **Mode** ◂ button to proceed to the next test.

IR Remote Test

This test verifies that the unit can respond to infrared commands from the infrared remote.

Remote Setup:

1. Set the remote control to its default menu by pressing the **HOME** button.
   The LCD display on the remote control should appear as in Figure A below.
2. Press the top left **MAIN** button once to open the MAIN menu.
   The LCD display on the remote control should appear as in Figure B below.

Figure A: HOME MENU

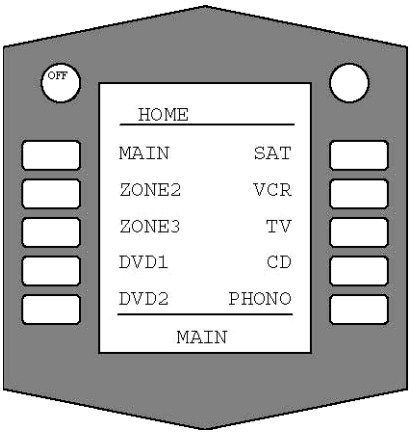
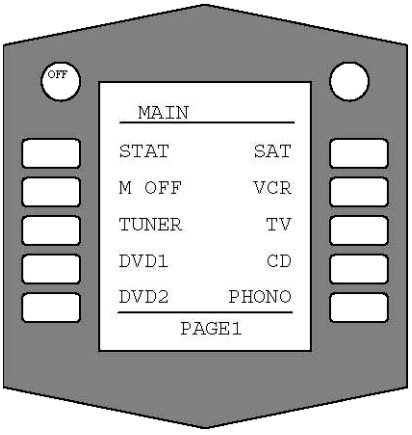


Figure B: MAIN MENU



***Note**:*
The RV-8 will NOT respond to the PAGE, HOME, FAV, M1, M2 and M3 buttons.

3. RV-8 Setup: The front panel display should indicate:
   "IR REMOTE TEST
   Remote Test:"

Test:

1. Press and hold the **DVD2** button on the remote.
2. Verify the yellow IR ACK LED is blinking on the RV-8 front panel.
3. Verify the display indicates:
   "IR REMOTE TEST Remote
   Test: 21 IR"
4. Press the **Mode** ◂ button to proceed to the next test.

Display Character Test

This test verifies that the display on the unit can display the same character on every pixel.

Test:

1. Verify the display indicates:
   "AAAAAAAAAAAAAAAAAAA AAAAAAAAAAAAAAAAAAA."
2. Turn the **encoder knob** clockwise until the display indicates:
   "BBBBBBBBBBBBBBBBBBB BBBBBBBBBBBBBBBBBBB"
3. Turn the **encoder knob** counter clockwise until the display indicates:
   "??????????????????? ???????????????????"
4. Turn the encoder knob counter clockwise until the display indicates:
   "==========
   ==========
   ==========
   =========="
5. Press the **Mode** ◂ button to proceed to the next test.

Display Block Test

This test verifies that the unit can display all the pixels in one block at a time.

Test:

1. Verify the display has one block lit with no missing pixels in the top left corner of the display.
2. Turn the **encoder knob** clockwise until all forty blocks have been displayed.

***Note**:*
The blocks along the top row will be lit first followed by the blocks on the bottom row (If the knob is continuously turned clockwise the block lighting pattern will repeat).

3. Press the **Mode** ◂ button to proceed to the next test.

Switch Test

This test verifies the operation of each of the twenty-two front panel switches. During the test the LED associated for each switch pressed will light and remain lit until another switch is pressed.

Setup:

The front panel display should indicate: "SWITCH TEST SwTst: None pressed."

Test:

1. Press each switch and verify that the front panel display indicates the correct name for the switch.

   Standby = STANDBY Mode

   Left = LEFT MODE

   Right = RIGHT MODE

   Mute = MUTE MODE

   The MAIN switches = MAIN *Switch Name*, where *Switch Name* is the name of the Switch that is labeled on the front panel.

   The Zone 2 switches = ZONE 2 *Switch Name*, where *Switch Name* is the name of the Switch that is labeled on the front panel.

   The Zone 3 switches = ZONE 3 *Switch Name*, where *Switch Name* is the name of the Switch that is labeled on the front panel.

   The Tuner switches = TUNER *Switch Name*, where *Switch Name* is the name of the Switch that is labeled on the front panel.

   When all twenty-two switches have been pressed the display will indicate:
   "SWITCH TEST All Switches Done."

2. Press the **Mode ◂** button to proceed to the next test.

Encoder Test

This test verifies the operation of the encoder knob.

Setup:

The front panel display should indicate: "ENCODER TEST ENCODER Test."

Test:

1. Turn the **encoder knob** clockwise until the display indicates:
   "ENCODER TEST Encoder Test CCW 24."
2. Turn the **encoder knob** counter-clockwise until the display indicates:
   "ENCODER TEST ENCODER Test Passed."
3. Press the **Mode ◂** button to proceed to the next test.

LED Test

This test verifies the operation of each of the twenty-three front panel LEDs.

Setup:

The front panel display should indicate: "LED TEST LED Test: 11 STBYRed."

Test:

1. Turn the **encoder knob** clockwise and verify that each LED lights individually and is the correct color. See the color code table below and on the next page.
2. When all LEDs have been lit, press the **Mode** ◂ button to proceed to the next test.

LED Color

CODE	LED	COLOR
11	Standby	RED
12	Ready	BLUE
49	IR Ack	YELLOW
50	Overld	RED
51	Sys ON	BLUE
10	Mute	YELLOW
	MAIN	
0	Main DVD1	BLUE
2	Main Sat	BLUE
4	Main TV	BLUE
6	Main Tuner	BLUE
1	Main DVD2	BLUE
3	Main VCR	BLUE
5	Main CD	BLUE
7	Main Phono	BLUE
9	Main OFF	RED
	ZONE2	
16	Zone2 DVD1	YELLOW
18	Zone2 SAT	YELLOW
20	Zone2 TV	YELLOW
22	Zone2 Tuner	YELLOW
17	Zone2 DVD2	YELLOW
19	Zone2 VCR	YELLOW
21	Zone2 CD	YELLOW
23	Zone2 Phono	YELLOW
24	Zone2 OFF	RED

CODE	LED	COLOR
	ZONE3	
32	Zone3 DVD1	RED
34	Zone3 SAT	RED
36	Zone3 TV	RED
38	Zone3 Tuner	RED
33	Zone3 DVD2	RED
35	Zone3 VCR	RED
37	Zone3 CD	RED
39	Zone3 Phono	RED
40	Zone3 OFF	RED
	OTHER	
8	Amp 1	BLUE
25	Amp 2	BLUE
26	Amp 3	BLUE
27	Amp 4	BLUE
41	Amp 5	BLUE
42	Amp 6	BLUE
43	Amp 7	BLUE

Headphone Insert Test

This test verifies that the RV-8 can detect the presence of headphones plugged in to the front panel **Phones** jack.

Setup:

The front panel display should indicate:

“HEADPHN INSERT TEST
HDPhones: OUT”

Test:

1. Insert a 1/4-inch headphone plug into the **Phones** jack on the RV-8 front panel, and verify that the display indicates: “HEADPHN INSERT TEST HDPhones: IN.”
2. Remove the 1/4-inch headphone plug from RV-8 front panel **Phones** jack.
3. Press the **Mode** ◂ button to proceed to the next test.

Temperature Test

This test verifies the temperature measurement circuits in the RV-8.

Test:

1. Verify the display indicates the temperature of Amp1 (**xx** = approximately 30-40 (C):
   "TEMP TEST
   AMP1: xx degC"
2. Rotate the **encoder knob** slowly clockwise and verify that the temperature measurements for Amp2: through Amp7: are within 30-40° (C).

***Note**:*
The temperature is affected by the environment around the RV-8 under test. In a warmer location, the temperature readings will be higher.

Fan Test

This test checks the operation of the internal fans using the encoder knob to select the fan speed and verifies that the speed of the fans increases with each increment of the fan speed indicator. The fans are located at the bottom of the RV-8 chassis. Two fans are on the left side and two are on the right side of the unit.

Setup:

The front panel display should indicate:
"FAN TEST
FAN Speed: 0"

Test:

1. Turn the **encoder knob** slowly clockwise until the display indicates: "FAN Speed: 1"
2. Verify that the fans have started turning.
3. Turn the **encoder knob** slowly clockwise until the display indicates: "FAN Speed: 2"
4. Verify that the speed of the fan speed has increased from previous step.
5. Turn the **encoder knob** slowly clockwise until the display indicates: "FAN Speed: 3"
6. Verify that the speed of the fan speed has increased from previous step.

To verify all four fans are working:

1. Place your fingers under the chassis on the sides and feel for the draw of the fans.
2. Press the **Mode** ◂ button to proceed to the next test.

Diagnostic Tests Completion

When the Diagnostic Tests are complete, the unit will display the test results. Verify the display indicates:

"FUNCTIONAL
TESTS Passed"

DISASSEMBLY INSTRUCTIONS

The following are instructions for disassembling the RV-8 when removal of components is necessary.

WARNING

The amplifier channels may still be charged. Be sure to discharge for safety. See page 4-4 for instructions on discharging amplifier channels.

To remove the top cover:

1. Remove the thirteen screws that hold the top cover of the unit.
2. Carefully slide the cover to the back of the RV-8 and remove.

   Reverse the above procedure when reinstalling the cover.

To remove the bottom cover:

1. Carefully rotate the RV-8 onto its side.
2. Loosen the eight screws (four on each side of the bottom cover).
3. Push the cover towards the front panel and remove from the bottom of the RV-8.

To remove the Power Supply Board:

1. With the RV-8 front panel facing you, locate the power supply module mounted to the inside chassis on the left-hand side of the RV-8.
2. Remove the two wire connectors on the top and bottom of the supply module.
3. Hold the supply with one hand and remove the two screws that hold the supply to the inside chassis.
4. Carefully remove the supply from the RV-8 chassis.
5. Store the module in a static-free area.

To remove the amp channels:

1. For ease of removal of the left 3 channel amp, remove the switching power module first
2. Locate and disconnect the black 6 wire connector and two thin white ribbon cables that run to the main analog board at J18 and J21. Also remove one large thin white ribbon cable on the underside of the amp channel connecting to J22 of the main processor board.
3. Remove the seven screws that hold the channel in place. There are three on the back panel, two on the front end holding it to the main chassis, one in the top, and one on the bottom main chassis.
4. Carefully pull the amp channel to the front panel and lift it free.
5. Store the module in a static-free area.
6. For the right 4 channel amp, locate and disconnect the black 6 wire connector and two thin white ribbon cables that run to the main analog board at J1 and J27. Also remove one large thin white ribbon cable on the underside of the amp channel connecting to J18 of the main processor board.
7. Remove the nine screws that hold the channel in place. There are three on the back panel, two on the front end holding it to the main chassis, one in the top, and three on the bottom main chassis.
8. Carefully pull to the front panel the amp channel and lift it free.

9. Store the module in a static-free area.

To remove the video board:

1. First rotate the RV-8 so the rear panel is facing you.
2. Disconnect the following cables: J18 (the 4 wire power cable) and J20 (the thin white ribbon cable).
3. On the back rear panel remove the four black screws that hold the board in place.
4. Carefully pull the board inward then up and out of the RV-8.
5. Store it in a static-free area.

To remove the analog board:

1. Disconnect the following cable on the analog board and power supply connector: J19.
2. Looking down on to the board, locate the three black screws that hold the board to the center chassis.
3. On the rear panel, remove the fifteen black screws along the row of analog RCA connectors.
4. Carefully pull the board inward then up and out of the RV-8.
5. Store it in a static-free area.

To remove the Main Power Supply Assembly:

Note*:*
To remove the center main power supply, first remove the amp channels.

1. On the top of the main supply assembly disconnect the following cables: J2, 5, 6, 7, 21 and P1.
2. Turn the RV-8 over and remove the ribbon cable J20 that runs to the front panel.
3. Remove the six screws that hold the assembly in place (three on each amp channel side).
4. Carefully grab on to the assembly and pull up, removing it out the bottom of the RV-8 chassis.
5. Store it in a static-free area.

To remove the Tuner/Phono Board:

1. Place the RV-8 upside-down with the rear panel facing you.
2. Locate the Ground Lug and remove it from the rear panel.
3. Grab the Tuner/Phono board assembly and remove the two rear panel screws.
4. Carefully lift the assembly out and disconnect the two ribbon cables at J2 and J4.
5. Lift the assembly out and store it in a static-free area.

Removing the Main Processor Board:

Note*:*
The Tuner/Phono assembly should be removed prior to removing the Main Processor board.

1. Place the RV-8 upside down with the rear panel facing you.
2. Locate and disconnect the following power and ribbon cables: J20, 2, 23, 24, 26, 27, 29, 31,and 32
3. Locate and remove the four screws that hold the Main board to the chassis.
4. On the rear panel of the RV-8 locate the screws and other fasteners that hold the Main board to the rear panel.

5. Carefully slide the Main board to the front of the RV-8 and up and out of the chassis.
6. Store it in a static-free area.

To remove the front panel:

1. Place the RV-8 upside down with the front panel facing you.
2. Locate and remove the two screws and ribbon cable J20 and disconnect it from the Main board.
3. Turn the RV-8 over. Locate and remove the two screws holding the front panel to the chassis.
4. Carefully pull the front panel away from the chassis and store it in a static-free area.

CHAPTER 6 – THEORY OF OPERATION

RV-8 AMPLIFIER THEORY

The RV-8 amplifier sections are designed using the most advanced linear power technology available. Using this technology allows maximum amplifier performance under the most demanding and extreme conditions.

In the RV-8 there are two amplifier modules. One module consists of three amplifier channels and the other consists of four amplifier channels. Each individual channel is identical schematically, but not identical in the way they are laid out.

For this portion of the theory, only one channel will be referenced since all channels are the same schematically. All references correspond to the SIDE RIGHT (Channel 2) channel on the four-channel module.

Features:

- Full-complementary output topology
- High performance error amplifier to provide extremely low THD
- Ultra high 140V rails to maximize dynamics
- Critical protection circuits local to each amp channel

Input Stage

Op amp U1-A (MC33078) is used to set up a conventional balanced to single-ended conversion stage. The overall gain of this stage is approximately –6 (15.6dB), which is set by R2 (2.49k), R4 (2.49k), R3 (15k), and R5 (15k). C1 (22pF) provides high-frequency feedback.

Power Amplifier Overall Gain

For this portion of the theory, consider the power amplifier as one large op amp. The output of U1-A (MC33078) feeds a single ended audio signal into the power amplifier. The power amplifier is set up as a conventional inverting amplifier. The gain of this stage is approximately –10 (20dB), which is set by R7 (2.49k), R9 (2.49k), and R10 (49.9k).

Bias

Bias is set by R14 (9.09k), R17 (9.09k), R15 (825), and R16 (825). This causes a small equal current to flow through R19 (825) and R29 (825) via steering diodes D4 (1N914) and D7 (1N914). R19 drives Q5 (MPSW92) and Q6 (MPSW92), while R29 drives Q9 (MPSW42) and Q10 (MPSW42). These four transistors also serve as voltage translators. Emitter resistors R20 (95.3), R21 (95.3), R30 (95.3), and R31 (95.3) set a current used to bias Q8 (MMBT3904). R84 (1k potentiometer) is then used to precisely tune the bias level to a point where output devices are just out of conduction. This provides the AB+B mode of operation for the output stage. Bias voltage is measured across R25 (30) and is set to 0.350Vdc ± 0.01 @ 25 degrees ambient.

Amplifier Operation

At the heart of the amplifier is a high performance error amplifier (U2 - TLE2037). From the error amp audio signals move through the voltage translators and on to Q7 (MJE15032) and Q11 (MJE15033). Q7 and Q11 form current gain cells, which feed the paralleled main output devices (MJ21194 NPN, MJ21193 PNP). The main output devices are connected in an emitter follower configuration. The devices are mounted directly to the heatsinks with no insulator, which means the heatsinks are at rail potential (±70Vdc).

Frequency Response

The frequency response of the amp module is set by several components. The dominant pole of the amplifier is set by R10 and C5 at approximately 145kHz. All of the stages prior to the power amplifier stage also contribute to the high frequency roll off of the amplifier.

Amplifier Feedback

Resistor R12 (47.5) and capacitor C8 (22pF) provide a local high-frequency roll off for the error amp. The error amp also receives split feedback signals from two points at the output. C23 (0.33uF) provides high frequency feedback through the output inductor L1 (1.5uH) while R58 (107) provides low frequency feedback, which negates the DC resistance effects of the output inductor. R10 and C5 provide overall feedback for the amplifier.

Time Dependent VI Limiting

For simplicity the positive side current limit is described below. The negative side current limit operates in a similar fashion.

Current Limiting

The output current of the amplifier is sensed across emitter resistors R26 (0.68), R27 (0.68), R169 (0.68), and R173 (0.68). This information is summed via R342 (23.2k) and R343 (23.2k) then divided down by R344 (1.82k) and R345 (100k). The divided voltage information is fed into the base of Q77 (KST5089). Once the voltage across R344 and R345 reaches approximately 0.65Vdc, Q77 turns on which causes Q79 (MMBT3906) to turn on as well. This redirects current coming from Q5 and Q6 through D12 (1N914) and Q79 to the output, thus limiting the amount of current driven into the base of Q7.

Time Dependency

C157 (4.7uF) provides time dependency to the current limit. When no current is flowing through the emitter resistors, C157 has no charge. When current suddenly flows through the emitter resistors, C157 is seen basically as a short, which essentially eliminates R345 from the limiting circuitry. As C157 charges the current is limited more and more until it reaches a steady state.

Voltage Information

D1 (1N914) and R129 (365k) provide the voltage information to the circuitry. As the output voltage of the amplifier increases, more current is pulled through R342, R343, R344, and R345 causing the voltage differential across pins 1 and 2 of Q77 to decrease. At the same time, D1 and R129 also pull charge out of C157, which stretches the time dependency of the limiter.

Other Protection

D14 (ES2GTR) and D15 (ES2GTR) are fly back diodes that steer reactive energy returned from the load around the current gain cells and back into the power supply. D5 (RLS245) and D10 (RLS245) limit collector voltages on the MPSW42's and MPSW92's, thus reducing cross conduction currents under high current/high frequency conditions.

Clip

The clip signal is derived from the output signal of the error amp. This signal is called V_ERR on the schematic. V_ERR is fed into a window comparator set up by U4-A (LM339D) and U4-B. When the signal coming out of the error amp exceeds ±12.5Vdc it triggers the window comparator. The output of this stage is sent into another comparator stage set up by U4-C. The output of U4-C feeds a RC circuit (R75, R76, and C31) that can be used to change the point at which a clip signal is indicated (in this case the C is not populated so it is not being used). The output of the RC circuit feeds a fourth comparator stage set up by U4-D. This comparator drives the clip signal. The clip signal is normally at 0Vdc and goes to +5Vdc when a clip occurs.

Temperature Sensing

An NTC is thermally coupled to the negative heatsink for every amp channel. As the temperature of the heatsink increases, so does the value of the temperature signal. At room temperature the temp signal usually reads in the range of approximately 0.5 to 0.6Vdc.

DCLF

The card is also protected from DC signals and Low Frequency (LF) signals. The output is monitored and will open the relay if either of these conditions exists. The relay will stay off for a few seconds and will try to turn back on. If a DC or LF signal still appears at the output the relay will either turn off again or not turn on at all. This cycle will repeat until a DC or LF signal is no longer present at the output.

The output of the amplifier is fed into a low-pass filter set up by R46 (200k), C23 (0.47uF), R47 (2.2k), and C24 (0.1uF). The output of the filter is sent into a window comparator set up by U3-A (LM393D) and U3-B. When the window comparator is triggered it turns on Q15 (MMBT3906), which then turns off Q16 (MMBT3904) and consequently turns of the output relay (K1).

RDY_CON

This is an input signal to each amp channel that is used to turn on and off the output relay. A 0Vdc input or no input will keep the relay off. A 5Vdc input signal will turn the output relay on if a DC or LF signal is not present at the output of the amplifier.

RDY_MON

This is an output signal of the amp card. The only function of the RDY_MON signal is to report the status of the output relay. A 0Vdc signal means the relay is open and a 5Vdc signal means the relay is closed.

RV-8 ANALOG BOARD THEORY

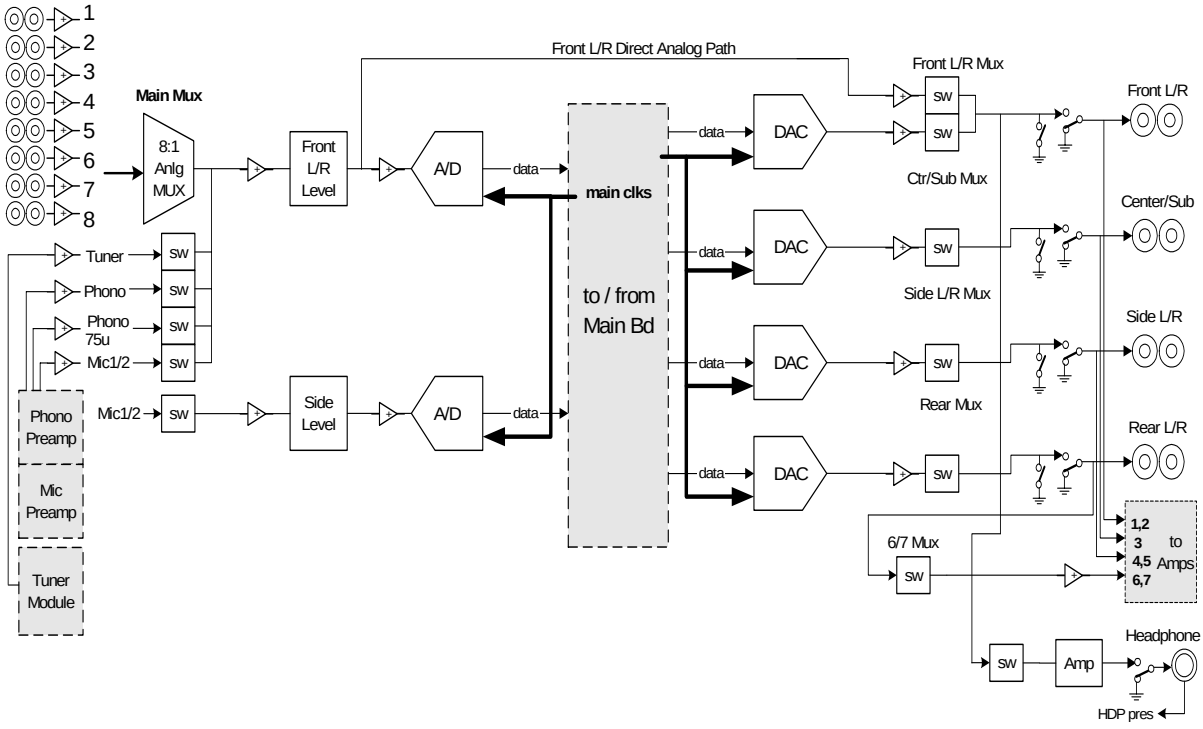
The analog board of the RV-8 encompasses all of the analog audio inputs and outputs, level controls and A/D and D/A converters. This board is located below the RV-8 Video Board.

There are three separate signal paths: Main, Zone2 and Zone3. Each of the eight analog stereo inputs, the tuner, the phono, or any of eight digital inputs can be routed to any of the three paths. The schematics refer to Main, Rec, and Zone. Rec is named for Zone2 and Zone is named for Zone3 on the back panel.

Main Audio Paths

One of the eight analog stereo inputs, the tuner, or the phono can be routed to the main path and to the A/D convertor(s). In addition, one of the eight digital inputs can be routed from the main board. The A/D digitizes the analog signal (if selected) and passes it to the DSP on the main board. Digital signals from the main board pass directly to the DSP. *(Refer to the Main Audio Paths 2-Channel Input block diagram below)*. The DSP creates eight different output signals from the 2-channel input. D/A converter IC's convert each of the eight signals from the DSP to analog and then send them to their respective RCA connectors. The outputs are also sent to the seven channels of amplification, with channels 6 and 7 having the ability to be redirected. A direct analog path is provided which passes a 2-channel analog input signal directly to the Left and Right Front outputs via the level controls, bypassing the DSP and converters.

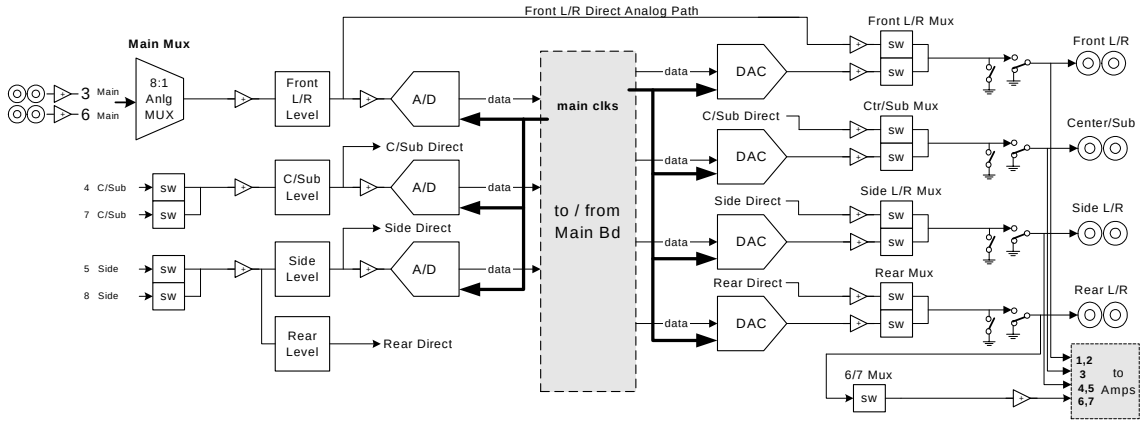
Main Audio Paths 2-Channel Input



In addition, a 5.1-channel source can be selected for the Main audio path. There are two possible methods of getting a 5.1 source into the box. Refer to the Main Audio Paths 5.1-Channel Input block diagram on the next page)

1. An S/PDIF signal may be encoded in Dolby Digital or DTS format and pass through a decoder that outputs the 5.1-channels. These channels are then passed along to the DSP and sent to the analog board.
2. Two sets of three separate analog input pairs can be routed directly to the outputs, bypassing the DSP and converters. This mode is available for DVD-Audio and multi-channel SACD players with 5.1-analog outputs. In the first case, Input 3 would pass to the Left and Right Front outputs, Input 4 would pass to the Center and Subwoofer outputs. Input 5 would pass to the Left and Right Side and Rear outputs. A duplicate set uses inputs 6,7, and 8 in a similar manner.

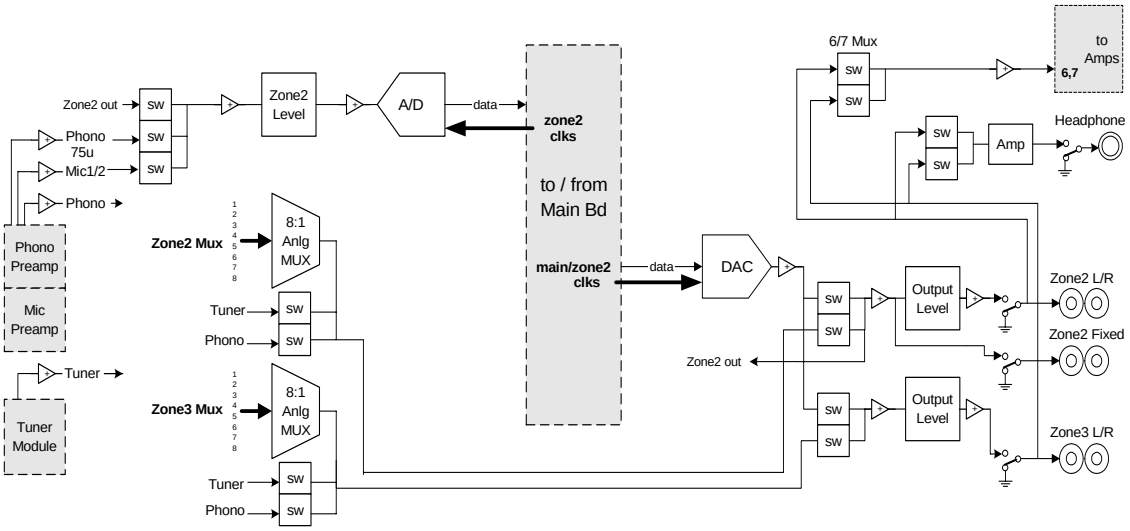
Main Audio Paths 5.1-Channel Input



Zone2 and Zone3 Audio Paths

Any of the ten analog or eight digital audio inputs can also be selected as the source for the Zone2 and Zone3 audio paths. Refer to the Zone2 and Zone3 Audio Paths block diagram below. An analog source can be passed directly to the analog outputs. Likewise, a digital source can be routed to a D/A converter for the analog outputs. In addition, a 5.1 Dolby Digital or DTS encoded 5.1 digital source may also be selected and passed through a decoder which will output a 2-channel downmix for the Zone2 outputs.

Zone2 and Zone3 Audio Paths



SCHEMATIC WALKTHROUGH

Analog Audio Inputs (sheets 1,2 & 3)

Sheets 1 and 2 are identical. The Left input jacks and associated circuitry are on sheet 1 while sheet 2 includes the Right input jacks and circuitry. Each input pair is buffered by a dual TL072 op amp. Each buffer connects to three DG408 8x1 CMOS switches. There are separate switches for the Main and Zone2/3 analog source selection with independent switches for left and right channels, for a total of six DG408s.

At the bottom right-hand corner of each sheet is a quad-switch. These switches are used when routing a 5.1-analog source. One routes the Center and Subwoofer signals from Inputs 4 or 7 while the other buffers the Surround L/R signals from Input 5 or 8.

Sheet 3 hold buffering and switches for tuner and phono, and buffering for phono75, and mic1/2. Three sets of switches are used to select inputs for each zone separately. These switches work in parallel with the muxes on sheets 1 and 2 to provide a 1-of-10 analog input mux function for each zone.

Main Inputs, C/Sub and Side Inputs (sheets 4,5,6 & 7)

The outputs of the Main source selectors feed the Main Input Level control on sheet 4. A dual op amp on sheet 4 buffers a 6dB voltage divider that feeds the level control. The output of the level control is used for the direct analog path to the Front L/R outputs and feeds the A/D converter.

Two microphone inputs are provided from the microphone preamplifiers. A DG411 analog switch can select Mic inputs 1 and 2 or the phono75 to be passed to the Main Input level control and A/D converter. These switches work in parallel with the muxes on sheets 1 and 2 to provide a 1-of-12 analog input function. When the Mic input is selected, the Analog inputs are disabled by bringing MAIN_ANLG_EN low on sheets 1 and 2.

The Main Input level control is the PGA2311, which has a range from +31.5 to –95.5 dB in 0.5 dB steps. The PGA2311 operates on ±5 volt rails and cannot handle signal levels greater than 7.5 Vpp. Two dual op amps provide the left and right differential audio signals to the A/D converter. The op amp circuits bias the signals at 2.5 V and attenuate it by 7dB. This means a 2 Vrms signal at the output of the level control will be equivalent to 0 dBFS after the A/D conversion.

The PCM1804 stereo A/D converter incorporates a multi-bit delta-sigma architecture. It outputs 24-bits at a 96kHz sample rate under normal operation. The serial audio data from the A/D converter goes directly to the Main board. Control signals are used for reset (MAIN_ADC_RST/) and to place the converter in 88.2k/96k or 192k sample rate mode (MAIN_ADC_96K_EN and MAIN_ADC_192K_EN). The main board provides three clocks: MAIN_ADC_MCKI/, which is 256xFS for 44.1k and 48k sample rates, 128xFS for 88.2k and 96k sample rates and 64xFS for 192k; MAIN_FS64/, which is 64xFS; and MAIN_FS/ which is 1xFS (where FS = sample rate).

Sheets 5, 6 and 7 cover the C/Sub, Side and Rec A/D channels. They are similar to the main zone except for various analog source differences and separate clock sources and data outputs.

Rec & Zone D/A converter (sheet 8)

The AK4395 24-bit delta-sigma stereo D/A converter operates up to 192kHz. The DAC is configured through its serial control port (pins 8,10,11) with a separate Reset pin.

The output of the DAC passes through a second order low-pass filter with its –3dB frequency at 187kHz. The filter topology is a compromise between the flat pass-band Butterworth filter and the Bessel filter with its superb transient response. The filter is flat out to 20kHz. It has an overall gain of 6.7dB when measured at the test points. This means a 0 dBFS signal at the D/A converter will be 4 Vrms going into the analog switches.

DG411 analog switches select either the output of the Rec/Zone DAC or the Rec analog input source directly. The selected signal goes to the dual op amp U32 which buffers a 6dB voltage divider that feeds the level control. The PGA2311 output level control is buffered by a 6dB gain driver. A direct path around the level control provides a fixed output. Rec analog output has a maximum output level of 4 Vrms. The signal passes through a muting relay on the way to the output jacks. The relays are controlled by the ZONE_MUTE_RLY/ signal.

Zone Level Control (sheet 9)

U63 serves as a direct bypass level control for the rear channels. The input comes from the side channels in the 5.1 direct bypass path.

The rest of the circuitry, U44, U33, U23 and U15 are similar to the Rec path (page 8). Zone analog output has a maximum output level of 4 Vrms.

Main D/A Converters (sheets 10-13)

There are eight outputs for the Main Audio Path. The D/A circuitry is shown for two outputs on each sheet. The circuitry is identical for all eight outputs.

The AK4395 is the same 24-bit D/A converter that operates Zone2. The AK4395 DACs are configured through their serial ports (pins 8,10,11). MAIN_DAC_RST/ puts the pairs of DACs into reset.

The DACs are followed by a 2nd order low-pass filter. The filter topology is a flat pass-band Butterworth filter with the –3 dB point at 127kHz and a pass-band flat to 20kHz. The filter amplifies the 1.7Vrms differential signal to 7Vrms (+11.2 dB) and converts it to single-ended for the level controls. Note these values assume a 0 dBFS digital input signal to the DAC.

ADG451 analog switches are used to select either the DAC output or analog input for the respective output. These direct analog signal paths have been designed to support two modes:

- 2-channel analog direct or bypass mode. Any analog input can be routed directly to the L/R Front outputs.
- 5.1-channel analog direct or bypass mode. When this mode is enabled, specific analog input signals are routed to specific analog outputs according to the table below:

Analog Input	Analog Output(s)
#3 or 6, left channel	Left Front
#3 or 6, right channel	Right Front
#4 or 7, left channel	Center
#4 or 7, right channel	Sub
#5 or 8, left channel	Left Side and Left Rear
#5 or 8, right channel	Right Side and Right Rear

Two different pairs of control bits are used to select the DSP/DAC signals or analog input signals for the Main outputs. MAIN_DACOUT_SEL/ selects the respective DAC outputs for all of the Main outputs (Front

L/R, Center, Sub, L/R Side, L/R Rear) whereas MAIN_DIRECT_SEL/ selects the 5.1-analog inputs directly. The rear channels are switched with separate controls REAR_DACOUT_SEL/ and REAR_DIRECT_SEL/.

The output from the analog switch goes to a –6dB level shifter and ADG451 output mute switch. The outputs pass through DC-blocking caps and relays before going to the RCA connectors. The relays mute the Main outputs during a power cycle and whenever the unit is in Standby or powered off. The relays are controlled by the MAIN_MUTE_RLY/ signal.

Control Registers (sheet 14)

A Xilinx CPLD hold the control registers for the board. The main board writes to them via a SPI data bus (ADA_SCLK, ADA_SDATA_OUT, ADA_LATCH). Their function is loosely related to the function and numbering of the MC-12 registers. The control register output bits provide relay control, 5.1 direct mux selection, analog source selection, A/D control, DAC reset control, output selection, independent zero crossing enable and mute for inputs and outputs.

Three-bits of data are returned to the main board through the SPI port (HEADP_PRES, TUN_TUNED, TUN_STEREO). A serial stream from the tuner for status and RDS data is also available (TUN_SDATA_OUT).

Amp Select and I/O Connectors (sheet 15)

The Main Board Digital connector is the source for the clocks and data for the A/D and D/A converters. The MCLK is at 256x the sample rate (FS). Each converter gets MCLK through a separate buffer and source resistor. The SCLK (64xFS) and LRCK (1xFS) are distributed directly to the DACs. All of the D/A converters operate in I^2S mode. J20 and J22 provide a row of test points for quick access to all the clocks.

J23 and J24 are ribbon connectors from the Mic/Phono Board and Tuner board respectively. The left and right signal pairs are buffered differentially and presented to the input muxes through these connectors. The tuner is controlled through the SPI port signals ADA_TUNER_CE/, ADA_SDATA_OUT, and TUN_SCLK.

Power Supply Connections and Regulators (sheet 16)

There is a separate feed from the switching power supply to the Analog board. The Analog board has a 4-pin connector that accepts ±15 volts, +5 volts and a ground connection to the supply. The –15 supply is a shared daisy chain connection from the supply to the analog and video boards.

Three regulators generate +12V for the tuner, +3.3VD for the convertors and CPLD, and –5VA for the volume controls and convertors. Heat generated by the –5V regulator is dissipated by a heatsink. Two voltage regulators create the +5VR supply from the +15V rail. The first regulator regulates to about 10V and the second regulates to 5V. +5VR is an alternative "clean" 5 volt supply used by the A/D and D/A converters.

Six DG411 switches select either front L/R or either of the two zones as a source for the headphones. A high current op-amp with 12dB of gain drives the headphone output at J25. A high impedance headphone presence detector is shunted to relay ground or the 10K output impedance by a normalling switch in the socket, and is pulled high when a jack is inserted.

RV-8 MAIN BOARD THEORY

This section provides a detailed description of the design theory embodied in the RV-8 Main Board. Each section of this document will discuss the theory of each functional subset of this board and will reference a schematic sheet for each block. The schematic set being referenced is at a minimum revision level of 6.

The RV-8 Main Board incorporates the following features:

- Command and control of the entire RV-8 system
- Digital audio inter-system routing via FPGA
- Front Panel display control, button monitoring, and LED display control
- Two expansion ports
- Amplifier environmental and power monitoring and control
- User and debug access via two RS-232 serial ports
- Four coaxial and four optical S/PDIF input ports
- One coaxial and one optical S/PDIF Record Zone output
- One Composite Video Zone 3 output
- Two remote power outputs
- Two Phase Locked Voltage Controlled Oscillators for master audio clock generation
- IR remote control sensing and discrimination from the front panel and Zone Two
- “Canned” Algorithm Surround Processing via a single Crystal Semiconductors DSP engine
- Lexicon specific supplemental DSP via two Analog Devices SHARC DSP engines.

START-UP CONDITIONS

Power On and Boot Procedure

Once the unit is powered up, the reset generator U31 provides both active low and active high reset signals of approximately 3ms duration. During this interval, the CPU processor (U33) is held in an inactive state as well as the three DSP engines, and the FPGA. This reset is also passed along to all of the remaining boards in the system. Once this reset interval has passed, the processor and FPGA are ready for further instruction. The DSP engines remain in reset, however, and are not released from this state until commanded by the system software. The CPU then begins booting from the on-board 1Mx16 Flash, U26. Diagnostic testing is run on the on-board DRAM (U42). If the test passes, test LED D10 will light; it will flash if the test fails. The bulk of the boot and application software is then loaded from the Flash into this DRAM and a checksum test is performed. If this test passes, test LED D11 will light, flash if the test fails. Internal registers of the processor device are then configured. These include the following:

- Bus State Controller
- Wait State Controller
- DRAM Configuration (the default conditions are now replaced with optimized settings)
- Serial Communication Ports 1 and 2
- Pin Function Control
- General Purpose I/O.

The processor then checks the status of PE[3:1] (88:86) to determine which start-up configuration has been chosen by the user. If these port pins read as all low, then the processor continues with the normal boot procedure.

The Serial port UARTs are now tested, and if the test passes LED D12 will light, flash if the test fails. The FPGA (U41) is now programmed. If the operation is successful, LED D13 will light, flash if the operation fails. If all of these steps are completed successfully, LED D10 will dimly glow. This is due to the LED being driven with a 4mS square wave. All through these tests, progress may be monitored via a hyperterminal monitor connected to serial port 0. If a problem exists with this serial connection, LED D11 will light.

Diagnostics continue by testing the Character RAM on the front panel Vacuum-Fluorescent Display. Connection integrity to the Video Board, Analog I/O Board, AM/FM Tuner Module, and Amplifier SPI ports is tested as well. The FPGA status is checked by polling it's internal ID register. The Format DSP (U25) is now taken out of reset and its associated Flash device (U19) is tested. The algorithm DSP devices (U16 and U34) are taken out of reset and loaded with algorithm code. Status is monitored by polling the internal registers of the DSP devices.

Connection to the amplifiers is tested by serially shifting a single bit up to the amplifiers via the SPI ports, and then monitoring its return. Power is then briefly applied via the Soft Start Relay, which applies a current limited full scale voltage to the amp rails. If a problem exists with the amplifier power supply, as indicated by either the status read back from the SPI ports or by the Brown Out Interrupt, power is immediately removed and status is indicated on the hyperterminal monitor. If everything checks out, then the Mains Relay is activated, and the Soft Start Relay is de-activated. The hyperterminal will indicate that the unit is now ready.

Host Processor (Sheet 1)

This page contains the embedded CPU and its associated DRAM and flash memory for storage of the boot mode and system control software. In addition, provisions are in place for a separate boot flash memory and emulator support during software development.

Processor (U33)

The processor is a Hitachi SH7014 single chip RISC. This device implements all system control via a 16-bit wide data bus over 8Mwords of address space. This address map is split into four chip select areas (CS[3:0]) of 2Mwords each. The processor is pre-configured by four mode pins MD[3:0] which are hard coded via zero ohm resistors to a value of 1001 (binary). This establishes that the CS0 memory space (the memory boot space) is 16-bits wide, and that the on-chip PLL is operating in 4X mode. The processor runs from a 6.25MHz clock, supplied by a CPLD device (see schematic sheet 7) into the EXTAL pin (74). With 4X PLL operation, the internal bus of the processor runs at 25MHz. This clock is sourced to the rest of the system via the PA15_CK pin (83). The PLL is biased and noise filtered by an external network comprised of R125, R126, C120, and C121.

Serial Ports

Signals: DEBUG_RXD, DEBUG_TXD, USER_RXD, USER_TXD

The CPU provides two asynchronous serial ports which are used as a debug port and as a user port. The debug port is implemented by PA0_RXD0 (51) and PA1_TXD0 (50). Connecting a hyperterminal to this port grants the user access to the debugging and register editing tools built into the boot code. During the boot phase, each step of the process is echoed to the terminal via this debug port as well as any initialization failures that may occur. The debugger allows the user to manually change register values within the CPU and each of the peripheral devices attached to the host. It will also allow the running of configuration scripts to test various functions and features included in the RV-8. Re-programming the system FLASH is also called into service via the debugger.

The user port is implemented by PA3_RXD1 (48) and PA4_TXD1 (47). Connecting an HDI emulated hyperterminal to this port allows access to the system software at the code level. This port is also used to download new code to the FLASH device.

Serial Port Settings

Each serial port must be set to the following protocols in order to work properly with hyperterminal connections:

- 19200 Bits Per Second
- 8 Bits
- Odd Parity
- 1 Stop Bit
- Flow Control set to None

Interrupts

Signals: BROWN_OUT, CPU_CRYIRQ/, CPU_DSPABIRQ/, CPU_KYBDIRQ/, CPU_VIDTUNIRQ/

The CPU has provisions for six interrupt sources, of which five are used. The highest priority interrupt is the Non-Maskable Interrupt NMI (76). This interrupt monitors the status of the amplifier power supply. If the voltage rails should drop by more than 10%, as would happen during brown out conditions, the interrupt is triggered, and the unit goes into standby mode. This is the BROWN_OUT interrupt. Ferrite bead FB14 suppresses spurious signals that may falsely trigger an NMI.

The next level of interrupt is implemented within the IRQ0 (49) domain. This interrupt is dedicated to monitoring the status for the front panel pushbutton array. An interrupt is generated when the button is pressed, and a second one when it is released. This is CPU_KYBDIRQ/.

IRQ1 (46) is currently unused. It may be used as an interrupt source monitor or a general purpose I/O in the future.

IRQ2 (43) monitors the status of the SPI port transfers to and from the algorithm DSPs. Currently this interrupt is masked off by the system software, but it remains as a provision. This is CPU_DSPABIRQ/.

IRQ3 (42) monitors the status of INTREQ or'ed with FINTREQ from the output steering DSP (U25). Each indicates out-going data from the DSP sub-modules within this chip that must be read by the host processor. This is CPU_CRYIRQ/.

IRQ[4:5] are internal interrupts. They are not utilized outside of the CPU.

IRQ6 (31) is a shared resource with the CPU address bit 20. As such, it is not available for use.

IRQ7 (32) monitors interrupts from the Video Board and from the Tuner Module. This is CPU_VIDTUNIRQ/.

FPGA Configuration

Signals: FPGA_INIT/, FPGA_PROG/, FPGA_DONE, FPGA_SDATA, FPGA_CCLK

The FPGA is programmed during the boot phase. This is accomplished by serially loading the device with the appropriate code. The process begins when the CPU asserts FPGA_PROG/ low on port **PE6** (104). In response, the FPGA asserts FPGA_INIT/ low; the CPU monitors **PE5** (102) for status of this signal. The configuration memory inside the FPGA is automatically cleared. Once this is done, the FPGA asserts FPGA_INIT/ high. Once the CPU receives this response, the loading of configuration data begins.

Configuration data FPGA_SDATA is sourced from the **PB13** (112) port of the CPU along with the serial clock FPGA_CCLK from the **PE15** (2) port. Data is clocked into the FPGA on the rising edge of this clock. When this process is complete, the FPGA asserts the signal FPGA_DONE to a high state, monitored by the CPU on port **PE7** (105). It should be noted that LED D46 lights when this signal goes high. The CPU may continue with the remainder of the boot phase upon receipt of the FPGA_DONE signal.

Amplifier Environment Monitor and Control

Signals: FAN_DRV, TEMP[7:1], AC_MON

The CPU incorporates eight 10-bit A/D Converters of which seven are used to monitor the temperature of the amplifier heatsinks. This is accomplished by monitoring the analog voltages present on the TEMP[7:1] signal lines connected to the **AN[6:0]** ports of the CPU (98:91). These voltages are provided via thermistors placed in direct contact with the heatsink metal. Each thermistor is part of a voltage divider the output of which is converted to a 10-bit value by each converter. The output value of the converters are directly proportional to this voltage, and hence to the temperature of the heatsink. The entire spectrum of voltages is separated into four heat categories. From these temperature values, the software determines how fast or slow the heatsink fans are to run. Under extreme heating conditions, the CPU protects the amplifiers from thermal runaway by placing the entire system into standby mode.

The processor incorporates four Multi-Function Timer Units that may be used to generate timing oriented waveforms or as interval/event counters. Two are used in this implementation. Timer 1 generates a PWM signal that is used to control environment fans. The FAN_DRV signal is sourced from the **TIOC1A** port (89) of the CPU. As the heatsink temperature increases beyond each heat category, this PWM signal shrinks in duty cycle in order to increase the fan speed. This methodology was embraced to keep fan noise to a minimum while the unit is in operation.

AC_MON is a provision for monitoring the transformer secondary voltage from the amplifier power supply via the **AN7** A/D Converter port (99). It is currently not used.

Front Panel Boot Level Monitoring and Control

Signals: OVLED, SYSLED, FP_IR_ACK, FPSWITCH[3:1]

The user has the option of starting the RV-8 into three modes:

- Normal start-up (default)
- AMON
- Diagnostics

The processor monitors PE port bits 1 through 3 during the earliest stages of boot, which are connected to signals FPSWITCH[3:1]. The following button map applies:

- FPSWITCH1 – Right Mode
- FPSWITCH2 – Zone 2 DVD2
- FPSWITCH3 – Zone 3 DVD2

When a high is read on any of these port pins, it indicates that a button is being pressed and held. The table on the next page illustrates the button combinations and their associated modes. These combinations must be pressed and held during power up.

Buttons and Associated Modes

START UP MODES				
Right Mode	Zone 2 DVD2	Zone 3 DVD 2	Mode	Description
-	-	-	Normal	Boot Process executes uninterrupted
*	*	-	AMON	Allows the loading of new code without re-flashing storage RAM
-	*	*	Diagnostics	Places unit into diag mode, allowing individual testing of functionality

Behind the display window are three LEDs that are driven directly from the processor. These LEDs are driven via the **PE[10:12]** port (108, 110, 111). When these port pins are high, the associated LED lights. The following table illustrates their functionality.

DISPLAY LED INDICATORS		
PORT BIT	**SIGNAL NAME**	**FUNCTION**
PE10	FP_IR_ACK	Yellow LED indicating infra-red remote access
PE11	SYSLED	Blue LED indicating unit is on and functional
PE12	OVLED	Red LED indicating clipping on an audio input

Miscellaneous Peripheral Control

Signals: CPU_WRD_CLK_MON, FLBY/

Timer Channel 0 is used as an interval counter that monitors the period of FSCLK from both the Main Zone and Zone 2. The FPGA Multiplexes each clock signal into the **TIOC0A** port (85) as signal CPU_WRD_CLK_MON. With each rising edge of FSCLK, the event timer is restarted and the period is verified by count value.

FLBY/ is output from the storage FLASHRAM (U26) to indicate that the device is busy either during an erase or re-programming operation. The processor device monitors this signal via the **PE14** port (1). When the signal is low, the FLASHRAM is not ready for read accesses. When high, the device may be accessed as normal.

DRAM (U42)

The DRAM used in this product is a standard 70nS 1Mx16 Fast Page Mode device (U42). The processor executes all software instructions from this device, except for the earliest phases of boot up. After DRAM testing has passed, all of the system code that resides in the FLASHRAM is migrated to the DRAM for execution. The data bus from the CPU is one word wide, as mandated by the fact that all instructions are word length. As all accesses are word wide, the address bus to the DRAM is oriented on word boundaries, hence the 10-bit address beginning at CPUADDR1 instead of CPUADDR0.

Boot Mode Jumper Selection

The RV-8 supports multiple booting options to aid in software development. In the final product, only one of these modes is available, booting from FLASH, as described on page 6-15. For development, booting may be accomplished from either the EEPROM or the ROMulator by proper jumper selection, as

implemented in **W3**, **W4**, and **W5**. The following table illustrates the various modes available to the developer.

Boot Mode Jumper Configuration			
W3	**W4**	**W5**	**Usage**
Uninstalled	1-2	Uninstalled	Default; Boot and Program Run from FLASH
Open	2 - 3	1 - 2	Boot from EEPROM, FLASH Program Run
Open	Open	2 - 3	Boot and Program Run from ROMulator
Open	2 - 3	2 - 3	Boot from ROMulator, Program Run from FLASH
1 - 2	1 - 2	Open	EEPROM Boot, Program Run from ROMulator

FLASH (U26)

The FLASH RAM used in this product is a 1Mx16 120nS device. There is a sector of memory of 16Kwords available at the bottom of the memory array. This is intended for use as a boot sector, and can be write protected to prevent erasure when updates to the system or algorithm software are being programmed. This write protect is enforced or disabled by the state of the **WP/** pin (14). This pin is under software control by the CPU. When this pin is low, protection is enforced. When high, the boot sector may be erased and re-programmed.

The **RYBY/** pin (15) is an output flag of the internal status of the device. When this pin is low, it indicates that the Flash is in the middle of an erase or programming cycle (busy). When this pin returns to a high state, it indicates that the operation at hand has been completed and the device contents may be read in the same manner as an EEPROM. The **WE/** (11), **CE/** (26), and **OE/** (28) have the same function as those on an EEPROM.

Erasure or in-circuit programming is accomplished by executing the erase or program command sequence. These sequences initiate the proper embedded algorithm that ensures proper execution of the desired command.

The **RESET/** pin (12) is tied to the system level power-on reset. When this pin is low, it suspends any operation that is in progress, and resets the internal state machines to reading array data. During power-up, the internal state machines are set up in this manner.

The **BYTE/** pin (47) is pulled high to configure the Flash as a word mode device.

The CPU fetches its start-up instructions from the boot sector of this device. Once boot-up is complete, all system control and DSP algorithm code is accessed from here as well. Under normal operating circumstances, CS0/ from the CPU controls the CE/ pin of this device. This signal is labeled **BOOTCS/**, and it is routed to the FLASH device by jumpering pins 1 and 2 on W4. During code development cycles, CS1/ from the CPU is routed to the CE/ pin by jumpering pins 2 and 3 on W4. In this case, the chip select signal is labeled **PROGCS/**. All code outside of low level booting may be executed from the memory space occupied by CS1/. R88 acts as a pull-up for the FLASH CE/ pin.

EEPROM (U32)

The EEPROM is a 64Kx16 1Mbit device that serves as the primary boot code source during software development. The **WE/** pin (43) is pulled high by R160 to prevent inadvertent write cycles to the device that would corrupt the resident code. The **BOOTCS/** signal is routed to the **CE/** pin (3) by placing a jumper plug between pins 1 and 2 on W5. R187 serves as a default pull-up resistor. This device is not

used in the released version of this product, and therefore is installed during software development cycles only.

Emulator Support (J14)

The Emulator socket is designed to accept a 40-position emulator pod for boot code development. When the pod is in place, it acts exactly like the EEPROM mentioned above. The **BOOTCS/** signal is routed to the chip enable pin by placing a jumper plug between pins 2 and 3 on W5. This device is not used in the released version of this product, and therefore is installed during software development cycles only.

Reset Generator (U31)

The Reset Generator provides reliable one-shot pulses of both polarities to various components on the Main Board and to all off-board peripheral devices that are required to initialize to a known state when power is first applied. These pulses are approximately 3mS in duration, from the time that power is first applied. The time constant is set by the value of C116, and is determined by the equation:

$T_D = (2.6 \times 10^{4}) \times C112$

Where: T_D is in seconds, C112 is in Farads.

Resistor R111 serves to eliminate false triggering of the output pulse by limiting the current flowing into the **CT** pin (3). This impacts the T_D value minimally, by slowing the rise time of the output pulse. Generally, this is not critical, and therefore can be ignored. R110 provides a default pull-up of the **RESIN/** pin (2), thereby enabling the reset circuit to work as intended. A test point (E6) has been provided so that manual triggering of the reset may be accomplished by connecting the test point to ground momentarily. This saves the trouble of having to power cycle the entire unit. C111 provides high frequency filtering of the internal voltage reference at the **REF** pin (1). R113 provides a default pull-up for the **RESET/** pin (5) while R112 provides a default pull-down of the **RESET** pin (7). C114 is a standard power supply decoupling capacitor.

Buffers, Level Shifters (Sheet 2)

This sheet contains a set of external registers for software control of certain external resources, as well as level shifters interfacing the 5V and 3.3V domains.

Level Shifters (U36 and U37)

U37 is a bidirectional transceiver hardwired for signal flow from the A ports to the B ports. Signals originating from the 3.3V domain are given a shift in level, making them compatible with the CMOS 5 volt threshold of the CPU input pins. Five of the interrupt sources discussed in the previous section are sourced from the FPGA directly to the processor after undergoing level shifting. U36 performs a similar function with a byte wide data bus between the FPGA and the CPU. It should be noted that the FPGA is 5 volt tolerant on all of it's I/O, and therefore needs not to have any 5V level signals attenuated to 3.3V. When a memory access is made to the CS2/ space of the CPU, U36 is taken out of tristate and becomes active. The BUFDIR signal as generated by the FPGA controls the direction flow of this device, that is to say signal flow is from the CPU to the FPGA during write cycles, and from the FPGA to the CPU during read cycles.

External Registers (U20 and U21)

U20 and U21 are octal D-flops that provide software control for the following:

- Resets to the DSP engines
- Resets to the expansion ports
- Control of external trigger voltages
- Amplifier Soft Start and Main Relays
- Status LEDs for debugging and boot monitoring
- FLASH Write Protect

When the unit is powered up, these D-flops are cleared to zero, placing all DSPs and expansion ports into a reset state. In addition, the external triggers, amp relays, and status LEDs are held in an inactive state. The Flash boot sector write protect is active. These flops are strobed by an address decoded signal provided by the CPLD on sheet seven of the schematic. Refer to the Programmers Guide Revision 6 for further details regarding address decoding and bit field definition.

The test LED signals are also broken out to a row of test pads represented by J10.

RESET/ Buffer (U45)

U48 provides a buffered equivalent of the RESET/ signal to the FPGA, and to off-board components on the Front Panel PCB, the Amplifiers, and the Video PCB. All reside within the 5 Volt domain.

Proprietary Algorithm DSP 1 and 2 Host Interface (Sheet 3)

This sheet contains the system clock generator, spread spectrum generator, and the host interface and configuration blocks of both SHARC engines.

Clock Generator and Buffers (U46 and U47)

U47 is a standard Hex Inverter of which one stage is configured as a Colpitts Oscillator comprised of Y2, R165, C159, and C160. This circuit generates a 12.500MHz square wave at CMOS levels. R165 provides hysteresis for the gate, initiating and sustaining a reliable switching characteristic, while C159 and C160 provide the proper AC load to the reactive element of Y2. The second stage of this circuit is another gate from the hex package that simply buffers the output of the oscillator, presenting a minimal load to it while providing drive capability. Final buffering to the remainder of the 5V domain of this board is provided by yet another gate from U47, while buffering to the 3.3V domain is provided by U46.

Spread Spectrum Generator (U48)

U48 is a device that deliberately introduces a certain amount of clock jitter to any clock provided to the **CKI** pin (1). The purpose of this is to provide a quick solution to EMI emissions. By introducing a small amount of jitter to the system, the overall emission level is averaged out over a very wide band of frequencies, rather than isolated spikes of RF being emitted from a relatively low baseband of noise. The effect is an instantaneous change in duty cycle of the output clock at any given time. The amount of modulation is dependent on the state of the **SS** input pin (4). When this pin is high, the instantaneous duty cycle of the clock at the **CKO** pin (5) may have increased or decreased by as much as 3.75%. When the **SS** pin is low, the duty cycle variation is limited to 1.25%. The **FS2** and **FS1** pins (8 and 7) select the frequency range that the input clock falls within. FB17 provides a cleaner equivalent of the 5V digital supply rail to the Spread Spectrum device while C161 acts as a standard de-coupling capacitor.

As of this date, the Spread Spectrum operation has not been selected for use in this system. Resistors R166 and R170 select between straight unmodified system clocking or spread spectrum clocking. The default operation of this unit is with R166 in place: straight unmodified clocking.

DSP 1 and 2 Configuration (U16 and U34)

DSP 1 and DSP 2 are Analog Devices ADSP21161N 32-bit SHARC Microcomputers. They come packaged in a 255 position Ball Grid Array. The IO pins on these devices are not 5 volt tolerant, necessitating the level shifters on sheet 2 of this schematic set. These DSP devices are responsible for proprietary signal processing, such as Bass Management, Room Equalization, and LOGIC7 Surround Decoding. These blocks represent the sections of the Proprietary Algorithm DSPs that configure their default operation.

Clock I/O and Configuration

Device Pins: CLKIN (P12), XTAL (R13), CLKOUT (R9), CLK_CFG[1:0] (N12:13), CLKDBL/ (R12)

The DSP devices each have a clock input of 12.500 MHz, as provided by buffer gates U46. The clock-input pins **CLKIN** are impedance matched by R161 and R162. Since this topology uses an external oscillator rather than a crystal, the **XTAL** pins on each device are left floating and unused. The core clock frequency is derived from this input clock by internal PLL circuits. The PLLs are configured for X4 operation by the **CLK_CFG[1:0]** pins by hardwiring them to a binary value of 10, setting the core frequency to 50MHz. This core frequency is then further multiplied by two, by hardwiring the **CLKDBL/** pin to a logic 0. This makes the final core frequency 100MHz. The **CLKOUT** pin on each device connects to a test-point **ACKO** or **BCKO** depending upon which DSP device is of interest. The clock signals appearing here are 2X the input clock, or 25.00 MHz.

Interrupt Requests

Device Pins: IRQ2/ (J1), IRQ1/ (H4), IRQ0/ (H2)

The ADSP21161N has provision for three interrupt sources. In this application, only one is used, **IRQ0/**, with the unused IRQ lines pulled to an inactive high state. **IRQ0/** monitors an active low interrupt provided by the FPGA, which is generated coincident with the rising edge of the word clock divided by eight (i.e. 14.112MHz / 8 = 1.764MHz). Therefore, for every eight audio samples an interrupt is generated to the DSPs.

Bus Arbitration

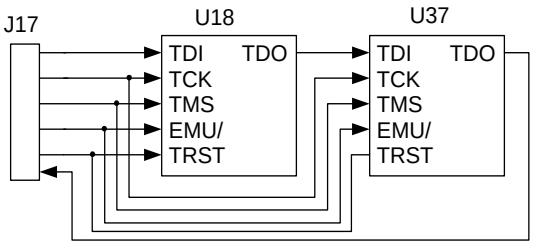
Device Pins: RBPA (B3), HBR/ (R10), HBG/ (R11), CS/ (N11), PA (R6), BR6/:BR1/ (M7, N7, P7, R7, N8, P8), SBTS/ (P6), ID2 (J3), ID1 (J2), ID0 (J4)

These DSP devices operate independent of each other, therefore the bus arbitration capabilities of these devices go unused and are wired to their inactive states. Since these devices share no resources each DSP has an ID code of 000, as hardwired to the ID[2:0] pins.

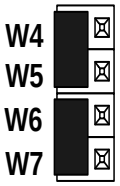
JTAG Interface

Device Pins: EMU/ (C2), TMS (C1), TCK (D2), TRST/ (B1), TDI (B2), TDO (D1)

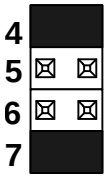
The DSPs support JTAG debugger access to the internal registers. Development code may also be loaded via the JTAG port using the Analog Devices ICE development toolkit. The principle departure from standard JTAG is the presence of the EMU/ signal. This is a status line that is read by the ICE tools. The JTAG signals break out to JTAG connector J17. Jumpers W7 through W10 implement device selection for JTAG. By selective jumpering one may talk to U16, U34, or U34 in series with U16. The following diagrams illustrate the various configurations. This function is used only in development and as such is not used in the standard build of this product. Note that R159 and R160 must be removed before using JTAG as they provide default termination of the TRST and TCK pins during normal operation.



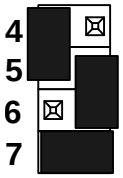
Series Connection Diagram



U18 JTAG ENABLED



U37 JTAG ENABLED



U37 + U18 JTAG ENABLED

General Purpose I/O

Device Pins: FLAG[9:4] (F3, E3, F2, F4, F1, G3)

Each flag pin may be configured as input or an output. In this application the flag pins listed above are configured by software as outputs. An internal register controls each flag output. They are used as test bits that activate status LEDs for each device. U15 provides increased drive capability for each flag pin to light the LEDs, while resistor networks RP1 through RP3 provide a default pull down state for these pins when the DSPs are being configured during the boot phase. When the devices are unconfigured, these flag pins default to input mode.

Note that FLAG0 is no longer used in this application. Its function is non-descriptor.

Proprietary DSP A SDRAM and Flash (Sheet 4)

This sheet shows the interconnection between DSP A and its SDRAM. It also illustrates the boot configuration for DSP A.

SDRAM (U6)

Each SHARC is supported by a 2 Mbit x 32 100MHz SDRAM. The memory interface is implemented as four banks of 256-words. Each successive 256-word page is accessed by bank switching. The memory device itself is non-linear as access is defined by row column address multiplexing. The SDRAM addressing scheme is implemented via a 10-bit wide address bus. The mapping is defined as:

Column Address:A[7:0]
Row Address: A[10:0]

Each 256-word page is accessed across four banks, with each bank selected by two bits BA[1:0].

The SHARC devices contain a memory interface controller, which multiplexes an array of internal address bits into the row-column scheme illustrated above. An integral part of the address muxing is the

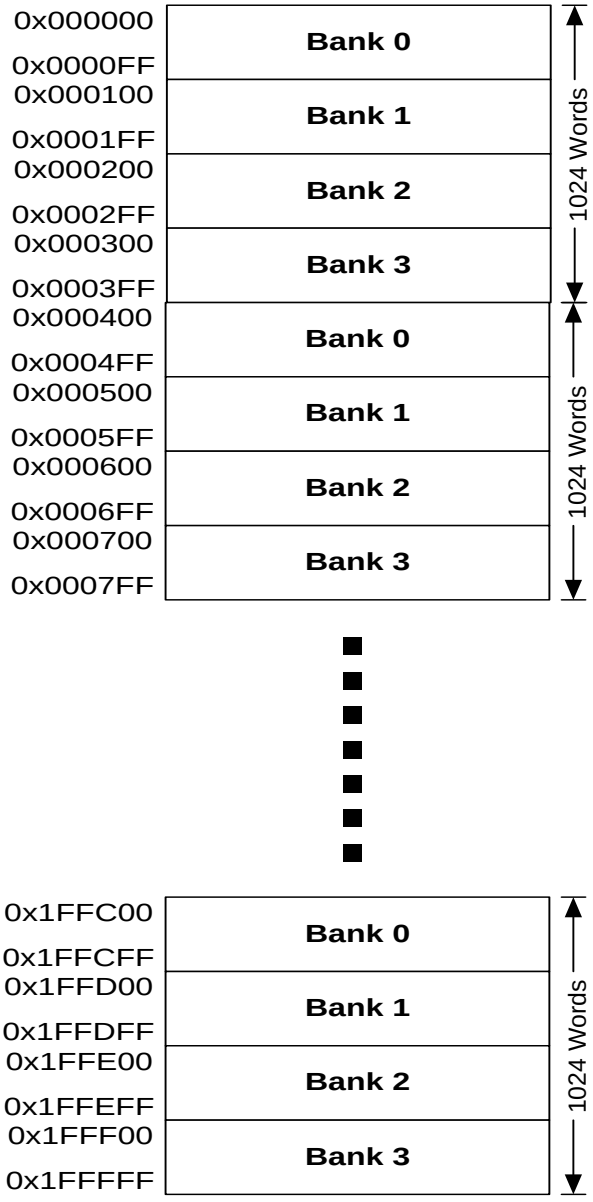
incorporation of the bank bits within the address space. The following table illustrates the internal to external address multiplexing.

SHARC DSP Internal to External Address bit mapping

Row Address		Bank Bits		Column Address	
Internal	**External**	**Internal**	**External**	**Internal**	**External**
A[20:10]	*A[10:0]*	*A[9:8]*	*A[14:13]*	*A[7:0]*	*A[7:0]*

Memory access is contiguous with this scheme. The following diagram illustrates how each 256-word page is interleaved in relation to the internal address.

Memory Interleave Diagram



Proprietary DSP A (U16)

The Memory interface and control block for U16 is shown on this page. The on-chip memory controller provides all the necessary interface to the SDRAM. The DSP accesses the memory data bus 32-bits at one time, eliminating the more conventional four data mask controls. These have been replaced by one control signal **DQM** (P13) which acts like an output enable during read accesses. This device also allows for four banks of memory and provides four chip select signals. As this application uses only one memory device, **MS0/** (N6) is the only chip select used. The **WR/** (M9), **RD/** (R8), **BRST** (N9), and **ACK** (M12) pins are valid only in topologies where there is a bus master and a bus slave. As there is no host connection to the DSPs through the Address and Data busses, and both DSPs are independent of each other, these signals serve no function. They are connected to their analogous pins on DSP B and are pulled up by internal resistors.

Boot Mode Configuration

The ADSP21161N supports a multitude of boot-up options. These options are chosen by hardwiring the **EBOOT** (A5), **LBOOT** (A6), and **BMS/** (A3) pins to the appropriate values. This application utilizes the SPI boot option, therefore these pins are hardwired to a value of 010 via RP4 and R69-R71.

Proprietary Algorithm DSP B SDRAM and Flash (Sheet 5)

This sheet shows the interconnection between DSP B and its SDRAM. It also illustrates the boot configuration for DSP B. The functionality of this page is identical to that of Sheet 4. Further discussion would be redundant.

DSP SPI Serial and Link Ports (Sheet 6)

This sheet shows the interconnection between DSP A and DSP B, as well as the SPI host interface as well as the audio data path into and out of the SHARCs.

SPI Interface

Signals: DSPASEL/, DSPASPICLK, DSPARXD, DSPATXD, DSPBSEL/

SPI is a serial interface protocol consisting of a four-wire interface: a chip select, two data pins, and a clock pin. This interface runs in full duplex mode allowing the SHARC to simultaneously receive and transmit data on the same port. The SHARCs are configured as slave devices to a master boot device. The interface between the CPU and the SPI port on each SHARC is implemented in the FPGA. The receive and transmit wires as well as the SPI clock are shared between the two DSPs, while selection of the devices is accomplished with their individual chip select signals.

The SPI interface is essentially a shift register that serially transmits and receives data synchronously with **DSPASPICLK**. When a SPI transfer occurs, data is shifted out of one end of the shift register on **DSPATXD** and into the other end of the shift register on **DSPARXD**. SPI transfers to U16 are accomplished by asserting **DSPASEL/** and beginning the transfer. SPI transfers to U34 are accomplished by asserting **DSPBSEL/** and beginning the transfer. The internal registers of the SHARCs are accessed sequentially with each transfer of a data byte.

Link Ports

Signals: DSPABLDATA[7:0], DSPBALDATA[7:0], L0CLK, L0ACK, L1CLK, L1ACK

The link port is a full duplex pathway that allows 100MHz bit rate transfers of audio data between the SHARCs. The **L0DAT[07:00]** ports on each device are configured as transmitters while the **L1DAT[07:00]** ports are configured as receivers. Data is transmitted from U16 to U34 on **DSPABLDATA[7:0]** synchronous with the clock sourced from the **L0CLK** pin on U16. U34 receives this data on the rising edge of this clock. When a transfer is complete, U34 transmits an acknowledge signal to U16 via the **L0ACK** signal. Transfers in the opposite direction are handled the same way, except that the clock source is on U34 while the acknowledge source is on U16.

Currently this application is not using the link ports, and as such this interconnection is only a provision for future enhancements of capability.

SPORT Data Ports

Signals: SPORT_CLK_A, SPORT_FS_A_N, DSPASP3FPGA, DSPASP0FPGA, SPORT_CLK_B, SPORT_FS_B_N, DSPBSP3FPGA

Each SHARC has four SPORT data ports comprised of a frame sync signal, a serial clock, and two bi-directional data ports. U16 utilizes three of these ports. Port 0 is used as the receive data port, while Port 2 is used as a full duplex channel between U16 and U34. Port 3 is the return port for the Main Zone data. Port 1 is unused. Timing is shared among all three used ports.

The SPORT data format is comprised of a serial bit stream of eight 32-bit samples, a serial shift clock and a frame start signal. The audio data entering U16 on **DSPASP0FPGA** is comprised of samples from either the system S/PDIF inputs, the outputs of the A/D Converters from the Analog IO Board, or the I^2S streams output from the Format Decoder DSP. The selection of which stream is sent along to the SHARC is done via data multiplexing within the AVRX FPGA. The data is clocked into the input buffers on the SHARC by **SPORT_CLK_A** while the beginning of the data frame is marked by **SPORT_FS_A_N**.

SPORT data for the Main Zone is returned to the FPGA via **DSPAP3FPGA**. This data is synchronous with **SPORT_CLK_A** with each frame start marked by **SPORT_FS_A_N**. This data is re-converted back to the I^2S format via a look-up table operation within the AVRX FPGA.

DSPA2DSPB is a data path from U16 to U34 synchronous with **SPORT_CLK_A** and frame start marked by **SPORT_FS_A_N**, while **DSPB2DSPA** is a data path from U34 to U16 synchronous with **SPORT_CLK_B** and frame marked by **SPORT_FS_B_N**.

U34 provides a downmix data to the Analog IO Board via **DSPBP3FPGA** on SPORT port 3. This data is converted back to I^2S data via look-up table operation within the FPGA. This data is synchronous with **SPORT_CLK_B** and frame start marked by **SPORT_FS_B_N**. SPORT port 0 on U34 is a full duplex communication channel to U16, and performs the same function as port 2 on U16.

The data ports are open drain, therefore need pull-up resistors R73, R74, and R140.

DSP/FPGA Power Conn. (Sheet 7)

This sheet shows the power and ground pin distribution within the SHARC devices and the regulator scheme for the SHARC inner core power supply. This sheet also shows the glue logic CPLD and interface to the VFD on the front panel.

Power and Ground Distribution (U16 and U34)

The SHARC devices require two supply voltages. One voltage powers the 3.3V IO while the inner core of the device runs off of 1.8V. There are 13 pins on each device that require 3.3V, 14 pins that require 1.8V, and one pin that requires a separate 1.8V to power the internal PLL circuitry. There are twenty-six digital logic ground pins and one analog ground pin for the PLL. When the SHARCs are first powered up, care must be taken to ensure that the IO supply voltage does not come up faster than the core voltage supply as destruction to the silicon would result. D37 and D47 are fast Schottky diodes rated at a forward current of 1 amp. These diodes effectively clamp the 3.3V rail to the 1.8V rail, ensuring that the two sets of supply pins will track each other during power up to a level of 1.8V, thereby ensuring a stable core voltage being present before the IO voltage climbs to its stability point.

The AGND pin is tied to digital ground in this implementation.

1.8V Regulator Circuitry (U22 and U39)

U22 and U39 are Adjustable Low Dropout Voltage Regulators. Resistive dividers set the output voltages for these devices; R77/R78 for U22 and R143/R144 for U39. The voltage is set by the following equation:

$V_{OUT} = V_{REF} (1 + R77/R78) + I_{ADJ} R78$

Where: $V_{REF} = 1.25V$, $I_{ADJ} = 60uA$

Substitute R143 for R77, R144 for R78 for U42 programming.

C67 and C127 provide local filtering of the 5V supply feeding the regulators. C75 and C133 provide local bulk capacitance to the 1.8V planes for each SHARC. At least one device from each of these pairs must be a low ESR tantalum type, or the regulators will oscillate. Pins 2 and 4 of the regulators are electrically the same pins, but they are shown connected together at the schematic level. R76 and R142 provide a de-coupled 1.8V to the analog PLL supply pin on each SHARC while C73/C74 and C130/C131 provide local high frequency de-coupling of this voltage.

The 1.8V planes for each device break out to test points +1.8V-A and +1.8V-B for ease of measurement.

Glue Logic CPLD (U44)

This device provides address decoded strobes for the external registers, the CPU clock, and the address decoded control interface to the VFD.

CPUCLKI is a 6.25MHz clock signal that is derived by dividing the input clock **CLK12500B** by 2. This clock is the system clock for the CPU on sheet 1.

RESREGDECL is decoded from chip select **CPUCS3/**, write strobe **CPUWRL/**, and the condition **CPUADDR[3:1]**==000. The result is an active high strobe when a write operation is performed at CPU address 0x00C00000. This strobe acts as a clock signal for register device U21 on sheet 2. The table on the next page illustrates the register control.

Address == 0x00C00000							
07	**06**	**05**	**04**	**03**	**02**	**01**	**00**
AMPMRLY	EXPBRST	EXPARST	ETRGEN1	ETRGEN0	DSPCRST	DSPBRST	DSPARST

- AMPMRLY – Amp Mains Relay CTRL
  = 0: Relay is open.
  = 1: Relay is closed.
- EXPBRST – Expansion Slot 1 Reset
  = 0: Expansion Slot 1 is reset.
  = 1: Expansion Slot 1 is out of reset.
- EXPARST – Expansion Slot 0 Reset
  = 0: Expansion Slot 0 is reset.
  = 1: Expansion Slot 0 is out of reset.
- ETRGEN1 – External Trigger 1 Enable
  = 0: External Trigger 1 is inactive.
  = 1: External Trigger 1 is active.
- ETRGEN0 – External Trigger 0 Enable
  = 0: External Trigger 0 is inactive.
  = 1: External Trigger 0 is active.
- DSPCRST – Format DSP Reset
  = 0: CS494001 is in reset.
  = 1: CS494001 is out of reset.
- DSPBRST – SHARC U33 Reset
  = 0: U33 is in reset.
  = 1: U33 is out of reset.
- DSPARST – SHARC U16 Reset
  = 0: U16 is in reset.
  = 1: U16 is out of reset.

External Register U21 bit map

RESREGDECH is decoded from chip select CPUCS3/, write strobe CPUWRH/, and the condition CPUADDR[3:1]==000. The result is an active high strobe when a write operation is performed at CPU address 0x00C00000. This strobe acts as a clock signal for register device U20 on sheet 2. The following table illustrates the register control.

Address == 0x00C00000							
15	**14**	**13**	**12**	**11**	**10**	**09**	**08**
D10	D11	D12	D13	D14	D15	BOOTLOCK	SOFTRLY

- CPULED6 – Test LED D10
  = 0: D10 is off
  = 1: D10 is lit
- CPULED5 – Test LED D11
  = 0: D11 is off
  = 1: D11 is lit
- CPULED4 – Test LED D12
  = 0: D12 is off
  = 1: D12 is lit
- CPULED3 – Test LED D13
  = 0: D13 is off
  = 1: D13 is lit
- CPULED2 – Test LED D14
  = 0: D14 is off
  = 1: D14 is lit
- CPULED1 – Test LED D15
  = 0: D15 is off
  = 1: D15 is lit
- BOOTLOCK – Program Flash Boot Sector Lock
  = 0: Boot sector is write protected
  = 1: Boot sector is write enabled
- SOFTRLY – Amplifier Soft Relay
  = 0: Soft Relay is open
  = 1: Soft Relay is closed

External Register U20 bit map

Note that the U20 and U21 are word accesses to the same CPU address and that they are write only.

DISP_RS is a decode of **CPUCS3/** and the condition **CPUADDR[3:1]** == 001. This is an active low signal and is a function bank select signal for the VFD.

DISP_RW is a read/write strobe for the VFD. When this signal is high, the VFD registers are in read mode. When low, the registers are in write mode. This signal is a decode of **CPURD/**, **CPUCS3/**, and the condition **CPUADDR[3:1]** == 001 or == 010.

DISP_E is a global enable of the VFD and is a decode of **CPUCS3/** and **CPUADDR[3:1]** == 001 or == 010. This is an active high signal.

VFD Data Bus Transceiver (U43)

This device is a byte wide, bi-directional tristate buffer interface for the VFD data bus. The buffer's direction and tristate controls are address decoded signals from CPLD U44. When write cycles are performed to the VFD Display Control Register (CPU Address 0x00C00003) or the VFD Data Register (CPU Address 0x00C00005), the tri-state buffer is enabled, and data flow is from the CPU to the VFD. When read cycles are performed at these register locations, The buffer is enabled and data flow is from the VFD to the CPU. When these register locations are not addressed for access, the tristate buffer is disabled and the IO pins float.

Format DSP (Sheet 8)

This sheet contains the format DSP, associated FLASH RAM algorithm memory, timing circuitry, and delay components necessary for proper interfacing between the DSP and RAM.

Format DSP (U25)

This device decodes all the "canned" algorithm information from the input data streams provided by the FPGA. This device is a Crystal Semiconductor CS494001 Multi-Standard Audio Decoder. It is packaged in a 144 pin LQFP. In truth, this decoder is actually two DSP engines in one package (DSPAB and DSPC). Each engine has it's own SPI port for host communication.

Power Up State

Signals: CRY_RESET/, FHS[2:0], UHS[2:0]

When the RV8 is first powered up, the Format DSP is placed in a reset state by the signal **CRY_RESET/** going low. This signal is controlled by external register U21, which will hold U25 in reset until released by the system software. When this reset is asserted high, pins **FHS[2:0]** and **UHS[2:0]** are sampled on the rising edge of **CRY_RESET/**. **FHS[2:0]** sets the host interface mode for DSPAB to SPI serial mode by hardwiring these pins to a binary value of 101. **UHS[2:0]** performs the same function for DSPC, and is hardwired to a binary value of 101, again selecting SPI serial mode.

SPI Interface

Signals: CRY_SCS/, CRY_SPICLK, CRY_RXD, CRY_TXD, CRY_INTREQ/, DSPASPICLK, DSPARXD, DSPATXD, CRY_FCS/, CRY_FINTREQ/, HINBSY

During the boot phase of RV-8, algorithm code is loaded into the format FLASH and then into the on-board SRAM. All external memory is accessed through DSPC via its SPI port. As demonstrated with the SHARC devices, the two SPI ports for DSPAB and DSPC are shared, with each one selected by independent chip select signals. Host instructions to DSPC are transmitted from the FPGA via **CRY_RXD**. Status from DSPC is transmitted back to the FPGA/Host via **CRY_TXD**. Data on both ports is synchronous with **CRY_SPICLK**. All transfers to and from DSPC take place when **CRY_SCS/** is asserted low. DSPC only serves to interface to external memory. The available post-processing of audio data is not utilized in this application. **CRY_INTREQ/** is an open drain output that is asserted low when DSPC has control data that requires host CPU attention. This signal is pulled up to +2.5V via a section of RP10.

DSPAB implements the following audio algorithms:

- Dolby Digital EXTM
- Dolby Pro Logic IITM
- DTS-ES 96/24TM
- DTS 96/24TM
- DTS-ES
- Discrete 6.1TM
- DTS-ES Matrix 6.1TM
- DTS Digital SurroundTM
- DTS Virtual 5.1TM
- Surround 6.1 (C.O.S. 6.1)TM
- THX Surround EXTM
- THX Ultra2 CinemaTM.

The I^2S audio streams coming in to the Format Processor are interrogated via the DSPAB SPI port and its status is reported back to the CPU. The SPI port for DSPAB is selected by asserting **CRY_FCS/** low. **CRY_FINTREQ/** is an open drain output that is asserted low when DSPAB has control data that requires the host CPU attention. This signal is pulled up to +2.5V by a 3.3K resistor.

Provision is made to utilize the SPI signals for SHARC U16, **DSPASPICLK**, **DSPARXD**, and **DSPATXD**. This provision would be selected by installing R101, R103, and R104 and de-installing R100, R102, and R105. This provision is not implemented in this application.

HINBSY is an output signal the status of which is latched into a control register within the FPGA. The CPU polls this register bit. If this bit is high, it indicates that either DSPAB or DSPC has not read data written via SPI. No other data may be written until this bit is cleared to 0 internally.

All SPI signals are broken out to test points for ease of monitoring.

Unused Pins

Pins: CS/, WR/, RD/, A0, A1, HDATA[7:0], FA0, FA1, FDATA[7:0], CMPREQ, CMPCLK, CMPDAT, LRCLKN, SCLKN, SDATAN[3:0]

All above listed pins function either as parallel host interface pins or as unused audio channel inputs. As such they are unused in this application and therefore are pulled up to +2.5V by a section of RP7.

Audio Input Port

Signals: DEC_IN_FSI, DEC_IN_SCKI, DEC_SDI

This port takes as input I^2S audio data **DEC_SDI** synchronous with **DEC_IN_SCKI**. A frame start pulse is also utilized, **DEC_IN_FSI**. These signals are sourced from the AVRX FPGA. This data is multiplexed into the Format Decoder from one of two sources. I^2S data may come from the Main zone S/PDIF input block or from one of six ADCs on the Analog I/O Board.

Chip Clock

Signals: CLK12500C, XTALO, PLLVDD, FILT1. FILT2, CLKSEL, PLLVSS

There are two possible methodologies of providing a global clock signal to the Format Decoder. The default topology consists of U30, a 12.288MHz 3.3V oscillator. R107 places the output of U30 into the path of the **CLKIN** pin. R108 ties the oscillator enable high, causing it to generate the clock.

The second clock source is from the system clock signal **CLK12500C**. R106 would pass this clock signal along to the Format Decoder in this option. Naturally, the other two options would have to be disabled and taken out of the path. This topology has been determined to be not practical due to the differences in internal topologies between the Format Decoder and the SHARCs. As a result, this option is not implemented.

FB13 provides a high frequency filtered version of the 2.5VA supply, which in turn is a high frequency filtered version of the digital 2.5V supply. This double filtered supply voltage drives the internal Phase Lock Loop of the Format Decoder at the **PLLVDD** pin. C100 provides local bulk capacitance for this supply rail through the **FILT1** pin.

The internal PLL circuitry requires external band-pass filtering, which is provided via the **FILT2** pin by R99, C98, and C99.

CLKSEL selects the source clock for all internal logic in the Format Decoder, and is controlled by software. When this signal is low, the internal clock source is the internal PLL. When high, then all internal logic is driven by the **CLKIN** pin directly. This signal is significant during the boot phase of RV-8 when the algorithm FLASH U19 is being loaded. Writing to this FLASH can only happen reliably when **CLKSEL** is high.

PLLVSS is connected to digital ground. This is the ground return pin for the internal PLL.

SDRAM Interface

Signals: SD_CS/, SDCKE/, SDCLKI, SDCLKO, DQM0/, DQM1/, SD_CAS/, SD_RAS/, SDWE/

SDRAM is not implemented for the Format Processor. As such, these pins are all pulled high by RP5, RP6, and RP7.

FLASH Interface

Signals: CRY_NVCS/, CRY_NVWE/, CRY_FLCS/, CRY_NVOE/, DELWE/, NVCS, CRY_A[19:0], CRY_D[7:0], GPIO20, GPIO21

The format processor utilizes a 512Kx8 FLASH RAM (U19) for algorithm storage. The algorithms are loaded into the FLASH during the boot phase. Due to a bug in the silicon for the CS49400, the write enable for the FLASH must be delayed approximately 10nS in relation to the address bus **CRY_A[19:0]**. This is accomplished by R50/C21 which slows down the falling edge of **CRY_NVWE/**, effectively delaying it by approximately 5nS. This signal is OR'ed with the original **CRY_NVWE/** to better align the rising edge of **DELWE/** with the address bus so that the hold time will not be violated. An additional 5nS is picked up

from the propagation delay of a gate within U7. The resultant signal **DELWE/** is the write enable for U19. Software requirements dictate that the FLASH address space begin at 0x80000. U13 decodes out the start address with chip select. When **CRY_A19** is high and **CRY_NVCS/** is low, pin 4 of U13 goes low. This signal is used as the chip select for the FLASH, **CRY_FLCS/**.

Due to another bug within the CS49400, writing the FLASH must be accomplished by using GPIO20 and GPIO21 as address pins. At the beginning of a write cycle to the FLASH, erase commands are sent to specific addresses within the device. **GPIO[21:20]** take the place of **CRY_A[1:0]** during this phase of the operation. During normal read operations, the GPIO pins are programmed to be always low, and **CRY_A[1:0]** are passed along to U19 via OR-gates U7. During read cycles, **DELWE/** is driven high while the output enable signal **CRY_NVOE/** is driven low, enabling the read buffers on U19. All data transfers are eight-bits wide, and are accomplished via data bus **CRY_D[7:0]**.

In future revisions of the CS49400 silicon, all delay and logic steering circuitry will be designed out. Provision to remove the delay elements from the circuit is provided by R51, R52, R54, and R56.

Audio Output Port

Signals: DEC_MCKI, DEC_OUT_SCKI, DEC_OUT_FSI, DEC_SDO[3:0]

The Format Decoder outputs four I^2S audio data streams to the AVRX FPGA, **DEC_SDO[3:0]**. These are multiplexed to an eight channel serial interface that is in the Analog Devices SPORT mode. This eight channel interface drives the SPORT inputs of the SHARCs. The serial bits are synchronous with **DEC_OUT_SCKI**, which is equal to 64 * FS. **DEC_OUT_FSI** is the audio output sample rate clock.

Output Port Map Table

Pin Number	Pin Name	Signal	Map
110	AUDATA0	DEC_SDO0	Left/Right
109	AUDATA1	DEC_SDO1	Center/Sub
107	AUDATA2	DEC_SDO2	Left Surround/Right Surround
106	AUDATA3	DEC_SDO3	Downmix OR Left Back/Right Back

DEC_MCKI is the master serial bit clock for the Format Decoder, and is provided by the AVRX FPGA, as are **DEC_OUT_SCKI** and **DEC_OUT_FSI**.

Test Pins

Signals: TEST, DBCK, DBDA, FDBDA, FDBCK

These pins are pulled up to +2.5V via RP8 for normal operation, with the exception of **TEST**, which is pulled down. These pins are for internal testing by the manufacturer and serve no useful function to this application.

Power Supply and Ground

Signals: +2.5VD, +3.3VD, DGND

The CS49400 operates with 3.3V I/O and a core voltage of 2.5V. There are seven core voltage pins tied to +2.5VD by a mini-plane on the PCB and four I/O voltage pins tied to the system wide 3.3VD plane. Diode D24 is a fast SCHOTTKY device rated with a forward current of 1A. The diode clamps the core voltage supply pins to the I/O supply pins. This ensures that the I/O pins will track the core voltage at power-up. Destruction of the chip could result if the I/O voltage rises faster than the core voltage. With this topology, the 3.3VD supply will be pulled along with the 2.5VD supply if the 3.3V supply is slow in

coming up. This is a likely scenario given the fact that the 3.3V rail is more heavily loaded than the 2.5V rail.

There are seven ground pins associated with the core supply, and four associated with the I/O supply. In addition, there are five no connect pins that are recommended by the manufacturer to be tied to GND. All sixteen pins are tied to the DGND system plane.

Algorithm Storage FLASH RAM (U19)

The FLASH RAM is an ATMEL AT29LV040A 4Mbit device, organized as 512Kx8. 3.3 volts power this device. It operates much like an EEPROM. Read cycles are identical to PROM operation with data output on **CRY_D[7:0]** when chip select and output enable are both low. The output buffers enter a high impedance state when either of these signals is high.

This device uses software data protection programming. Prior to writing data to this device, a series of three programming commands must be presented at specific addresses. Data will not be written without this sequence. The FLASH is organized as 2048 sectors of 256 bytes each. If any data within a sector is to be changed, then the entire sector must be programmed. Each sector is erased automatically prior to writing. Writing occurs when the WE/ and CE/ pins are low, and OE/ is high.

Main FPGA (Sheet 9)

This page contains the AVRX FPGA, which performs many salient functions to the main board. It is packaged in a 208-pin QFP package. The AVRX FPGA converts and routes various digital audio formats among the system I/O connectors and DSP processors, and has Serial Peripheral Interface (SPI) ports that provide the means for the host processor to communicate to the system peripherals. It also has an I2C interface for host communication to the video codec and it has interfaces for the IR remote control and rotary encoder.

AVRX (U41)

Functionality is implemented within a Xilinx XC2S200 device. This device contains 200,000 logic gates, 75,264-bits of distributed RAM, and 56K bits of block RAM. 2.5V for core operation and 3.3V for IO operation powers it. The FPGA may be configured either by the system software during the boot phase, or by a 128K serial FLASH PROM during development.

Configuration

Resistors R157 and R158 select the programming mode of the FPGA. The default condition with R158 installed and R157 uninstalled configures the device as a slave operating in serial mode. In this operating mode, the programming data is loaded into the device via the DIN_DATA0 pin (153) with the rising edge of the signal appearing at the CCLK pin (155). The host processor provides both signals. In the alternative scheme, R158 is uninstalled and R157 is installed. This places the FPGA in master serial mode. This is appropriate for loading from a serial EPROM. In this mode of operation, the FPGA provides a shift clock out of the CCLK pin to the programming EPROM, which in turn shifts programming data into the DIN_DATA0 pin synchronous with this clock.

Resistors R128 through R131, R133 through R135, and R148 through R151 configure the source of programming. The default condition routes the serial data and shift clock from the host CPU. In addition, the INIT/, PROGRAM/, and DONE pins of the FPGA are routed to the host. The following table illustrates the configuration for this mode.

FPGA Programming Source Configuration Table

FPGA PROGRAMMING CONFIGURATION													
R128	R129	R130	R131	R133	R134	R135	R148	R149	R150	R151	R157	R158	MODE
IN	IN	IN	IN	OUT	OUT	OUT	IN	OUT	IN	OUT	OUT	IN	Host Programming (Default)
OUT	OUT	OUT	OUT	IN	IN	IN	OUT	IN	OUT	IN	IN	OUT	EPROM Programming (Development)

Host Bus Interface

Signals: CPUADDR[9:0], LVDATA[7:0], CPUCS2/, CPUWRL/, CPURD/, BUFDIR, CPUCLKOUT, RESET/

The AVRX FPGA internal registers are contained entirely within the CS2/ memory space of the host CPU. Therefore, the memory space that these registers occupy begins at a base address of 0x00800000. Register accesses are implemented over a byte wide data bus **LVDATA[7:0]** with 1Kbytes of addressing implemented over a 10-bit wide address bus **CPUADDR[9:0]**. Write accesses are made when the host CPU asserts **CPUWRL/** and **CPUCS2/** to low states. Read accesses are made when the host CPU asserts **CPURD/** and **CPUCS2/** to a low state.

The FPGA has 5 volt tolerant IO, so the address, chip select, read and write control lines come directly from the CPU. During read cycles, the FPGA places data on the bus at 3.3V logic levels. This must be level shifted into the 5V domain to be reliably read by the CPU. The bi-directional ports on sheet two of this schematic provides this level translation to and from the CPU. The direction of these level-shifting transceivers is controlled by **BUFDIR**. This signal is low during write cycles to the FPGA, and high during read cycles from the FPGA.

CPU accesses to and from the FPGA are synchronous with the core frequency of the host processor, 25MHz. This clock is provided by the host to the FPGA as CPUCLKOUT.

RESET/ is a power-up reset signal that clears the state of the internal registers to zero. This signal serves little more purpose than to be a fail safe mechanism to ensure proper resetting of the FPGA, as this device is cleared whenever the power to the unit is removed. The FPGA is re-configured at each power-up and boot phase.

Interrupt Sources

Signals: WCLKDIV8INT/, LVKYBDIRQ/, LVDSPABIRQ/, LVCRYIRQ/, LVVIDTUNIRQ/

WCLKDIV8INT/ is an interrupt to the SHARC DSPs that occurs once every eight audio samples being presented to the SPORT IO.

LVKYBDIRQ/ is an interrupt to the host CPU that is generated each time a button on the front panel is pressed. A second interrupt is generated when the key is released. This carries a host interrupt priority of level 0. This interrupt is level shifted to 5V prior to being presented to the CPU.

LVDSPABIRQ/ is an interrupt to the host CPU that is generated whenever a read or write transaction via the SHARC SPI ports has been completed. This carries a host interrupt priority of level 2. This signal is level shifted to 5V prior to being presented to the CPU. At present, this interrupt is masked off and unused by system software.

LVCRYIRQ/ is an interrupt to the host CPU that is generated whenever a read or write transaction via the Format Decoder SPI ports has been completed. This carries a host interrupt priority of level 3. This signal is level shifted to 5V prior to being presented to the CPU. At present, this interrupt is masked off and unused by system software.

LVVIDTUNIRQ/ is an interrupt to the host CPU that generated whenever RDS data from the tuner module is ready to be read by the CPU. This interrupt is a shared resource with the video board. It carries an interrupt priority of level 7. This signal is level shifted to 5V prior to being presented to the CPU. At present, this interrupt is masked off and unused by system software.

Front Panel Interface

Signals: FP_IR_IN1, FP_SDATA_IN, FP_SDATA_OUT, FP_SDATA_CLK, FP_SDATA_LTCH, FP_ENCA_IN, FP_ENCB_IN

FP_IR_IN1 is a signal from the front panel remote control infra-red detector. The data from this detector is a serial bit stream that represents commands that change operative modes of the RV8. When a low to high transition has been detected from the IR receiver, the internal state machine checks to make sure the incoming signal is a valid command stream by checking the period of the low to high and high to low transitions. If it is not, then the state machine waits for another low to high transition in the detector stream.

If the incoming stream is a valid command stream, then the data extracted is compared to a look-up table of valid code values. This value is then stored in a RAM buffer that is polled by the host CPU.

FP_SDATA_IN is part of a four-wire interface that controls the front panel LED display and pushbutton matrix. This signal is a return stream of data reporting front panel button status to the host CPU. Changes in button status are serially transmitted to the AVRX FPGA where current status is XOR'ed with the previous status of the last scan. A retriggerable timer is armed whenever the XOR gate is activated indicating a change in any of the buttons. This timer sends a host interrupt after button activity has stabilized for three milliseconds. This three millisecond period filters any switch bounce.

FP_SDATA_OUT is the transmitting stream from the main board to the front panel that controls the LED illumination that is part of the user interface. LED data is written to a RAM buffer internal to the FPGA and is transmitted up to the front panel at a bit rate of 1MHz.

SDATA_CLK is the clock signal that controls the serial shift of data up and back from the front panel.

FP_SDATA_LTCH is a signal that marks the beginning of an eight bit sample being transmitted to the front panel.

This four-wire interface works in conjunction with an FPGA on the front panel PCB. Refer to the theory of operation for this board for further details.

FP_ENCA_IN and **FP_ENCB_IN** comprise a two-wire quadrature signal from the rotary encoder on the front panel. The direction of rotation of the encoder is determined by the relative position of a rising edge on **FP_ENCB_IN** compared to **FP_ENCA_IN**. When the encoder is rotated clockwise, the rising edge of **FP_ENCB_IN** occurs during a high cycle of **FP_ENCA_IN**. When the encoder is rotated counter-clockwise, the edge occurs during a low cycle. The AVRX FPGA debounces the signals from the rotary encoder, and uses the debounced signals to control a four position Gray Code counter. This counter can be read by software to determine the position of the encoder.

Digital Audio I/O

Signals: SPDIF_COAX_IN[4:1], SPDIF_OPTO_IN[4:1], DIG_REC_OUT

Provision is made within the RV-8 for eight S/PDIF inputs, four from coaxial sources, and four from optical fiber sources. The coax sources are signal conditioned and buffered prior to being routed to the AVRX FPGA. The optical sources require no additional conditioning and so are routed directly to the AVRX from the TORX connectors. The AVRX determines the word clock from incoming S/PDIF samples via phase comparison with the system word clock from the on-board PLL circuitry. The PLL is adjusted until the system word clock is the same as the S/PDIF word clock. The S/PDIF inputs are sampled with a clock that is 1024 times the sample rate in 96/88.2 KHz mode and 2048 times the sample rate in 48/44.1 kHz mode to compensate for sources that display a significant amount of jitter. This oversample scheme eliminates the need for a two stage PLL. The S/PDIF channel status bits from all channels may be read through the host interface.

DIG_REC_OUT is sourced from the AVRX FPGA. SPORT data from the downmix port of the SHARCs or digital audio data from the Record Zone DAC is converted to a Bi-phase mark signal with parity added by the AVRX.

Format Decoder Interface

Signals: CRY_CLKSEL, CRY_TXD, CRY_RXD, CRY_SPICLK, CRY_FCS/, CRY_SCS/, CRY_INTREQ/, CRY_FINTREQ/, HINBSY, DEC_IN_FSI, DEC_IN_SCKI, DEC_SDI, DEC_MCKI, DEC_OUT_SCKI, DEC_OUT_FSI, DEC_SDO[3:0]

CRY_CLKSEL is a programmable bit within the MUTE/IR control register that sets the internal operating speed of the Format Decoder. When this bit is high, the internal logic of the Format Decoder runs at the input clock rate. When low, the Format Decoder runs at the higher frequency of its internal PLL. The power up mode of this pin is low.

CRY_TXD transmits control data to the Format Decoder utilizing a modified SPI (Serial to Parallel Interface) protocol. Control data is written to the internal Format Decoder SPI Control RAM by the system software and serially shifted out via this pin.

CRY_RXD receives control status information from the Format decoder in serial form. This data is stored within the Format Decoder SPI Status RAM and is polled by the system software.

CRY_SPICLK is the shift clock used by the SPI protocol to serially shift data into and out of the Format Decoder. The speed of this clock is controlled by **CRY_CLKSEL**. This clock must be in slow mode when programming the Format Decoder FLASH RAM during boot up.

CRY_FCS/ is the chip select for the DSPAB section of the Format Decoder. This chip select is enabled when bit 0 in the SPI Chip Select Register is set high. This register bit must be set before data is written to the Format Decoder SPI Control RAM. The DSPAB section of the Format Decoder is responsible for all algorithm decoding as listed on page 6-27. SPI transfers are initiated when the Format Decoder SPI DMA Block Size Register is loaded with the number of bytes to be transferred. When a transaction has been completed, the host processor must reset the chip select bit low.

CRY_SCS/ is the chip select for the DSPC section of the Format Decoder. This chip select is enabled when bit 1 in the SPI chip select register is set high. This register bit must be set before data is written to the Format Decoder SPI Control RAM. The DSPC section of the Format Decoder is responsible only for accessing the FLASH device attached to the Format Decoder. SPI transactions are handled in the same manner as for **CRY_FCS/**.

CRY_INTREQ/ is an interrupt line that indicates that DSPC has out-going control data and should be serviced by the host CPU. When this interrupt occurs, bit 2 in the Interrupt Status Register is set. This bit is then cleared after the host CPU polls this register. This interrupt is active low.

CRY_FINTREQ/ is an interrupt line that indicates that DSPAB has out-going control data and should be serviced by the host CPU. When this interrupt occurs, bit 3 in the Interrupt Status Register is set. This bit is then cleared after the host CPU polls this register. This interrupt is active low.

HINBSY is a status signal from the Format Decoder that indicates that control data written via the SPI port has not yet been read by the decoder. This signal serves as a hold-off for the host CPU, preventing it from over-writing control data before it has a chance to be implemented by the Format Decoder. The state of this signal is stored within the Serial Interface Status Register at bit 7, which is continuously polled by the host processor. When this bit is set high, the host will not write any further instructions via the SPI port until the system software sees this bit UN-set to zero again.

DEC_IN_FSI is the word clock output to the Format Decoder that operates at 44.1kHz or 48kHz, dependent upon the sampling rate of the source material multiplexed in on the **DEC_SDI** signal.

DEC_IN_SCKI is the sample clock 64FS output to the Format Decoder. **DEC_SDI** is synchronous with this clock.

DEC_SDI is the I^2S formatted audio data input to the Format Decoder. Audio data from the system S/PDIF inputs or from the signal **MAIN_I2S_IN1** is multiplexed down to this one signal.

DEC_MCKI is the bit clock of the DEC_SDI stream and equivalent to 256FS.

DEC_OUT_SCKI is the sample clock 64FS output from the Format Decoder. Signals **DEC_SDO[3:1]** are synchronous with this clock.

DEC_OUT_FSI is the word clock output from the Format Decoder that marks the sample frames on the DEC_SDO outputs.

DEC_SDO[3:0] are the four data output streams from the Format Decoder. These streams carry the 5.1 decoded audio data. This data is further format for compliance to the Analog Devices SPORT specification and routed to the SHARC devices.

SHARC Interface

Signals: DSPATXD, DSPARXD, DSPASPICLK, DSPASEL/, DSPBSEL/, DSPASP3FPGA, DSPBSP3FPGA, DSPASP0FPGA, SPORT_CLKA_A, SPORT_FS_A_N, SPORT_CLK_B, SPORT_FS_B_N

DSPATXD transmits control data to the SHARCs utilizing the Analog Devices SPI (Serial to Parallel Interface) protocol. Control data is written to the internal SPI Control RAM by the system software and serially shifted out via this pin. This signal is shared between both SHARC devices.

DSPARXD receives control status information from the SHARCs in serial form. This data is stored within the SPI Control Status RAM and is polled by the system software. This signal is shared between both SHARC devices.

DSPASPICLK is the shift clock used by the SPI protocol to serially shift data into and out of SHARCs.

DSPASEL/ is the chip select for the SPI port on SHARC1 (U18). This signal enables SPI communications with U18. Setting bit 4 in the SPI Chip Select Register high enables it. Once this bit is set, then control data is written to the SPI Control RAM, then the number of bytes to be shifted out on **DSPATXD** is written

to the SPI DMA Block Size Register. Once this register is written, then a SPI transfer occurs to the SHARC. When the transfer is done, the host CPU is interrupted by **DSPABIRQ/**. The system software must then clear bit 4 in the SPI Chip Select Register to zero.

DSPBSEL/ is the chip select for the SPI port on SHARC2 (U37). This chip select is enabled by writing a one to bit 5 in the SPI Chip Select Register. Transfers to SHARC2 are implemented in the same fashion as described under **DSPASEL/**.

DSPASP3FPGA is the DOWNMIX audio return signal from SHARC1 in SPORT format. The data present in this stream is converted to S/PDIF and I^2S formats and mapped via Look-Up Table to the output ports.

SPORT_CLK_A is the serial shift clock for the data present on **DSPASP3FPGA** and **DSPASP0FPGA**.

SPORT_FS_A_N is the frame sync signal for **DSPASP3FPGA** and **DSPASP0FPGA**.

DSPASP0FPGA is an input data stream in SPORT format to SHARC1. Samples from the outputs of the Format Decoder and from the various system inputs are multiplexed and mapped through the Input Source Look-Up Table to this data signal.

DSPBSP3FPGA is the MAIN audio return signal from SHARC2 in SPORT format. The data present in this stream is converted to S/PDIF and I^2S formats and mapped via Look-Up Table to the output ports.

SPORT_CLK_B is the serial shift clock for the data present on **DSPBSP3FPGA**.

SPORT_FS_B_N is the frame sync signal for **DSPBSP3FPGA**.

Video Interface

Signals: SYNC_DETECT, OSD_CS/, VIDEO_SCLK, VIDEO_DATA, VIDEO_REG, VID_I2C_DATA, VID_I2C_SCLK

SYNC_DETECT is a signal that indicates the presence or absence of video synchronization from the Video Board. This signal is stored in the Interrupt Status Register at bit 7. There is no interrupt assigned to this signal, so the host processor simply polls this bit for its status.

OSD_CS/ is the chip select for the Fujitsu MB90092 OSD Controller device located on the Video Board. This signal becomes active when transfers are initiated via the Video/OSD SPI interface. Transfer initiation takes place when the two-byte commands for the MB90092 have been written to the OSD Controller RAM. While the transfer is in progress, bit 6 is set in the Serial Interface Status Register.

VIDEO_SCLK, **VIDEO_DATA**, and **VIDEO_REG** comprise the remainder of the SPI interface to the On-Screen Display controller and the video board control logic. Instructions are sent from either the OSD control RAM or the Video control RAM inside the FPGA. The OSD control RAM is used to store the two-byte commands that are sent to the OSD controller on the video board. The contents of the entire RAM are shifted out of **VIDEO_DATA** synchronous with **VIDEO_SCLK** when a byte is written to the lower order byte RAM. A status bit is set in the Serial Interface Status Register while the OSD RAM contents are being shifted out. **VIDEO_REG** acts as a latch enable for the parallel register devices on the video board.

The Video Control RAM stores the instructions for the video logic. The entire contents of this RAM are transmitted when a byte is written to address 6 within this RAM block.

VID_I2C_SDATA and **VID_I2C_SCLK** comprise the I^2C control interface to the video CODEC. The host CPU writes data to storage registers within the FPGA, which in turn is transmitted to the CODEC using the I^2C protocol.

Tuner Board Control Interface

Signals: ADA_TUN_CE/, TUN_RDS_CLK, TUN_RDS_DAT

ADA_TUN_CE/ is a chip select that enables SPI transfers to the Tuner Board. The rest of the SPI port is comprised of **ADA_SDATA_IN**, **ADA_SDATA_OUT**, and **ADA_LATCH** from the Analog Board Control Interface. Currently the tuner board does not utilize a SPI interface, so the chip select signal is not used.

TUN_RDS_DAT is a bi-directional signal that comprises part of an I^2C interface to the Tuner Board. Control register addresses and data are serially shifted up to the tuner board synchronous with the rising edge of **TUN_RDS_CLK**.

Analog Board Control Interface

Signals: ADA_SDATA_OUT, ADA_SDATA_IN, ADA_SCLK, ADA_LATCH, ADA_VC_SEL/, ADA_TUN_CE/, TUN_RDS_CLK, TUN_RDS_DAT

These signals comprise the SPI interface to the Analog Board. Control data to the CODECs is transmitted from the FPGA via **ADA_SDATA_OUT** and status information is received via **ADA_SDATA_IN**. Both signals are synchronous with serial shift clock **ADA_SCLK**. Control data is latched into an eight-bit register on the Analog Board when **ADA_LATCH** is in a high state; this occurs at the end of every sample byte transmitted. **ADA_VC_SEL/** is a chip select that enables SPI transfers to the volume controller devices on the Analog Board. **ADA_TUN_CE/** is a chip select that enables SPI transfers to the Tuner Board. Currently, the Tuner Board does not use SPI control, so this signal is unused.

Analog Board Audio Interface

Signals: REC_ADC_FS/, REC_ADC_FS64/, REC_DAC_FS/, REC_DAC_FS64/, MAIN_FS/, MAIN_FS64/, MAIN_I2S_OUT[4:1], REC_DAC_I2S_OUT, MAIN_I2S_IN[4:1]

MAIN_I2S_IN1 is the serial data stream sourced from the MAIN A/D Converter on the Analog Board to the AVRX FPGA. This I^2S stream is the 24-bit left and right channel data encoded from a selected left/right analog input pair, the phono preamplifier, microphone 1, microphone 2, or tuner.

MAIN_I2S_IN2 is the serial data stream sourced from the C/SUB A/D Converter on the Analog Board to the AVRX FPGA. This I^2S stream is the 24-bit left and right channel data encoded from the number-four left/right analog input pair.

MAIN_I2S_IN3 is the serial data stream sourced from the SIDE A/D Converter on the Analog Board to the AVRX FPGA. This I^2S stream is the 24-bit left and right channel data encoded from the number-five left/right analog input pair.

MAIN_I2S_IN4 is the serial data stream sourced from the REC A/D Converter on the Analog Board to the AVRX FPGA. This I^2S stream is the 24-bit left and right channel data encoded from a selected left/right analog input pair, the phono preamplifier, microphone 1, microphone 2, or tuner. These analog sources are level controlled prior to conversion.

Note that in all cases, the analog sources are level controlled prior to conversion.

REC_ADC_FS/ is the Left/Right framing signal for **MAIN_I2S_IN4** sourced from the AVRX FPGA to the REC A/D Converter on the Analog Board.

REC_ADC_FS64/ is the serial clock for the **MAIN_I2S_IN4** data streams. This is sourced from the AVRX FPGA to the REC A/D Converter on the Analog Board.

MAIN_I2S_OUT1 is the 24-bit serial data stream sourced from the AVRX FPGA to the LEFT/RIGHT FRONT D/A Converter on the Analog Board.

MAIN_I2S_OUT2 is the 24-bit serial data stream sourced from the AVRX FPGA to the CENTER/SUB D/A Converter on the Analog Board.

MAIN_I2S_OUT3 is the 24-bit serial data stream sourced from the AVRX FPGA to the LEFT/RIGHT SIDE D/A Converter on the Analog Board.

MAIN_I2S_OUT4 is the 24-bit serial data stream sourced from the AVRX FPGA to the LEFT/RIGHT REAR D/A Converter on the Analog Board.

MAIN_FS/ is the Left/Right framing signal for the **MAIN_I2S_IN[3:1]** and the **MAIN_I2S_OUT[4:1]** data streams sourced from the AVRX FPGA to the MAIN, C/SUB, and SIDE A/D and D/A Converters on the Analog Board.

MAIN_FS64/ is the serial clock for the **MAIN_I2S_IN[3:1]** and the **MAIN_I2S_OUT[4:1]** data streams. This is sourced from the AVRX FPGA to the MAIN, C/SUB, and SIDE A/D and D/A Converters on the Analog Board.

REC_DAC_I2S_OUT is the 24-bit data stream sourced from the AVRX FPGA to the Record Zone D/A converter on the Analog Board.

REC_DAC_FS/ is the Left/Right framing signal for REC_DAC_I2S_OUT. It is sourced from the AVRX to the Record Zone D/A converter.

REC_DAC_FS64/ is the serial clock for REC_DAC_I2S_OUT.

The Zone 2 left/right VAR and FIX outputs are sourced by the Record Zone D/A converter.

Power Amplifier SPI Control

Signals: CTRL_DATA, STAT_DATA, SER_CLKA, DATA_LATCHA, CTRL_DATB, STAT_DATB, SER_CLKB, DATA_LATCHB

STAT_DATA is the receive path from the four-channel power amplifier. Data from this signal is stored in a 2x8 bit RAM internal to the AVRX, from which the host may determine the ready status and clip status of each channel. The following table illustrates the mapping of the internal RAM.

Address	Bits	Signal
Base + 0	7:0	Control bits [7:0] from the previous SPI cycle
Base + 1	7:4	Clip Indicator for Channels 4:1 (CLIP[4:1])
Base + 1	3:0	Ready monitor for channels 4:1 (RDY_MON[4:1])

Four Channel Status RAM Table

CTRL_DATA is the transmit path to the four-channel power amplifier. Control data from the Host CPU is loaded into an internal 2x8 bit RAM that is in turn serially shifted out to the four-channel amplifier board. The only control data currently being transmitted is in the form of four ready acknowledge bits, each of which activates a relay that places the speaker terminals into circuit with the amplifier outputs. The table on the next page illustrates the mapping of the internal RAM.

Address	Bits	Signal
Base + 0	3:0	Ready control for channels 4:1 (RDY_CON[4:1])
Base + 0	7:4	(Not used)
Base + 1	7:0	(Not used)

Four Channel Control RAM Table

SER_CLKA is the serial shift clock with which the control and status data are synchronous.

DATA_LATCHA is the signal that latches control and status data into registers when a full byte of data has been transmitted or received.

STAT_DATB is the receive path from the three-channel power amplifier. Data from this signal is stored in a 2x8 bit RAM internal to the AVRX, from which the host may determine the ready status and clip status of each channel. The following table illustrates the mapping of the internal RAM.

Address	Bits	Signal
Base + 0	7:0	Control bits [7:0] from the previous SPI cycle
Base + 1	2:0	Ready monitor for channels 7:5 (RDY_MON[7:5])
Base + 1	3	(Not used)
Base + 1	6:4	Clip indicator for channels 7:5 (CLIP7:5)
Base + 1	7	(Not used)

Three Channel Status RAM Table

CTRL_DATB is the transmit path to the three-channel power amplifier. Control data from the Host CPU is loaded into an internal 2x8 bit RAM that is in turn serially shifted out to the three-channel amplifier board. The only control data currently being transmitted is in the form of three ready acknowledge bits, each of which activates a relay that places the speaker terminals into circuit with the amplifier outputs. The following table illustrates the mapping of the internal RAM.

Address	Bits	Signal
Base + 0	2:0	Ready control for channels 7:5 (RDY_CON[7:5])
Base + 0	7:3	(Not used)
Base + 1	7:0	(Not used)

Three Channel Control RAM Table

SER_CLKB is the serial shift clock with which the control and status data are synchronous.

DATA_LATCHB is the signal that latches control and status data into registers when a full byte of data has been transmitted or received.

VCO Clock Control

Signals: MAIN_PLL_PUMP_UP, MAIN_PLL_PUMP_DN, MAIN_PLL_LOCK_DN/, MAIN_PLL_FPGA_MCKO, ZONE2_PLL_PUMP_UP, ZONE2_PLL_PUMP_DN, ZONE2_PLL_LOCK_DN/, REC_DAC_SEL[1:0], ZONE2_PLL_FPGA_MCKO, AUDIO_OSC

The AVRX FPGA uses the output frequency of each VCO implemented on RV-8 as a 512FS master clock at 44.1/48kHz and a 256FS master clock at 88/96kHz. Within the AVRX, the incoming clock frequencies are divided by 512 or 256 and is phase compared to a corresponding frequency derived from the reference clock source. This clock reference is derived from the S/PDIF sample rate, or it can be derived from the fixed crystal reference signal **AUDIO_OSC**. When the incoming master clock is too low compared to the reference, a series of active high pulses are sent to the VCO forcing it to increase the output frequency until a phase match occurs between the reference and the master clock. When the incoming master clock frequency is too high compared to the reference, a series of active low pulses are sent to the VCO forcing it to throttle back on the output frequency until phase match occurs. When the two are matched, a series of low going pulses to the VCO that sustains oscillation at a stable point. Further discussion as to the theory of VCO operation will be made later in this document.

MAIN_PLL_PUMP_UP is an active low signal that forces the master clock to increase in frequency when the master clock rate is lower than the reference frequency.

MAIN_PLL_PUMP_DN/ is an active low signal that forces the master clock from the VCO to decrease in frequency when the master clock rate is higher than the reference frequency.

MAIN_PLL_LOCK_DN/ is an active low signal that keeps the master clock from the VCO at a stable rate of oscillation when the master clock is equal to the reference frequency.

MAIN_PLL_FPGA_MCKO is the master clock output from the VCO for the Main Zone.

A set of analogous signals exists for the Zone 2 PLL circuitry. Their function is exactly the same as their Main Zone counterparts, so further discussion would be redundant. The signals in question are:

ZONE2_PLL_PUMP_UP, **ZONE2_PLL_PUMP_DN/**, **ZONE2_PLL_LOCK_DN/**, and **ZONE2_PLL_FPGA_MCKO**.

The Zone 2 D/A and A/D converter master clocks may be sourced from either the Main or Zone 2 VCOs. Two control register bits within the Clock Source Select #2 register make the source selection. The following table further illustrates the selection conditions.

Master Clock Source Select Table

Master Clock Source Select			
05	03	REC_ADC_MCKI/	REC_DAC_MCKI/
0	0	ZONE 2 PLL	ZONE 2 PLL
0	1	ZONE 2 PLL	MAIN ZONE PLL
1	0	MAIN ZONE PLL	ZONE 2 PLL
1	1	MAIN ZONE PLL (Default)	MAIN ZONE PLL (Default)

Expansion Slots

Signals: EXP[17:0]

The RV-8 has built in capacity for future expansion capabilities. A general purpose 18-bit bus is shared between two expansion ports. To date, the only use for this expansion bus is for a test fixture that may be plugged into either port to test continuity of the signals to the FPGA. Beyond this, there are no clear definitions of signal function for this bus.

FPGA Flash (Sheet 10)

This page contains the configuration FLASH EPROM for the AVRX FPGA, FPGA configuration indicator, the audio reference clock generator, and the Expansion slot connectors.

Configuration FLASH EPROM (U40)

This device is a Xilinx XC18V02 2Mbit 3.3V EPROM that is used to store programming algorithms for the AVRX FPGA. It is packaged in a 44-pin PLCC package. This device is used only during development cycles, and as such is not installed on the Main Board under normal circumstances. In order to use the FLASH as illustrated, the AVRX FPGA must be placed in Master Serial Mode; see the Configuration section on page 6-30 for further details as to how to implement this operational mode.

In Master Serial Mode, the FPGA provides an active low reset signal to the EPROM via *XFLASH_INIT/* which resets the internal address counter of the EPROM to zero. The FPGA then asserts this reset signal high. Once the reset signal is high, the FPGA asserts the EPROM chip select low via *FPGA_DONE*. The FPGA then provides a clock signal to the EPROM via *XFLASH_CCLK,* which causes serial data to be shifted out of the D0 data pin into the FPGA DIN pin; this signal is called *XFLASH_DIN* on the schematic. When configuration has completed, the FPGA re-asserts FPGA_DONE high. This signal is inverted by a single gate inside U38 causing D46 to illuminate upon completion of the configuration operation. This provides a visual cue as to when the FPGA is done.

XFLASH_CF/ is an output pin from the EPROM that allows the programming port connected to the EPROM to configure the FPGA.

Programming Ports

Signals: JTAG_TCK, JTAG_TDO, JTAG_TDI, JTAG_TMS

The EPROM supports boundary scan testing as well as In Circuit Programming via a fully compliant IEEE 1149.1 JTAG Port. J16 is a 1x9 row of pins that can accept a Xilinx download cable. By configuring the FPGA in Slave Serial Mode, J15 may be used as an In Circuit Programming port that will directly configure the FPGA, bypassing the EPROM.

Typically during development, the EPROM is socketed for easy removal and insertion and the EPROM is programmed in a standard PROM programmer.

Audio Reference Clock (U35)

AUDIO_OSC is a reference signal that is used by the PLL phase comparators within the AVRX device. It is used as a reference when no sample clock is derived from the S/PDIF inputs. U35 is a standard Unbuffered Hex Inverter of which one stage is configured as a Colpitts Oscillator comprised of Y1, R145, C140, and C141. This circuit generates a 14.112MHz square wave. R145 provides hysteresis for the gate, initiating and sustaining a reliable switching characteristic, while C140 and C141 provide the proper AC load to the reactive element of Y1. The second stage of this circuit is another gate from the hex package that simply buffers the output of the oscillator, presenting a minimal load to it while providing drive capability. R147 provides source impedance matching to the characteristic impedance of the PCB.

FB15 provides a cleaner 3.3V supply to the oscillator, minimizing contamination of the output clock signal by the switching characteristics of other devices connected to the 3.3VD plane. C142 is a standard high frequency de-coupling capacitor for U35.

Expansion Slot Connectors (J25, J30)

J25 and J30 are connectors that will provide system inter-connectivity for accessory boards that will enhance product capabilities. An eighteen bit wide bus from the FPGA is source impedance split into two different paths to the connectors. These signals are currently bi-directional in nature and have no clearly defined function as of yet.

J25 and J30 are 34-position Flat Flex Cable Connectors (FFC) that provide a 5VD supply to the expansion card via four pins. The contact impedance of the connector pins to FFC cable is such that future expansion cards should not draw more than one amp of current from the 5VD supply. Ground and signal return path is provided via ten pins on each connector. J25-3 is an active low reset signal **EXPA_RESET/**, while J30-3 has a separate active low reset signal **EXPB_RESET/**. Both resets are Host Processor controlled and allows each expansion slot to be reset independently.

Expansion Port Series Terminations (Sheet 11)

This page further illustrates the source impedance splitting of the expansion bus mentioned in the preceding section. RP29-RP37 provide source impedance matching for each of the eighteen bus signals originating from the AVRX FPGA. Each signal connects to two resistors, the opposite ends of which connect to J25 and J30. The effect is that the bus is shared between both connectors, but each slot has it's own impedance path back to the FPGA pins.

Board Interconn/Debug (Sheet 12)

This page contains all of the off-board interconnections to the Front Panel Board, Video Board, Analog IO Board, and Amplifier Modules. This page also contains the Debug and User Access RS-232 terminal ports.

RS-232 Transceiver (U5)

U5 is a Maxim MAX202E dual RS-232 Transceiver that runs on $5V_{DC}$ whereas most transceivers need +/-12 V_{DC} to accommodate the +/-10V swing intrinsic to RS-232. This device uses charge pump voltage conversion to accomplish this. C28 doubles the 5V present in the circuit to 10V, storing it on C27. The second charge pump inverts the +10V to –10V, storing it on C30. Using this technology, the output drive capability on pins 9 and 12 is +/-8V when loaded with a nominal 5K-Ohm RS-232 receiver. This conforms to the EIA/TIA-232E and V28 specifications for RS-232.

The debug transmit signal DEBUG_TXD from the CPU drives pin 11 of U5. This driver is output as TXDA on pin 14, and is ferrite bead de-coupled to remove spurious high frequency noise before being output on J4.

Signals received from the debug terminal enter the system via J4 pin A3. This signal is ferrite bead de-coupled to remove spurious high frequency noise, which drives U5 pin 13 as the signal RXDA. The output of this driver provides the receive signal to the Host CPU as DEBUG_RXD from U5 pin 12.

The user transmit signal USER_TXD from the CPU drives pin 10 of U5. This driver is output as TXDB on pin 7, and is ferrite bead de-coupled to remove spurious high frequency noise before being output on J4.

Signals received from the user terminal enter the system via J4 pin B3. This signal is ferrite bead de-coupled to remove spurious high frequency noise, which drives U5 pin 8 as the signal RXDB. The output of this driver provides the receive signal to the Host CPU as USER_RXD from U5 pin 9.

W1 and W2 are test points for ease of debug.

C12-C13 provides a high frequency path to ground for noise entering the system from the outside world.

DSR and RLSD signals from the terminals are not used, and so they are pulled up to +5VD via R21-R24.

J4 is a dual stacked DB9-F connector; DB9 is the standard profile for RS-232.

Analog Board Connector (J26)

J26 is a 40 position Flat Flex Cable (FFC) connector. All digital audio streams and their associated clocks are either sourced from the FPGA to the Analog Board, or they return to the FPGA from the Analog Board. Detailed description of these signals may be found on page 6-37. Signals not previously discussed or bearing special consideration are as follows:

RESET is an active high signal generated by Reset Generator U31. It provides power-up reset to the Analog Board and is the only positive going reset signal in use in the RV-8 system.

Amp Board Connectors (J18 and J22)

J18 is a 14 position FFC connector that provides interconnection with the Crown Four Channel Amplifier Module. A ferrite bead de-coupled 5V is supplied to the module to power the SPI control logic. The ferrite is necessary for the suppression of parasitic frequencies that would compromise the RFI integrity of the amplifiers. The SPI port signals SER_CLKA, CTRL_DATA, STAT_DATA, and DATA_LATCHA are discussed in greater depth on page 6-38 and will not be expanded upon here.

Each channel amplifier contains a thermistor that monitors heat sink temperatures local to each channel's output transistors. This information is provided to the A/D inputs of the Host CPU in the form of a voltage that increases proportionally with temperature. TEMP[4:1] are the voltages for the four channel module. See page 6-12 for more information.

J22 is the same form factor as J18, and performs the same function. The only difference is that this component provides interconnectivity with the Crown Three Channel Amplifier Module. TEMP[7:5] provides temperature monitoring to the Host CPU in the same manner as on the four channel module.

AMP_RESET/ is a buffered equivalent active low reset signal as provided by Reset Generator U31. This is used to clear the SPI logic on the modules to zero.

SPARE_AD is intended as a monitoring signal for the amplifier power supply. To date, this has not been implemented in the design.

Front Panel Connector (J20)

J20 is a 40 position FFC connector that conveys all the signals necessary to control and report status of the front panel LED array, the pushbutton array, the rotary encoder, and the Vacuum-Fluorescent Display.

FP_RESET/ is a buffered equivalent of the active low reset signal generated by U31. This signal is used to reset the state machines controlling the LED matrix, and the switch status.

SYSTEM_ON_LED is a buffered equivalent of the SYSLED signal, which is driven directly by the Host CPU. The *SYSTEM ON LED* is one of three LEDs located behind the VFD lens on the front panel.

OVLD_LED is a buffered equivalent of the OVLED signal, which is driven directly by the Host CPU. The *OVERLOAD LED* is one of three LEDs located behind the VFD lens on the front panel. U15 provides the buffered signals from the CPU to the Front Panel Board.

FP_IR_BLINK is a repeater signal from the ZONE 2 remote control detector plugged into the back of the RV8. This signal causes an infrared LED to blink which in turn is sensed by the front panel IR detector.

FP_IR_BLINK_RET is the return current path from the front panel infra-red LED.

FP_IR_IN1 is the output signal from the infra-red detector on the front panel. Whenever a signal from a hand held remote control is detected, the IR detector outputs a Hamming Code signal to the AVRX FPGA which then decodes the command. The Host CPU then reads and processes the code accordingly.

FP_IR_ACK is a signal driven directly from the Host CPU to a front panel LED indicator. This LED flashes whenever a hand-held remote control access has been made. It serves as a visual verification that the remote signal is being received.

FP_ENC(A,B)_IN are rotary encoder output signals. R172-R175, C165, and C170 are low-pass filtering and pull-up networks for these quadrature signals. See page 6-30 for further information regarding these signals.

FP_SDATA_IN is the signal by which the AVRX FPGA receives data back from the CPLD on the Front Panel Board with regards to the status of the pushbutton array

FP_SDATA_OUT is the signal by which the AVRX FPGA transmits data to the CPLD on the Front Panel Board in order to write to the LED array.

SDATA_CLK is the clock signal that controls the serial shift of data up and back from the FPGA front panel.

FP_SDATA_LTCH is a signal that marks the beginning of an eight bit sample being transmitted to the front panel.

All four of these signals comprise the SPI interface to the front panel.

DISP_RS is an address decoded bank select for the VFD.

DISP_RW is an address decoded read/write strobe for the VFD. When this signal is high, the VFD registers are in read mode. When low, the registers are in write mode.

DISP_E is an address decoded global enable of the VFD.

FP_D[7:0] is an eight-bit data bus to the VFD. All register accesses to the VFD are made via this bus.

FPSWITCH[3:1] are breakout signals from the RIGHT MODE, MAIN DVD2, and ZONE 2 DVD2 buttons on the front panel. The Host CPU monitors these signals. The boot-up state of these switches determines the operational mode RV8 will enter once boot-up is complete. See page 6-8 for further details.

Supply voltages +3.3VD and +5VD are both needed to power the Front Panel Board. The IR/ENCODER Board, VFD, and LED matrix are powered by +5VD, while the CPLD is powered by +3.3VD.

Video Board Connector (J29)

J29 is a 16 position FFC connector that conveys all the signals necessary for Host CPU access to the on-board FPGA and the Video Decoder/Encoder components.

VIDEO_RESET/ is a buffered equivalent of the active low reset signal generated by U31. It provides an initiating signal to the state machines within the FPGA on the Video Board.

SYNC_DETECT is a signal that indicates the presence or absence of video synchronization from the Video Board.

OSD_CS/ is the chip select for the Fujitsu MB90092 OSD Controller device located on the Video Board.

VIDEO_SCLK is the serial data shift clock that comprises the SPI interface to the OSD and control logic.

VIDEO_DATA is the serial data that is part of the SPI interface to the Video Board.

VIDEO_REG comprise the remainder of the SPI interface to the On-Screen Display controller and the video board control logic.

VID_I2C_SDATA is a serial data stream that communicates to the Video Codec using I^2C protocol. Provision is made for a pull-up resistor R180 for compliance with the I^2C specification. The equivalent resistor is already populated on the Video Board, and hence is not needed here.

VID_I2C_SCLK is the serial data stream shift clock that communicates to the Video Codec using I^2C protocol. Provision is made for a pull-up resistor R181 for compliance with the I^2C specification. The equivalent resistor is already populated on the Video Board, and hence is not needed here.

CVID_ZON3 is a composite video analog signal that is sourced from a video selector that selects between one of five composite inputs or one of five S-VIDEO inputs on the rear panel.

Amp Power Supply Connector (J27)

J27 is a 6 position FFC connector that provides enable controls for the Amplifier Power Supply Board Relays that activate the power amplifiers. This connector also provides a BROWN_OUT signal to the Host CPU, where it is monitored as a Non-Maskable Interrupt (NMI). Provision is made to use conventional ribbon cable for board interconnect via J28, but to date is not used in this design.

SOFT_RLY is a signal that is activated from the external registers on sheet 2. This signal enables a current limited supply voltage to the power amplifiers during the final stages of boot-up. During this phase of the boot process, readiness status is queried of each of the amp channels by the Host. This relay signal returns to the inactive state if a problem is found within the amplifier blocks, and also when the power supply has stabilized and current limiting on the supply rails is no longer necessary.

MAINS_RLY is a signal that is also activated from the external registers on sheet 2. This signal enables the full supply to the amplifiers once the state of the amplifier channels are known to be good. This relay activates before the SOFT_RLY signal is made inactive.

BROWN_OUT is a monitoring signal from the amp power supply that will trigger an NMI if the power supply rails drop by more than 10% of their nominal voltage. This will place the RV-8 into a standby mode with the amplifiers shut off until the supplies have stabilized.

S/PDIF IO (Sheet 13)

The AVRX FPGA receives eight S/PDIF streams from the back panel. Four are from coaxial sources requiring signal conditioning and amplification. The remaining four are from optical sources that go directly to the FPGA. Record S/PDIF outputs are available as a single coax and a single optical signal. This page also illustrates the Zone 3 video output.

Coax S/PDIF Inputs

J1 and J2 are dual stacked RCA connectors. Each input is protected by a spark gap, providing a path for ESD discharges made to the connectors. C1/R1, C3/R2, C5/R3, and C7/R4 present a standard impedance to the incoming S/PDIF signals. C2, C4, C6, and C8 provide AC de-coupling for each of the signals as they enter the amplifier stage.

D1-D4 provide diode clamp protection of the amplifiers by ensuring that the input stages are never subjected to voltages greater than 5V nor lower than DGND. U3 and U4 are configured as amplifiers by R5-R12 by forcing the gates to run in a semi-linear region. The effective result is that each input gate acts as an amplifier with a gain of 10, increasing the amplitude of the input stream from 0.5V to 5V. The second gate in the signal chain acts as a simple buffer, providing a minimal load to the amplifier stage thereby preserving stability.

Optical S/PDIF Inputs

CP1-CP4 are standard TORX style optical receivers. No additional signal conditioning is required for these signals, and as such they are presented to the AVRX FPGA right from these inputs.

Record Zone S/PDIF Outputs

A digital audio output for the Record Zone is sourced from the AVRX FPGA to a 74VHCT244 Octal Buffer U2. Two out of the available eight buffers are actually used. The first output drives a TORX style optical output connector. The second buffer output drives a voltage divider that reduces the CMOS level of the signal to one of approximately 1.2V in amplitude. C18 and C19 provide wave shaping and impedance compensation to the signal before being output through RCA coax connector J8. This output network conditions the CMOS signal to standard S/PDIF specifications. J8 is protected from ESD by a spark gap.

Zone 3 Composite Video Output

J7 accepts a composite video signal from the Video Board and passes it to the outside world. J7 is spark gap protected.

Trigger Outputs (Sheet 14)

The RV-8 provides two $12V_{DC}$ voltage sources for remote powering external accessories in the user's home theater. Each trigger output can provide up to 1 Amp to an external load.

U8 is a low drop-out adjustable regulator. It is powered by +15V while it's output voltage is set by R15 and R16, following the equation:

$V_O = 1.275[(R15 + R16) / R15]$

C25 provides local bulk capacitance for the voltage input. C22 is a low ESR type capacitor which provides stability for the regulator and bulk capacitance for the output voltage. R13 and R14 provide a current path for any load that would source current when shut off, as U8 cannot sink current. FB1 and C10 provide suppression of high frequencies, preventing EMI effects. J3 is the output connector which is protected by a spark gap.

The regulator provides the external 12VDC when the ON/OFF pin is brought to a logic 0. This pin is software controlled via the external registers on sheet 2. See page 6-23 for further information. Inverter U14 permits us to use positive logic in the software register.

This circuit is duplicated exactly with U9 and all associated components.

VCO A (Sheet 15)

The purpose of the VCO is to provide clean, stable clock that matches the average properties of a potentially unstable reference, such as jitter. At the heart of the circuit is the metal-encased VCO module, which provides an output clock at 22.579MHz or 24.576MHz depending on the control voltage. The control voltage should fall between 5V and 6V.

The 700mVpp output of the VCO is amplified by one gate of U10 to a 5V logic level. This gate is self-biased in the middle of its inverting characteristic by R41, R42, and C49. Another gate of U10 is used to invert and buffer the output signal of the conditioning circuit. R43 provides source impedance termination to reduce overshoot.

The output of the VCO is sent to the AVRX FPGA via **MAIN_PLL_MCKO**. This is used as a 512FS master clock in 44kHz or 48kHz mode, and a 256FS master clock at 96KHz. The FPGA divides this clock down to 44/48/96kHz and the result is phase and frequency compared to a corresponding frequency from a selected reference, such as the derived clock from an S/PDIF stream or the local crystal oscillator. When **MAIN_PLL_MCKO** is too low relative to this reference, the FPGA generates a series of active low pulses to the PLL Error Amplifier U11 via **MAIN_PLL_PUMP_DN/**. If **MAIN_PLL_MCKO** is too high relative to the reference, the FPGA generates a series of active high pulses to the PLL Error Amplifier via **MAIN_PLL_PUMP_UP**.

The PLL Error Amplifier U11 is biased at 2.5V via the voltage divider comprised of R38 and R39. The pump up/down pulses from the FPGA are buffered by U19 and connected to schottky diodes D18 and D19. When no pulses are asserted, the diodes are reverse biased and no current is injected into the summing node of U11. When the VCO frequency is too low, D16 will be forward biased by the **UPA/** pulses, asserted low by U19. The resulting current through R46 will be integrated by feedback capacitors C41 and C42. This will cause a progressively higher voltage at test point VCOVA. This is the control voltage to the VCO module; as this voltage rises, it causes the VCO output frequency to increase. R40 smoothes out the transient response of the feedback loop.

When **MAIN_PLL_MCKO** has reached equilibrium with the reference clock, the pump up/down signals are inactive. The FPGA delivers a series of active low pulses to the error amplifier via **MAIN_PLL_LOCK_DN/**. The average duty cycle of these pulses is approximately 1/128. Instabilities such as jitter in the reference will appear as variations in pulse width, but the instantaneous variation gets averaged by the action of the loop filter. The result is a steady control voltage to the VCO that produces a high stability frequency based on the average frequency of the reference.

When a lock down pulse forward biases D20, current flows through R48, which is integrated by C48. R49 provides a constant current of opposite polarity, which also gets integrated. The two integrals oppose each other, and when the net current into the summing node is zero, the voltage at U11 pin 1 remains constant. If the duty cycle of the pulse is too small, the voltage is driven progressively lower. If the duty cycle is too high, the voltage is driven progressively higher. The resultant voltage is applied to R47, which sinks current from the summing node of the loop integrator, which raises the VCO control voltage. This gets counter-acted by current pulses through D17 and R44. When the integral of these two currents balance, the control voltage remains constant, so the VCO output frequency remains constant, and the loop is stabilized and locked.

D16 prevents the control voltage from going much below 2V, ensuring that the VCO is never driven to a non-oscillating state. D21 prevents the duty cycle integrator from being driven to the wrong polarity when the loop is out of lock.

VCO B (Sheet 16)

Sheet 16 replicates the VCO and PLL circuitry on sheet 15 for Zone 2. Further enhancement of details will not be made here.

Power Supply (Sheet 17)

Power Entry Connector (J31)

Power is brought onto the PCB via J31, a Molex style connector rated for high current. C167-C169 provide de-coupling of the +5VD supply at a wider range of frequencies than could be achieved with a single high value capacitor. All of the logic supply voltages are derived from +5VD. The +/-15V rails are de-coupled by C171-C176 in the same manner as the +5VD rail. These supply voltages are used to derive power for both VCO circuits, output triggers, and environment fans. Chassis Ground is picked up by LUG1, which provides mechanical contact with the chassis via the rear panel.

2.5V Regulator (U12)

This regulator provides a supply voltage for the AVRX FPGA core and for the Decoder DSP core. It is derived from +5VD via an LM2937. This device is a fixed output voltage regulator specified at 2.5V. It is rated for 500mA current, which is far less than the required current. C54 provides local bulk capacitance to the regulator input while C53 provides it for the output.

3.3V Regulator (U38)

U41 is a fixed output voltage regulator that provides a 3.3V supply to most of the logic on this board. It is derived from +5VD. C158 provides local high frequency de-coupling to the input while C122 provides local bulk capacitance to the output. L1 and C123 form a low-pass filter to provide a cleaner supply to the 3.3V. It has been determined that this precaution is not needed in this design, and so these components are not used. W6 provides a zero ohm path from the 5VD supply to the input of U38. Diode D48 ensures that the output voltage never assumes a level higher than +5VD, which could cause destruction to U38.

Fan Control Circuitry

U47 inverts the pulses supplied by one of the PWM timer circuits inside the Host CPU. R179 acts as a default pull-down for Q1 in the event that there is no signal source connected to U47 and the output achieves an indeterminate state as a result. This prevents the fans from turning on in the absence of a control voltage. R177 provides current limiting to the base of Q1. When positive current flows into the base of Q1, the transistor saturates, effectively pulling the gate of Q2 low. When a logic zero is applied to the base of Q1, the transistor appears as an open circuit to the gate of Q2, causing it to conduct from the drain to the source. The drain of Q2 follows the input signal **FAN_DRV**. D49, L2, and C178 act as a full wave rectifier and filter that produces a DC voltage proportional to the duty cycle of **FAN_DRV**. This voltage will vary between 3V and 11V. The environment fans are driven from the +15V supply with this control voltage present on the other side of the fan windings. Therefore, the fans will run on voltages from 4V to 12V, dependent upon the duty cycle of **FAN_DRV**. Connectors J21, J23, J24, and J32 are connected in parallel so that all four fans are controlled by the same signal. L3 is a provision to keep brush noise from the fan from getting into the +15V supply. It has been determined that this protection is unnecessary, and so it is not installed. R182-R186 Provide a total resistance between +15V and the fans of approximately 10 Ohms capable of dissipating 1.25W. This resistance suffices to suppress back EMF from the fans. C177 provides local bulk capacitance for the circuit.

IR Remote Connector (Sheet 18)

This page contains the IR detector input for ZONE 2.

ZONE 2 Remote Input

Remote control of the RV-8 is made possible via an infra-red detector behind the front panel lens. Control from the Main Zone is made by pointing the remote at the front panel and activating functionality on the remote control surface panel. Remote control for a second zone is made possible by connecting an IR detector to J5. When commands from the remote strobe this external detector, the resultant signal is passed along to an infra-red LED located in close proximity to the main zone detector. This LED is also located behind the front panel lens. The result is that the serial commands made by the remote control from ZONE 2 are repeated by the front panel IR LED which in turn are received by the front panel detector. J5 is spark gap protected and diode clamped by D5 and D6. R25 and R26 form a voltage divider to properly bias the IR LED.

Provision is made for a third zone of remote control, but this has not been implemented in this product. In this case, signals passed along from the external detector via J6 activate IR LED D8 which are then received by IR detector U1. Both components are located in close proximity inside the unit chassis. The output from the detector is passed along to the AVRX FPGA for further processing and signal conditioning.

Bypass Capacitors (Sheet 19)

This page illustrates the distribution of capacitive de-coupling for each of the supply voltage zones. Of the six voltage planes used in this project, the 3.3VD supply is larger because a far larger percentage of the design uses 3.3V logic. This plane, therefore, has more in the way of high frequency de-coupling as well as evenly distributed bulk capacitance.

The 5VD plane area is the next largest. It primarily supplies the Host CPU and its support memory.

The 1.8V planes are for the core voltages used by the Hammerhead SHARCs.

The 2.5V plane area supplies the core voltages for the AVRX as well as the Format Decoder.

The +/-15V supplies are used exclusively by the two PLL circuits.

RV-8 PHONO / MICROPHONE INPUT BOARD THEORY

The Phono / Microphone Input Board contains the circuitry for the phono and mic input preamplifiers. This board is located in a metal tray with the Tuner Board attached to the back panel.

The outputs from the preamps are sent to the Analog Board via a flat flex cable and eventually to differential buffers on that board. All unbalanced “+” signals are sent with a local ground reference as a “–” to form a differential pair.

Phono Inputs

The phono is designed as a two stage RIAA filter circuit. The first operational amplifier takes care of the 50Hz and 500Hz breakpoints, while the 2122Hz rolloff is accomplished by the passive network R35, R44, and C37. The second amplifier supplies an additional 19.5 dB of gain. Using two amplifiers results in accurate conformance to the RIAA curve as well as lower distortion due to the fact that each amplifier is operating at a lower gain than would be the case in a single-amplifier design.

D10 and D13 diode networks prevent the large signals that come from phonograph needle dropping to get into the mux circuitry on the analog board. C31, C38 and C45 for a third order high-pass circuit at around 8Hz to block the low frequency rumble sounds. A tap is provided after the first opamp section. This output is labeled 75uS_R/L because it does not include the 2122Hz / 75uS time constant rolloff filter, which is useful to provide high frequency rich signals for click and pop detection algorithms.

Microphone Inputs

The circuitry here supplies power (9 volts) to an external microphone capsule, and performs balanced to unbalanced conversion and amplification. The input op amp is protected from the common-mode phantom power by 10uF input capacitors and an inductor-capacitor RFI filter network. This op amp is unity gain and rejects common-mode noise from a differential microphone signal. The second op amp amplifies the signal by 25.5dB. A diode network prevents microphone accidents from creating a large signal that could clip the muxes on the analog board. A 100 ohm resistor pair isolates the output from reactive loads.

Microphone “Phantom” Power Supply

Power is pulled from the +15V supply and regulated down to 9 volts by a voltage regulator. Diode D8 prevents back-biasing the regulator when +15V is removed. An RC filter is created by 330 ohms and 10uF. The 2.2K resistors provide current limiting and define the input impedance that the microphone sees at the input of the amplifier.

RV-8 TUNER BOARD THEORY

This section provides a detailed description of the design theory embodied in the RV-8 Tuner Board. Each section of this document will discuss the theory of each functional subset of this board and will reference a schematic sheet for each block. The schematic set being referenced is at a minimum revision level of 1.

- The RV-8 Tuner Board incorporates the following features:
- AM Stereo decoding
- Station identification via the front panel
- Radio Data Stream decoding (RDS)
- Inter-station noise muting

Overall Design Theory

The entire design of the Tuner Board fits on one schematic sheet. Each functional block is discussed separately.

Antenna Input (J1)

The antenna connectors comprise separate inputs for AM and FM. The AM terminals are standard thumbscrew types that will accept twin-lead cabling, such as found on the antenna included as an accessory shipped with the RV-8. FM is brought into the tuner via a 75-ohm F-type connector. FM signals may be provided to the tuner via cable television service, or with the use of a 75/300 ohm Balun transformer and a Y-style twin-lead antenna. The signals are mixed down to a single path into the UT1384 tuner module by inductor L1, which provides a low impedance path for AM signals, and C1, which provides a low impedance path for FM signals. The entry point into the tuner module acts as a

voltage-summing node. The common side of each antenna terminal is tied directly to the rear panel chassis via LUG1.

Tuner Module (U4)

The heart of the design is the Microtune UT1384 Tuner module. This device provides all RF descrimination and provides as outputs AM program material in analog audio format, multiplexed FM program material in the form of an analog signal, and Radio Data Stream (RDS) material in the form of an analog signal. The RDS output provides both RDS data and multiplexed FM material on the same pin. The module also provides a field strength signal in the form of a proportional DC voltage at pin 15. Incoming signal strength and quality are further represented by the AF_SAMP and AF_HOLD signals (pins 20 and 19, respectively). These signals are used to control an off-module sample and hold that will store the average value of the analog signals output by the module. The processor chip U2 contains the sample and hold function. A reference signal of 75.4kHz is available for external processing via the FREF pin (pin 21). This signal is typically divided down to 38kHz and 19kHz to provide demultiplexing of the RDS signal information and the left and right audio samples of the FM program material, respectively. CPU command and control to the module is provided via an I^2C bus, comprised of a serial data stream SDA (pin 11) and a serial shift clock SCL (pin 10). Station selection via the on-board PLL synthesizer, as well as selection of AM or FM programming, is accomplished via this I^2C bus.

Two voltage supply rails are present on this module. VCC5 (pin 5) is a standard 5V supply input that powers the digital logic inside the module, while all of the analog functionality, such as the PLL synthesizer, signal strength, and signal quality control is powered by VCC8P5 (pin 6). This is an 8.5V DC supply. The five volt rail is de-coupled by C10 and C11, while the 8.5V rail is de-coupled by C8 and C9.

The AM AF signal, FM MPX, and the FM/RDS signals are AC coupled to the CRISP processor (U2) via C3, C5, and C2 respectively. R2 and C4 form a de-emphasis filter for the FM MPX signal, but as we are decoding this from the combined FM/RDS stream, this option is left unused. R1 provides the FM/RDS signal to both the RDS and FM inputs of U2.

Signal Processor (U2)

The signals provided by tuner module U4 are processed by U2, a Philips TEF6892H device. This is a signal processor with on-board DSP that is intended for use in car audio systems. Although signal paths for Cellphone, CD player, and Cassette Tape are provided, they are unused in this application. All radio signal de-multiplexing and enhancements are made via this device. The AM signal is processed to remove noise caused by external sources, such as AC line disturbances and path loss, and gain controlled based upon the signal strength as provided via the LEVEL signal (pin 1). AM is introduced into the device via pin 7, and the FM/RDS via pin 6. The AFSAMP and AFHOLD (pins 10 and 9, respectively) are provided with the sample and hold control signals from the tuner block, and in conjunction with the LEVEL pin, are used to provide an average voltage of the radio signal levels, which in turn determines signal strength. The FREF signal from the tuner is introduced by pin 11, and is internally divided down to provide the de-multiplexing pilot signals for FM and for the RDS. Volume and Equalization are controlled within U2 via the I^2C bus pins SDA and SCL (pins 42 and 43, respectively). This is the same bus that provides control of the tuner module. A gated equivalent of this bus is provided via SCLG and SDAG (pins 3 and 4, respectively) and are provided a path to the tuner module by R4 and R7. This was to accommodate using a single register set to control all functionality on the board, but as it was determined to not be necessary, this option remains unused. R5 and R6 pass the I^2C bus along to the tuner block. The I_2C bus provides CPU control of the radio signal AGC and indication of stereo signal detection, as well as capabilities to provide overall signal level and equalization control at this level of implementation.

Left and Right audio signals are presented to the rest of the RV-8 system via LFOUT and RFOUT (pins 27 and 28, respectively). C12 and C13 provide an AC couple path to the output of the board, while R8 and R9 ensure equal path impedance for these signals. R16 further balances the common return path for the output signals. C14 and C15 provide a high frequency roll-off for noise in conjunction with R8 and R9. C20 provides storage of a reference voltage used by the internal D/A converters in the control path of U2.

C18 and C19 provide de-coupling for the 8.5V supply voltage that powers U2.

Output Connector (J2)

J2 is the only system-wide interface to the tuner module. A bulk supply of 12VDC is provided to the PCB via pin 3 of J2. This bulk voltage is noise filtered by FB1. Pins 4 and 6 provide the LEFT and RIGHT stereo signals from the tuner to the rest of RV-8, while the common return path for both of these is provided by pin 5. Pins 12 and 13 provide the I^2C bus that controls the tuner system. RDS data is fed back to the system CPU on these lines as well. R14, R15, C6, and C7 provide standard I^2C pull-up and edge control as described in the Philips specification for I^2C.

MH1 is a plated-through hole that connects to Chassis Ground at the opposite end of the PCB from LUG1. The RV-8 system provides a ground path on this pin, and by keeping it independent from the Tuner functionality and tying it to Chassis Ground here, we ensure minimal radiated EMI from the unit.

Rail Supplies (U1 and U3)

U1 provides the analog supply voltage to the tuner module and the CRISP processor. R12 and R13 program the low drop-out regulator U1 to derive 8.5Vdc from the bulk 12Vdc provided. C17 provides bulk de-coupling capacitance of this output supply voltage.

U3 provides the digital supply voltage to the tuner module. R10 and R11 program the low drop-out regulator U3 to derive 5Vdc from the bulk 12Vdc provided. C16 provides bulk de-coupling capacitance of this output supply voltage.

C21 bulk de-couples the 12Vdc driving both regulator circuits.

RV-8 VIDEO SYSTEM THEORY

The RV-8 video section consists of three major functional blocks: video switcher, video converter, and on-screen display generator (OSD).

The video assembly consists of three boards, the Video In Board (schematic 060-15509), the Video Out Board (schematic 060-15519) and the Video Board (schematic 060-15589).

The RCA input and output boards connect to the main board via flexible ribbon connectors, with most of the active circuitry contained on the Video Board. Video input and output connectors are mounted directly on the boards, which attach to the rear panel of the RV-8. Separate cables supply power and control signals to the video assembly. Control from the main board is implemented via a serial interface.

Composite video inputs (Video In board schematic sheet 1)

Specific references are to input 1; other inputs are similar. Standard video levels applied to RCA jack J5 develop 1Vp-p is across 75-ohm termination resistor R15. Emitter-follower Q5 is located close to the connector and buffers the input with a gain slightly less than unity. Transistor bias is supplied through R13. Buffered video is fed to pin 10 of ribbon cable J6 through low-value series resistor R14, which reduces high-frequency peaking in the transmission path to the video board.

Composite video outputs (Video Out board schematic sheet 1)

Composite video outputs originating on the video board are fed through individual pins of J5 to the corresponding output RCA jacks. The on-board traces are controlled-impedance and form part of a 75-ohm wideband transmission system, and output level is 1Vp-p when terminated in 75 ohms (2Vp-p open-circuit).

S-video inputs (Video board schematic sheet 1)

Specific references are to input 1; other inputs are similar. S-video luminance inputs (pin 3 of the mini-din jacks) are terminated and buffered the same as composite inputs. AC-coupling is applied after buffering; C25 couples s-video #1 luminance. Chrominance input #1 (pin 4 of mini-din jack J15) is first ac-coupled by C24, and then buffered by emitter follower Q19. The dc-level at the chroma input pin is direct-coupled to subsequent sense circuitry through the voltage divider formed by R70 and R71.

Main (Monitor) Composite / S-video (Video board schematic sheet 2)

Composite and S-video luminance connect to multiplexers U20, U21, and S-video chrominance connects to U22. The composite multiplexer is addressed by the MVID_SELn bits, and the S-video multiplexers are addressed by the MSVID_SELn bits. When MCVID_EN/ is asserted low, U18 is enabled, and all MSVID_SELn bits are forced to 0 by logic in CPLD U14 (sheet 9). Composite multiplexer U20 selects one composite source. With MSVID_SELn set to 0, the s-video path is disabled because U21 is selecting a disconnected input, and U22 is selecting a grounded input to feed the chrominance channel. When MCVID_EN/ is high, U20 is disabled, disconnecting the composite inputs, and U14 passes addresses to the MSVID_SELn bits, allowing U21 and U22 to select one of the S-video sources. The composite/luminance (MY) signal from U20/U21 is amplified by non-inverting stage U28. R207 makes the gain be slightly greater than the desired factor of two in order to make up for slight losses in other stages. The signal from U28-1 is fed through R204 to the sync-stripper and dc-restorer (sheet 8). The dc-correction signal BPCOR returns through R206 to close the dc-feedback loop and maintain the video back-porch near 0Vdc. The signal OSD_Y_IN is distributed to output amplifiers U16, U27, and U38, and also feeds the on-screen display (sheet 7).

Chroma selected by U22 (MC) is ac-coupled by C127 and amplified by U28, also with gain slightly greater than two. With a composite source selected, U22 is forced to input 0, grounding the chroma channel. The signal OSD_C_IN is distributed to output amplifiers U15, U27, U38, and U5, and also feeds the on-screen display (sheet 7).

The dc-level on the chroma channel of the selected source is fed to two dc amplifiers through multiplexer U23, filtered by C5. The overall gain of the dc path from the chroma input is unity, such that the dc voltage on the chroma input is buffered and can be applied to the chroma output.

The amplifier formed by Q5, Q6, and Q4 applies dc to the chroma of the S-video 2 output, and Q8, Q9, and Q7 applies dc to the chroma of the S-video 1 output. Each dc path can be selectively enabled by the MORPHEN/ and MORPHEN1/ logic levels. A high logic level disables the amplifier and no dc voltage is added to the corresponding chroma output. The purpose of the dc amplifiers is to transfer the dc voltage at the input to the output, to accommodate different S-video aspect ratio switching schemes that rely on different dc-voltages.

Main S-video at J4 is driven by gain-of-one amplifiers U16 (luma) and U15 (chroma). Internal multiplexers in these amplifiers determine whether the s-video is taken from the OSD path (MSTHRU/=hi) or straight through from the input amplifiers (MSTHRU/=low). MSTHRU/ follows MTHRU/ unless MSVID_YOFF is asserted by logic in CPLD U14 (sheet 9). MSVID_YOFF allows main s-video luminance to be shut off by U40 (sheet 7) when a composite source is in use. Amplifier outputs are fed through 75-ohm series resistors (R145, R142), forming a matched transmission-line driver system. R144 and R141 compensate for slight impedance errors due to the resistance of the on-board connecting traces. The chroma output is ac-coupled by C80, with a dc-level introduced through R18, according to the action of the associated dc amplifier.

Main S-video at J3 is driven by gain-of-one amplifiers U27. S-video at J3 is not subject to the OSD and is not selectively disabled when composite video is in use.

Main composite video CVID_MAIN1 is driven by U38. Luma and chroma from the input amplifiers are summed by R211 and R212, scaled by ½ and the result is amplified by U38, which has a gain of two. With composite input, there is no chroma, and the result is simply the composite video. With S-video input, the result is the composite version of the S-video, the sum of Y+C. The internal U38 multiplexer selects whether the OSD is in the path or whether the input is fed straight through, controlled by MTHRU/. Output impedance is structured as with the main luma output.

Main composite video CVID_MAIN2 is driven by U5. Luma and chroma from the input amplifiers are summed by R126 and R127, scaled by 1/2, and the result is amplified by U5, which has a gain of two. CVID_MAIN2 is not subject to the OSD.

Standard 1Vp-p video input levels produce 1Vp-p output on the composite and luminance channels when terminated in 75 ohms, or 2Vp-p open circuit. The composite main outputs are fed to the output rca jacks on the Video Out board via ribbon cable J16.

Zone2 Composite / S-video (Video board schematic sheet 3)

Zone2 functionality in the RV-8 corresponds to Record functionality in previous products, and the nomenclature reflects this legacy. In many places, the “record” nomenclature has been retained to correspond with the software base, but from the user perspective, this circuitry drives Zone2. Zone2 video circuitry is structured similarly to main video, but without OSD capability. Refer to the previous section for additional description. Multiplexers U10 and U11/U12 are addressed by the RECVID_SELn and RECSVID_SELn bits respectively to select an independent zone 2 (record) source, but otherwise operate like their counterparts in the main path. There is no dc-restorer in the zone2 path, so back-porch dc-level varies with average picture level due to input ac-coupling. The multiplexer internal to output amplifier U17 allows the zone2 S-video luminance to be shut off when a composite source is in use. Multiplexer U13 feeds the input dc voltage to the dc amplifier formed by Q2, Q3, and Q1, to transfer dc voltage on the chroma input to the chroma output for S-video switching purposes. The Zone2 composite output from U18 feeds two 75-ohm outputs, connecting to rca jacks on the Video Out board via ribbon cable J16.

Zone3 Composite video (Video board schematic sheet 4)

Zone3 is an additional video path in the RV-8 which provides one composite video output. Zone 3 video functionality corresponds to zone2 audio functionality in previous products and the signal-naming nomenclature reflects this legacy. Signals on the schematic refer to zone2, but this is zone 3 from the user perspective and rear-panel labeling. Multiplexers U9 and U7/U8 are addressed by the Z2VID_SELn and Z2SVID_SELn bits respectively to select an independent zone 3 source, but otherwise operate like their counterparts in the main path. There is no dc-restorer in the zone3 path, so back-porch dc-level varies with average picture level due to input ac-coupling. Refer to the composite video description in the previous sections for additional information. The zone3 composite output from U5 feeds the Zone 3 VIDEO rca jack on the Main Board via cable J20 (sheet 10).

Video Converter (Video board schematic sheet 5)

Composite or S-video inputs can be decoded and converted to component analog video output in the Y Pb Pr format by video codec U34. U34 combines the functionality of a video decoder and encoder (codec). U34 accepts the selected main composite or s-video source on two analog input pairs, AI1 and AI2. AI1 is taken after the input amplifiers but before the OSD, while AI2 is subject to the OSD. Within U34, the inputs are dc-restored and converted to digital form for decoding. The decoded digital video is passed via the PDn bus to the encoder portion of the codec to be re-encoded. The encoder incorporates 3 d-a converters for producing Y,Pb,Pr component analog video. The analog outputs from the encoder are filtered and buffered by U4 and U3 (sheet 6). The dc-level of the Y component is biased to place the back-porch around 0Vdc, and the dc-level of the Pb and Pr components is biased to place the 0 color-

difference level around 0Vdc. The converted input video is introduced into the component-video relay tree and is a selectable output just as any Y Pb Pr component input.

The encoder within U34 produces the complete video waveform for normal NTSC or PAL video inputs. However, during trick modes of VCR playback (pause, shuttle), the sync portion of the video is derived from a logic signal HVSYNC/. CPLD U14 detects trick modes based on anomalies in the decoded video sync timing. With normal video, the PLAYSPEED signal is asserted high. In trick modes, PLAYSPEED is not asserted, and system software in the host asserts SYNC_EN. U2, Q20, and associated circuitry switch U4 during sync time to construct a video waveform with sync derived from HVSYNC/.

There is time-base instability inherent with a VCR even in normal playback. To improve the stability of the converted video output, a phase-locked loop (U1, sheet 9) is used to reduce abrupt frequency shifts of the encoder clock ENC_27MHZ. A multiplexer within U14 determines whether ENC_27MHZ comes from the PLL or directly from XCLK, according to a multiplexer within U14. The preferred clock is dependent on the particular display device.

U34 is clocked at 24.576MHz by U33. Proper operation of the codec depends on the settings of an extensive set of internal registers of both the decoder and encoder. These registers are read and written via the I2C ports, connected to the host processor on the Main Board via J20 (sheet 10).

Component Video Switcher (Video board schematic sheet 3)

Component video switching is performed by means of relays to maximize signal fidelity and format compatibility. There is no active circuitry in the video path of external component sources.

Three sets of component input rca jacks (component inputs 1,2,3) feed a 3-wide, two-tier tree of double-throw relays. Each tier is comprised of a pair of dpdt relays. The tree selects one of the input sets and presents it to the bank of final output relays. The final tier of relays (RY3,RY1) connects the output RCA jacks either to the selected component input or to the video converter. One transistor driver is associated with each pair of relays. Relays are actuated when the associated PSELn bit is asserted high, switching from the normally-closed to the normally-open circuits.

Component OSD in the RV-8 is implemented through the video converter, which decodes the S-video OSD and produces the Y Pb Pr component OSD.

One normally-open pole of RY2 disconnects the luminance component CNV_Y in order to effectively disable component output.

The signals generated by the RV-8 OSD are compatible only with the 480i Y Pb Pr component format. When incompatible formats are in use, the component OSD is inapplicable, and is not accessed by the operating system software.

On-Screen Display Signals (Video board schematic sheet 5)

OSD chip U26 produces a character-based video display that can be overlaid on program video or that can occupy a full-screen, based on an independent internal video generator. OSD modes and parameters are controlled by an extensive set of internal registers, accessed via serial interface.

The character strings to be displayed are loaded serially into the screen memory within the chip. The bitmapped patterns that define the shapes of individual characters are stored in external font memory, interfaced through the A[15:0] and D[7:0] buses (see below). Character dot-clock is fixed at about 15 MHz, based on the external LC circuit formed by L7/C99/C100. A crystal clock is supplied by oscillator U37 (PAL) or U36 (NTSC). The active oscillator is determined by a high level on either NTSC_EN or PAL_EN, enabling the respective oscillator.

In overlay mode, composite or s-video luminance from the input amplifier is applied to YIN, and similarly, s-video chrominance (if applicable) is applied to CIN. The video applied to YIN is shifted to have a back-porch dc-level of about 1.57Vdc by U31 and associated circuitry. C123/C73 passively couple the ac-content of the luminance signal, with the op-amp providing the dc response. The chroma channel is biased to the same 1.57V level by R171/R172. The OSD video is related to program video by the separate H and V syncs (GMHSYN/, VSYNC/) derived by the sync stripper (sheet 8).

The full-screen mode is independent of video and sync inputs. Raster generation is based on the appropriate crystal clock.

The OSD luminance output is dc-shifted back to 0V back-porch level by U31 and associated circuitry. C121/C122 passively couple the ac-content, with the op-amp providing the dc response. Chroma is simply ac-coupled by C107/C108. The shifted OSD video is buffered and filtered by U30 to produce OSD_SY_OUT and OSD_C_OUT. Switch U40 permits the S-video luminance to be turned off when MSVID_YOFF is asserted high. OSD_Y+C_OUT is formed as half the sum of the buffer outputs. These OSD output signals feed the output amplifiers as described earlier.

In order to produce usable overlays in the SECAM system, the OSD switching action is bypassed at high frequency through U35 and R146, preserving an attenuated version of the fm color carriers.

On-Screen Display Serial Control (Video board schematic sheet 7)

The internal registers of the OSD are programmed serially from the main board in multiple 8-bit packets on VIDEO_DATA, accompanied by VIDEO_SCLK, operating at 1 MHz. During routine OSD updating, OSD_CS/ is level-shifted by U35, becoming OSD_CS5/, the OSD chip-select. The CPLD generates OSD_SCLKG from the VIDEO_SCLK, and U35 drives OSD_SCLK5 to clock the data into the OSD chip. Each logical transfer to the OSD chip consists of a pair of single-byte transfers.

Sync Stripper / DC Restorer (Video board schematic sheet 7)

Video from input amplifier U28 is fed through R204 to U41, which drives sync stripper U39 and the dc-restorer formed by switch U40 and op amp U41.

Sync stripper U39 accepts analog video and extracts vertical and horizontal sync, producing logic level VSYNC-OUT and AFC-OUT pulses respectively. A phase-locked loop based on ceramic resonator Y1 provides robust horizontal sync extraction even from noisy video sources. Pull-down resistors on the outputs improve the pulse waveshapes. Sections of U42 buffer and shape the pulses from U39. AFC-OUT is stretched by R244/C173 before buffering in order to meet the minimum width necessary for the OSD chip.

Sections of U42 and the network formed by R243,R242,D11 and C172 form pulses that are aligned with video back porch. These pulses switch U40, which in combination with integrator U41 forms a sample-and-hold circuit that closes the feedback loop around the input video amplifier during back-porch time. This acts to maintain the back-porch level at 0V. D10 limits the negative-going output of U41 in order to minimize the undesirable effects of unusual sync patterns inherent in the macrovision video copy-protection scheme.

Additional logic within U39 detects the presence of a valid video input. SYNC_DETECT is fed to the main board for use in OSD management.

The sync stripper U39 is susceptible to small variations on its power supply, and so it is specially-powered from a dedicated 5V regulator, U29.

With video input absent, AFC_OUT free-runs at around 15kHz.

Video Control Registers (Video board schematic sheet 8).

Control registers are implemented within CPLD U14, through a serial interface. The serial clock and data are VIDEO_SCLK and VIDEO_DATA, shared in common with the OSD. A transfer is initiated by a pulse on VIDEO_REG/, followed by a burst of clock and data that update all 56 control register bits within the CPLD in approximately 4.5 sec. All control bits are initialized to 0 at power-up by VIDEO_RST/.

Logic within the CPLD derives additional control bits from the values in the registers. For example, the MSVID_SELn bits are formed by gating the MVID_SELn bits with MCVID_EN/ such that the MSVID_SELn bits are forced to 0 when MCVID_EN/ is low.

The CPLD can be programmed in-circuit through the JTAG port J17.

Font Flash Programming Interface (Video board schematic sheet 9).

The CPLD U14 also controls the in-system programming of flash memory U25, which holds the bitmapped OSD font pattern. The CPLD is interfaced to the memory D[7:0] and A[15:0] buses.

In normal operation, this interface is tri-stated outputs and does not drive the buses, and the only bus activity is the fetching of font patterns from U25 over the A[15:0], D[7:0] buses under the control of OSD U26.

When necessary, the host processor on the main board manages the programming of the font flash memory. A large white box on the OSD is a symptom of an un-programmed memory. A control-register transfer with bit 47 set initiates a font flash write cycle, based on a state machine in the CPLD. The CPLD address and data buses are enabled, the OSD releases control of the bus (OSD_TSC/=high), and VROM_WR/ is asserted to write to the flash memory. The host performs a series of transfers with updated address and data to program subsequent bytes into the flash. During programming, the OSD continues to operate, but the write operations interfere with the normal bitmap fetching, which temporarily corrupts the OSD image. When the writing is complete, the corruption ceases, and the image is stable.

Power and Control Interface (Video board schematic sheet 10).

J20 is the control and status interface to the host. J18 supplies power from a connector on the main board. The main video +5-volt rail is +5VV, a filtered version of system +5VD, which also supplies relay coils through FB4. The negative rail is -5VV, derived from the main board -15VA by regulator U32. The video codec U34 and CPLD U14 are powered by 3.3V from regulator U24.

CHAPTER 7 – PARTS LIST

PART NO	DESCRIPTION	QTY	EFFECT.	INACT.	REFERENCE INFO.
Main Board Assembly					
022-14458	PL,MECH ASSY,VCO,MC12/B	2.00			J9,11
202-09794	RESSM,RO,0 OHM,0805	1.00			R82
202-09795	RESSM,RO,5%,1/10W,2.2K OHM	5.00			R6,8,10,12,25
202-09871	RESSM,RO,5%,1/10W,1K OHM	1.00			R26
202-09874	RESSM,RO,5%,1/10W,2.2M OHM	4.00			R47,49,96,98
202-09894	RESSM,RO,5%,1/10W,1M OHM	1.00			R145
202-09899	RESSM,RO,5%,1/10W,47 OHM	4.00			R43,92,120,147
202-10557	RESSM,RO,5%,1/10W,4.7K OHM	10.00			R21-24,129,131 R154-156,177
202-10558	RESSM,RO,5%,1/10W,47K OHM	8.00			R5,7,9,11,41,42 R90,91
202-10559	RESSM,RO,5%,1/10W,100 OHM	2.00			R37,86
202-10585	RESSM,RO,5%,1/4W,51 OHM	6.00			R178,182-186
202-10599	RESSM,RO,5%,1/10W,3K OHM	1.00			R119
202-10836	RESSM,RO,5%,1/4W,1K OHM	5.00			R13,14,17,18,176
202-10946	RESSM,RO,5%,1/10W,3.3K OHM	1.00			R109
202-10949	RESSM,RO,5%,1/10W,1.2K OHM	10.00			R40,45,46,89 R94,95,110-113
202-11040	RESSM,RO,5%,1/10W,150 OHM	7.00			R31-36,146
202-11041	RESSM,RO,5%,1/10W,680 OHM	12.00			R57-68
202-11071	RESSM,RO,5%,1/4W,75 OHM	4.00			R1-4
202-11496	RESSM,RO,0 OHM,1206	8.00			R121-127,188
202-12894	RESSM,RO,5%,1/10W,1.3M OHM	1.00			R165
202-12933	RESSM,RO,5%,1/4W,10 OHM	2.00			R76,142
202-14584	RESSM,RO,5%,1/10W,10K OHM,0603	17.00			R73-75,79-81,84,108 R114-116,132,140 R141,171,179,187
202-14585	RESSM,RO,0 OHM,0603	20.00			R53,55,70-72,100,102 R105,107,128,130 R137-139,148,150 R158-160,166
202-14792	RESSM,RO,5%,1/10W,56 OHM	5.00			R161-164,167
202-15681	RESSM,RO,5%,1/10W,47 OHM,0603	1.00			R152
203-10424	RESSM,RO,1%,1/10W,4.99K OHM	4.00			R38,39,87,88
203-10896	RESSM,RO,1%,1/10W,1.00K OHM	4.00			R15,19,77,143
203-11075	RESSM,RO,1%,1/10W,95.3 OHM	1.00			R30
203-11726	RESSM,RO,1%,1/10W,301 OHM	1.00			R29
203-11741	RESSM,RO,1%,1/10W,18.2K OHM	2.00			R48,97
203-11980	RESSM,THIN,1%,1/10W,10.0K OHM	2.00			R173,175
203-12471	RESSM,RO,1%,1/10W,442 OHM	2.00			R78,144
203-12491	RESSM,RO,1%,1/10W,205 OHM	1.00			R118
203-12722	RESSM,THIN,1%,1/10W,49.9K OHM	2.00			R44,93
203-12797	RESSM,RO,1%,1/10W,100 OHM	2.00			R172,174
203-12898	RESSM,RO,1%,1/10W,47.5K OHM	1.00			R99
203-12934	RESSM,RO,1%,1/10W,82.5 OHM	1.00			R50
203-13131	RESSM,RO,1%,1/10W,8.45K OHM	2.00			R16,20
205-14586	RESSM,NET,5%,ISOL,10KX4	11.00			RP1-8,11-13
205-15083	RESSM,NET,5%,ISOL,47X4	24.00			RP14-37
205-15737	RESSM,NET,5%,ISOL,3.3KX4	2.00			RP9,10
240-09786	CAP,ELEC,100uF,25V,RAD,LOW ESR	3.00			C169,173,176
240-10758	CAPSM,ELEC,1uF,50V,20%,5.5mmH	2.00			C42,84
240-12983	CAPSM,ELEC,100uF,10V,20%	2.00			C96,144
240-13217	CAPSM,ELEC,47uF,16V,20%	9.00			C22,24,41,45,53 C60,83,87,149
240-13913	CAPSM,ELEC,470uF,16V,20%	5.00			C17,78,139,177,178

PART NO	DESCRIPTION	QTY	EFFECT.	INACT.	REFERENCE INFO.
240-15668	CAPSM,ELEC,330uF,6.3V,20%,105C	4.00			C39,75,133,134
240-20028	CAP,ELEC,6800uF,6.3V,RAD,20%	2.00			C73,130
241-09798	CAPSM,TANT,10uF,10V,20%	3.00			C52,94,122
241-11799	CAPSM,TANT,4.7uF,6.3V,20%	4.00			C54,67,100,127
241-15206	CAPSM,TANT,33uF,10V,20%	2.00			C74,131
244-10423	CAP,MYL,.22uF,50V,RAD,5%,BOX	3.00			C168,172,175
245-09291	CAPSM,CER,470pF,50V,COG,5%	1.00			C118
245-09869	CAPSM,CER,.001uF,50V,Z5U,20%	14.00			C34,38,58,69,76,81 C97,106,132,137,146 C147,151,152
245-09876	CAPSM,CER,.01uF,50V,Z5U,20%	4.00			C2,4,6,8
245-10562	CAPSM,CER,150pF,50V,COG,10%	9.00			C10-15,167,171,174
245-10587	CAPSM,CER,18pF,50V,COG,10%	2.00			C140,141
245-10588	CAPSM,CER,33pF,50V,COG,10%	4.00			C1,3,5,7
245-10973	CAPSM,CER,22pF,50V,COG,5%	2.00			C159,160
245-10975	CAPSM,CER,3300pF,50V,X7R,10%	1.00			C98
245-10976	CAPSM,CER,47pF,50V,COG,5%	1.00			C19
245-11595	CAPSM,CER,.01uF,50V,COG,5%	2.00			C165,170
245-11645	CAPSM,CER,.47UF,50V,Z5U,20%	2.00			C23,25
245-12485	CAPSM,CER,.1uF,25V,Z5U,20%	72.00			C9,16,18,20,26-31,33 C35,37,40,43,44 C46-51,55,57,59,63 C64,66,68,72,80,82 C85,86,88-93,95,101 C104,105,109-117 C119-121,124,126,129 C136,142,143,145,150 C153,155-158,162 C163,166
245-12524	CAPSM,CER,68pF,50V,COG,5%	1.00			C21
245-14588	CAPSM,CER,.01uF,25V,X7R,10%,06	21.00			C32,36,56,61,62,65 C70,71,77,79,102,103 C107,108,125,128,135 C138,148,154,164
245-14764	CAPSM,CER,82pF,50V,COG,5%	1.00			C99
270-00779	FERRITE,BEAD	4.00			FB1,2,16,18
270-11545	FERRITESM,CHIP,600 OHM,0805	12.00			FB3-13,15
270-12323	FERRITESM,CHIP,750 OHM,0805	1.00			FB14
270-15670	INDUCTORSM,220uH,20%,1.2A	1.00			L2
300-10509	DIODESM,1N914,SOT23	4.00			D16,21,38,43
300-10563	DIODESM,DUAL,SERIES,GP,SOT23	6.00			D1-6
300-10564	DIODESM,SCHOTTKY,LOW VF,SOT23	8.00			D17-20,39-42
300-11599	DIODESM,GP,1N4002,MELF	6.00			D22,23,44,45,48,49
300-14286	DIODESM,SCHOTTKY,1A,SMB	3.00			D24,37,47
310-10566	TRANSISTORSM,2N4401,SOT23	1.00			Q1
310-15669	TRANSISTORSM,MOSFET,2A,55V,SOT	1.00			Q2
330-09889	ICSM,DIGITAL,74ACT04,SOIC	2.00			U17,28
330-10523	IC,HEX INVERTER,74HCU04,SOP	6.00			U3,4,10,23,35,47
330-12143	ICSM,DIGITAL,74ACT244,SSOP	1.00			U45
330-12451	ICSM,DIGITAL,74VHCT32,SOIC	1.00			U7
330-12452	ICSM,DIGITAL,74VHCT244,SOIC	1.00			U2
330-13865	ICSM,DIGITAL,74VHC04,SOIC	1.00			U14
330-13876	ICSM,DIGITAL,74VHC273,SOIC	2.00			U20,21
330-13882	ICSM,DIGITAL,74LCX14,SOIC	1.00			U46
330-14247	ICSM,DIGITAL,74VHCT245,SOIC	3.00			U36,37,43
330-15085	ICSM,DIGITAL,74ABT16244,TSSOP	1.00			U15
330-15735	ICSM,DIGITAL,74VHC139,SOIC	1.00			U13
340-09244	ICSM,LINEAR,78LS05,5V REG,SOIC	2.00			U18,29
340-11597	ICSM,LIN,TL072,DUAL OPAMP,SOIC	2.00			U11,24

PART NO	DESCRIPTION	QTY	EFFECT.	INACT.	REFERENCE INFO.
340-12119	ICSM,LIN,TL7705,+5V MON,SOIC	1.00			U31
340-13137	IC,LINEAR,LM2941CT,ADJ,TO-220	2.00			U8,9
340-13883	ICSM,LIN,LM2937,2.5V REG,TO263	1.00			U12
340-14535	IC,LIN,1585A,3.3V REG,TO220	1.00			U38
340-15088	ICSM,LIN,LM1117,ADJ,800mA,SOT	2.00			U22,39
345-13140	ICSM,INTER,RS232 XCVR,+5V,SOIC	1.00			U5
350-13879	ICSM,SDRAM,512KX32X4,3.3V,TSOP	2.00			U6,27
350-15096	ICSM,FPGA,XC2S200-6,28X42,PQFP	1.00			U41
350-15209	ICSM,DRAM,1MX16,60NS,SOJ	1.00			U42
350-15249	ICSM,GAL,16V8,RV8,V1.00	1.00			U44
350-15491	ICSM,FLASH,512KX8,3V,200NS,TSO	1.00			U19
350-16195	ICSM,FLASH,16M,RV8,MAIN,V1.03	1.00			U26
365-15490	ICSM,uPROC,DSP,CS49400,LQFP	1.00			U25
365-15660	ICSM,uPROC,ADSP21161,32BIT,BGA	2.00			U16,34
365-15661	ICSM,uPROC,SH7014,28.7MHz,QFP	1.00			U33
390-12076	CRYSTAL OSCSM,12.288MHz	1.00			U30
390-12458	CRYSTALSM,12.500MHz,PAR,HC49	1.00			Y2
390-13832	CRYSTALSM,14.112MHz,PAR,HC49	1.00			Y1
430-10419	LEDSM,INNER LENS,RED	6.00			D11,14,25,26,31,32
430-10420	LEDSM,INNER LENS,YEL	7.00			D12,15,27,28 D33,34,46
430-10421	LEDSM,INNER LENS,GRN	6.00			D10,13,29,30,35,36
510-10595	PHONE JACK,3.5MM,PCRA,3C,STER	1.00			J5
510-10745	CONN,POST,100X025,HDR,2MC,POL	4.00			J21,23,24,32
510-12319	CONN,D-SUB,9FCX2,STACKED,PCRA	1.00			J4
510-13146	CONN,HDR,.200,4MC,PCRA	1.00			TRIGGERS--J3
510-13147	CONN,RCA,PCRA,1FCG,YEL,GND	1.00			J7
510-13148	CONN,RCA,PCRA,1FCGX2V,BLK,GND	2.00			J1,2
510-13538	CONN,RCA,PCRA,1FCG,BLK,GND	1.00			J8
510-13840	CONN,OPTO,PCRA,TORX173,6Mbps	4.00			CP1-4
510-14079	CONN,POST,156X045,HDR,4MC,LOK	1.00			J31
510-14833	CONN,OPTO,PCRA,XMTR,13.2Mbps	1.00		12/13/04	CP5
510-15688	CONN,FFC,1.25MM,16 POS,VERT	1.00			VIDEO BD--J29
510-15689	CONN,FFC,1.25MM,34 POS,VERT	2.00			OPT BDS--J25,30
510-15690	CONN,FFC,1.25MM,40 POS,VERT	2.00			ANLG, FP BDS--J20,26
510-15694	CONN,FFC,1.25MM,6 POS,VERT	1.00			AMP PWR SUP--J27
510-15695	CONN,FFC,1.25MM,14 POS,VERT	2.00			PWR AMPS--J18,22
510-16389	CONN,OPTO,RA,XMT,13.2Mbps,SHTR	1.00	12/13/04		CP5
640-01701	SCRW,4-40X1/4,PNH,PH,ZN	2.00			U38; LUG 1
670-01974	WIRE,JMP,22AWG,0.1",NON-INSUL	1.00			W6
701-09640	BRACKET,KEYSTONE,621,4-40X2	1.00			LUG1
704-06165	HEATSINK,TO220,.75X.5X.5,TAB	2.00			U8,9
704-09508	HEATSINK,TO220,MTTAB,W/4-40NUT	1.00			U38
710-15550	PC BD,MAIN,RV8	1.00			PICK REV 5 PC BOARD
740-11287	LABEL,S/N,PCB,PRINTED	1.00			

VCO Masterclock Board Assembly

202-09899	RESSM,RO,5%,1/10W,47 OHM	1.00			R1
245-09895	CAPSM,CER,10pF,50V,COG,10%	1.00			C3
245-12485	CAPSM,CER,.1uF,25V,Z5U,20%	4.00			C1,2,4,5
270-11545	FERRITESM,CHIP,600 OHM,0805	1.00			FB1
270-14359	COILSM,VAR,1uH,5%,5.6X6.2X6MM	1.00			L1
300-13881	DIODESM,VARACTOR,BB132	1.00			D1
340-16132	ICSM,LIN,MC100EL1648,VCO,TSSOP	1.00			U1
510-14836	CONN,POST,100X025,HDR,5MC,RA	1.00			J1
710-16130	PC BD,VCO,MCLK	1.00			PICK REV 0 PC BOARD

PART NO	DESCRIPTION	QTY	EFFECT.	INACT.	REFERENCE INFO.
Microphone/Preamplifier Board Assembly					
202-09795	RESSM,RO,5%,1/10W,2.2K OHM	4.00			R1,3,4,6
202-09871	RESSM,RO,5%,1/10W,1K OHM	1.00			R15
202-10559	RESSM,RO,5%,1/10W,100 OHM	12.00			R19,20,23,24,33 R41-43,45,48,52,54
202-10586	RESSM,RO,5%,1/4W,100 OHM	2.00			R26,29
202-10598	RESSM,RO,5%,1/10W,330 OHM	2.00			R2,5
203-10578	RESSM,RO,1%,1/10W,2.21K OHM	4.00			R35,39,44,50
203-11077	RESSM,RO,1%,1/10W,237 OHM	1.00			R16
203-11723	RESSM,RO,1%,1/10W,4.75K OHM	2.00			R32,38
203-11980	RESSM,THIN,1%,1/10W,10.0K OHM	8.00			R7-14
203-12481	RESSM,RO,1%,1/10W,1.50K OHM	1.00			R25
203-12494	RESSM,RO,1%,1/10W,2.37K OHM	2.00			R49,55
203-12719	RESSM,THIN,1%,1/10W,2.00K OHM	2.00			R18,22
203-12723	RESSM,THIN,1%,1/10W,102 OHM	2.00			R17,21
203-12898	RESSM,RO,1%,1/10W,47.5K OHM	4.00			R27,28,31,37
203-13135	RESSM,THIN,1%,1/10W,432 OHM	2.00			R30,36
203-14566	RESSM,THIN,1%,1/10W,20.0K OHM	2.00			R46,51
240-09367	CAPSM,ELEC,10uF,25V,NONPOL,20%	4.00			C38,40,45,46
240-11111	CAPSM,ELEC,47uF,6V,NONPOL,20%	2.00			C31,32
240-11827	CAPSM,ELEC,10uF,16V,20%	7.00			C5-10,24
240-13216	CAPSM,ELEC,22uF,16V,20%	1.00			C18
241-09366	CAPSM,TANT,10uF,25V,20%	2.00			C26,28
244-11589	CAP,MYL,.068uF,63V,RAD,5%,BOX	4.00			C33,36,37,39
245-10562	CAPSM,CER,150pF,50V,COG,10%	6.00			C1-4,25,27
245-10974	CAPSM,CER,4.7pF,50V,COG,5%	2.00			C41,44
245-10976	CAPSM,CER,47pF,50V,COG,5%	6.00			C11,12,15,16,19,22
245-12485	CAPSM,CER,.1uF,25V,Z5U,20%	10.00			C13,14,17,20,21 C23,34,35,42,43
245-12522	CAPSM,CER,120pF,50V,COG,10%	2.00			C29,30
270-11545	FERRITESM,CHIP,600 OHM,0805	8.00			FB1-8
300-10563	DIODESM,DUAL,SERIES,GP,SOT23	8.00			D1-6,13,14
300-10564	DIODESM,SCHOTTKY,LOW VF,SOT23	4.00			D9-12
300-11599	DIODESM,GP,1N4002,MELF	2.00			D7,8
340-10552	ICSM,LIN,MC33078,DU OPAMP,SOIC	2.00			U1,2
340-11559	ICSM,LIN,LM317M,+ADJ REG,DPAK	1.00			U3
340-15699	ICSM,LIN,NE5532A,DUALOPAMP,SOI	2.00			U4,5
510-10595	PHONE JACK,3.5MM,PCRA,3C,STER	2.00			J1,2
510-10986	CONN,RCA,PCRA,1FCGX2V,RED/WH,G	1.00			J3
510-15688	CONN,FFC,1.25MM,16 POS,VERT	1.00			J4
640-02377	SCRW,4-40X1/4,PNH,PH,BLK	1.00			KEYSTONE BRKT
701-09640	BRACKET,KEYSTONE,621,4-40X2	1.00			LUG1
710-15520	PC BD,MIC/PREAMP,RV8	1.00			PICK REV 2 PC BOARD
740-11287	LABEL,S/N,PCB,PRINTED	1.00			
Tuner Board Assembly					
202-09794	RESSM,RO,0 OHM,0805	4.00			R1,3,5,6
202-10585	RESSM,RO,5%,1/4W,51 OHM	1.00			R16
203-10576	RESSM,RO,1%,1/10W,1.87K OHM	1.00			R12
203-10583	RESSM,RO,1%,1/10W,10.0K OHM	3.00			R13-15
203-11723	RESSM,RO,1%,1/10W,4.75K OHM	1.00			R11
203-11731	RESSM,RO,1%,1/10W,1.62K OHM	1.00			R10
203-12797	RESSM,RO,1%,1/10W,100 OHM	2.00			R8,9
240-09367	CAPSM,ELEC,10uF,25V,NONPOL,20%	2.00			C12,13
240-13217	CAPSM,ELEC,47uF,16V,20%	3.00			C18,20,21
241-15206	CAPSM,TANT,33uF,10V,20%	2.00			C16,17

PART NO	DESCRIPTION	QTY	EFFECT.	INACT.	REFERENCE INFO.
245-10562	CAPSM,CER,150pF,50V,COG,10%	2.00			C14,15
245-10588	CAPSM,CER,33pF,50V,COG,10%	1.00			C1
245-10976	CAPSM,CER,47pF,50V,COG,5%	2.00			C6,7
245-14588	CAPSM,CER,.01uF,25V,X7R,10%,06	2.00			C2,19
245-15691	CAPSM,CER,.001uF,25V,X7R,10%06	2.00			C9,11
245-15692	CAPSM,CER,.1uF,25V,X7R,10%,06	3.00			C3,8,10
245-15736	CAPSM,CER,.22uF,16V,X7R,10%	1.00			C5
270-00779	FERRITE,BEAD	1.00			FB1
270-15728	INDUCTORSM,6.8uH,10%	1.00			L1
340-15088	ICSM,LIN,LM1117,ADJ,800mA,SOT	2.00			U1,3
340-15659	ICSM,LIN,CRISP,TEF6892H,QFP44	1.00			U2
510-15729	CONN,FFC,1.25MM,13 POS,PCRA	1.00			J2
510-16141	CONN,MOD,RF,"F",W/SCRW TERM	1.00			J1
640-01701	SCRW,4-40X1/4,PNH,PH,ZN	1.00			LUG1
701-09640	BRACKET,KEYSTONE,621,4-40X2	1.00			LUG1
710-15540	PC BD,TUNER,RV8	1.00			PICK REV 1 PC BOARD
740-11287	LABEL,S/N,PCB,PRINTED	1.00			
750-15685	TUNER,AM/FM,1384,HORIZ PC MNT	1.00			U4
IR/Encoder Board Assembly					
202-00528	RES,CF,5%,1/4W,820 OHM	1.00			R1
202-00530	RES,CF,5%,1/4W,1.2K OHM	1.00			R2
202-00531	RES,CF,5%,1/4W,1.5K OHM	1.00			R3
245-03609	CAP,CER,.1uF,50V,Z5U,AX,80/20%	2.00			C1,2
345-14780	IC,INTER,GP1U28,38kHz,IR DET	1.00			U1B
430-10594	LED,T1-3/4,IR	1.00			D1
430-14487	LED,T1,BLU,430NM	1.00			SYSTEM ON--D4
430-14787	LED,T1,RED,700NM	1.00			OVERLOAD--D2
430-14788	LED,T1,YEL,585NM	1.00			IR ACK--D3
452-13640	SW,RTY,ENC,24POS,INC B,25L,VRT	1.00			SW1
630-14778	SPCR,LED,T1,.375"H	3.00			D2-4
680-14082	CABLE,100,PLUG/SCKT,2X7C,3"L	1.00			IR/ENC BD (J1) TO SW/LED BD
710-13690	PC BD,IR/ENC,MC12	1.00			PICK REV 2 PC BOARD
740-11287	LABEL,S/N,PCB,PRINTED	1.00			
Switch/LED Board Assembly					
202-09871	RESSM,RO,5%,1/10W,1K OHM	3.00			R11-13
202-09899	RESSM,RO,5%,1/10W,47 OHM	1.00			R31
202-10557	RESSM,RO,5%,1/10W,4.7K OHM	3.00			R32-34
202-10570	RESSM,RO,5%,1/10W,120 OHM	12.00			R1-9,28,43,50
202-10599	RESSM,RO,5%,1/10W,3K OHM	1.00			R30
202-11041	RESSM,RO,5%,1/10W,680 OHM	19.00			R10,14,16,18,20-27 R29,44-49
202-14584	RESSM,RO,5%,1/10W,10K OHM,0603	3.00			R15,17,19
202-14792	RESSM,RO,5%,1/10W,56 OHM	9.00			R35-42,51
205-14586	RESSM,NET,5%,ISOL,10KX4	4.00			RP1-4
240-09786	CAP,ELEC,100uF,25V,RAD,LOW ESR	1.00			C6
240-13217	CAPSM,ELEC,47uF,16V,20%	4.00			C1,13-15
245-12485	CAPSM,CER,.1uF,25V,Z5U,20%	7.00			C2-5,7,9,12
245-14588	CAPSM,CER,.01uF,25V,X7R,10%,06	3.00			C8,10,11
300-10509	DIODESM,1N914,SOT23	3.00			D1,20,31
310-10422	TRANSISTORSM,2N4403,SOT23	3.00			Q1-3
310-10510	TRANSISTORSM,2N3904,SOT23	1.00			Q4
330-15085	ICSM,DIGITAL,74ABT16244,TSSOP	1.00			U1
350-15517	ICSM,CPLD,RV8,FP,V1.00	1.00			U2
430-13639	LEDSM,BLU,30MCB,AX,ZBEND,2.5MM	16.00			D11,22-30,33 D35-38,40

PART NO	DESCRIPTION	QTY	EFFECT.	INACT.	REFERENCE INFO.
430-13888	LEDSM,RED,60MCD,AX,ZBEND,2.5MM	12.00			D2-10,21,32,39
430-14527	LEDSM,SYEL,250MCD,AX,ZBEND,2.5	9.00			D12-19,34
453-13899	SWSM,PBM,1P1T,6.2MMSQ,200GF	45.00			SW1-45
510-13145	CONN,POST,.100,HDR,2X7MCG,LP	2.00			J1,2
510-15690	CONN,FFC,1.25MM,40 POS,VERT	1.00			J5
710-15560	PC BD,SW/LED,RV8	1.00			PICK REV 1 PC BOARD
740-11287	LABEL,S/N,PCB,PRINTED	1.00			
Headhone Board Assembly					
245-10562	CAPSM,CER,150pF,50V,COG,10%	2.00			C1,2
270-00779	FERRITE,BEAD	3.00			FB1-3
510-11583	1/4"PH JACK,PCRA,3C,SW-TR,G,PT	1.00			J1
510-15696	CONN,FFC,1.25MM,4 POS,VERT	1.00			J2
710-15530	PC BD,HEADPHONE,RV8	1.00			PICK REV 2 PC BOARD
Analog Input/Output Board Assembly					
202-09872	RESSM,RO,5%,1/10W,33 OHM	4.00			R209,210,217,218
202-09873	RESSM,RO,5%,1/10W,10K OHM	8.00			R19,20,24,25,29,30 R107,109
202-09899	RESSM,RO,5%,1/10W,47 OHM	4.00			R345,349,353,357
202-10557	RESSM,RO,5%,1/10W,4.7K OHM	3.00			R121-123
202-10569	RESSM,RO,5%,1/10W,10 OHM	6.00			R114,260,263,267 R271,275
202-10570	RESSM,RO,5%,1/10W,120 OHM	11.00			R18,22,28,32,98,101 R111,301,404,415,417
202-10571	RESSM,RO,5%,1/10W,100K OHM	40.00			R50,51,54,55,58,59 R62,63,66,67,70,71 R74,75,78,79,113,117 R120,126,129,132,135 R238,240,244,246,250 R252,256,258,261,264 R268,272,276,390,406 R413,414
202-10585	RESSM,RO,5%,1/4W,51 OHM	18.00			R106,108,278,281,282 R285,286,289,290,293 R314,317,322,325,330 R333,338,341
202-10586	RESSM,RO,5%,1/4W,100 OHM	24.00			R1-16,33,36,37,40,41 R44,45,48
202-10943	RESSM,RO,5%,1/10W,22K OHM	8.00			R161,166,171,176 R181,186,191,196
202-10946	RESSM,RO,5%,1/10W,3.3K OHM	1.00			R83
202-10949	RESSM,RO,5%,1/10W,1.2K OHM	5.00			R81,82,410-412
202-11496	RESSM,RO,0 OHM,1206	4.00			R344,348,352,356
202-12191	RESSM,RO,5%,1/4W,330 OHM	6.00			R17,21,23,26,27,31
202-14585	RESSM,RO,0 OHM,0603	4.00			R342,346,350,354
202-14792	RESSM,RO,5%,1/10W,56 OHM	20.00			R49,52,53,56,57 R60,61,64,65 R68,69,72,73 R76,77,80,103,104 R200,201
203-10578	RESSM,RO,1%,1/10W,2.21K OHM	9.00			R204,205,297,299,392 R402,407,419,420
203-10583	RESSM,RO,1%,1/10W,10.0K OHM	9.00			R112,310,311,318,319 R326,327,334,335
203-10838	RESSM,RO,1%,1/10W,68.1 OHM	26.00			R162,163,167,168,172 R173,177,178,182,183 R187,188,192,193,197

PART NO	DESCRIPTION	QTY	EFFECT.	INACT.	REFERENCE INFO.
					R198,306-309,393-396
					R408,409
203-10896	RESSM,RO,1%,1/10W,1.00K OHM	24.00			R116,118,124,125,127
					R128,130,131,133,134
					R236,237,239,241-243
					R245,247,249,253-255
					R257,259
203-11078	RESSM,RO,1%,1/10W,422 OHM	9.00			R110,202,203,296,298
					R300,403,416,418
203-11697	RESSM,RO,1%,1/10W,909 OHM	2.00			R248,251
203-11726	RESSM,RO,1%,1/10W,301 OHM	2.00			R303,401
203-11734	RESSM,RO,1%,1/10W,4.32K OHM	8.00			R137,140,143,146,149
					R152,155,158
203-11993	RESSM,RO,1%,1/10W,357 OHM	1.00			R304
203-11995	RESSM,RO,1%,1/10W,2.55K OHM	2.00			R305,400
203-12371	RESSM,THIN,1%,1/10W,2.74K OHM	9.00			R206,207,294,295
					R397-399,421,422
203-12476	RESSM,RO,1%,1/10W,4.02K OHM	42.00			R84-91,115,119
					R358-389
203-12481	RESSM,RO,1%,1/10W,1.50K OHM	8.00			R138,141,144,147
					R150,153,156,159
203-12719	RESSM,THIN,1%,1/10W,2.00K OHM	16.00			R312,313,315,316
					R320,321,323,324
					R328,329,331,332
					R336,337,339,340
203-12723	RESSM,THIN,1%,1/10W,102 OHM	1.00			R302
203-12799	RESSM,RO,1%,1/10W,825 OHM	16.00			R34,35,38,39,42,43
					R46,47,92-97,99,100
203-12969	RESSM,THIN,1%,1/10W,316 OHM	20.00			R212-215,220-235
203-13133	RESSM,THIN,1%,1/10W,1.15K OHM	8.00			R164,169,174,179
					R184,189,194,199
203-13537	RESSM,THIN,1%,1/10W,5.62K OHM	8.00			R262,265,266,269
					R270,273,274,277
203-13638	RESSM,THIN,1%,1/10W,2.49K OHM	8.00			R279,280,283,284,287
					R288,291,292
203-15237	RESSM,THIN,1%,1/10W,681 OHM	4.00			R208,211,216,219
203-15479	RESSM,THIN,1%,1/10W,1.21K OHM	8.00			R160,165,170,175
					R180,185,190,195
203-15674	RESSM,RO,1%,1/10W,57.6K OHM	8.00			R136,139,142,145
					R148,151,154,157
240-09367	CAPSM,ELEC,10uF,25V,NONPOL,20%	20.00			C31,32,35,36,39,40
					C43,44,47,48,51,52
					C55,56,59,60,117
					C118,125,126
240-09786	CAP,ELEC,100uF,25V,RAD,LOW ESR	3.00			C449,452,455
240-11827	CAPSM,ELEC,10uF,16V,20%	7.00			C352,357,362,367
					C398,399,473
240-12136	CAPSM,ELEC,33uF,10V,20%	1.00			C459
240-13217	CAPSM,ELEC,47uF,16V,20%	8.00			C320,323,328,331
					C336,339,344,347
240-13642	CAP,ELEC,47uF,25V,RAD,NPOL,6D	18.00			C63-76,141,142
					C145,146
240-15668	CAPSM,ELEC,330uF,6.3V,20%,105C	22.00			C238,239,241,243-245
					C247,249-251,253
					C255-257,259,261,270
					C278,286,294,302,396
241-09798	CAPSM,TANT,10uF,10V,20%	2.00			C393,458
241-11799	CAPSM,TANT,4.7uF,6.3V,20%	52.00			C112,113,115,120,121

PART NO	DESCRIPTION	QTY	EFFECT.	INACT.	REFERENCE INFO.
					C123,273,275,277,281 C283,285,289,291,293 C297,299,301,305,307 C309,311,312,315,316 C319,322,324,327,330 C332,335,338,340,343 C346,403,405,407,410
245-10561	CAPSM,CER,100pF,50V,COG,5%	16.00			C415,417,419,422,427 C429,431,434,439,441 C446 C349,350,354,355 C359,360,363,365 C375,376,380,381 C385,386,390,391
245-10562	CAPSM,CER,150pF,50V,COG,10%	36.00			C1-30,448,450,451 C453,454,456
245-10587	CAPSM,CER,18pF,50V,COG,10%	12.00			C86,89,93,96,153,156 C157,160,161,164,165 C168
245-11594	CAPSM,CER,2200pF,50V,COG,5%	8.00			C400,401,412,413 C424,425,436,437
245-11598	CAPSM,CER,8200pF,50V,COG,5%	10.00			C229,236,240,242,246 C248,252,254,258,260
245-11949	CAPSM,CER,1500pF,50V,COG,5%	4.00			C230,231,234,235
245-12316	CAPSM,CER,.0082uF,50V,X7R,10%	7.00			C227,228,368,370 C470,471,475
245-12485	CAPSM,CER,.1uF,25V,Z5U,20%	238.00			C33,34,37,38,41,42 C45,46,49,50,53,54 C57,58,61,62,77-85 C87,88,90-92,94,95 C97-111,114,116,119 C122,124,127-140,143 C144,147-152,154,155 C158,159,162,163,166 C167,169-193,196,197 C202,203,208,209,214 C215,218-226,232,233 C237,262-269,271,272 C274,276,279,280,282 C284,287,288,290,292 C295,296,298,300,303 C304,306,308,310,313 C314,317,318,321,325 C326,329,333,334,337 C341,342,345,348,351 C353,356,358,361,364 C366,369,371-374 C377-379,382-384 C387-389,392,394,395 C397,402,404,406,408 C409,411,414,416,418 C420,421,423,426,428 C430,432,433,435,438 C440,442,444,445 C447,457,460-469 C472,474,476-480
245-13810	CAPSM,CER,1200pF,50V,COG,5%,08	16.00			C194,195,198-201 C204-207,210-213

PART NO	DESCRIPTION	QTY	EFFECT.	INACT.	REFERENCE INFO.
					C216,217
270-00779	FERRITE,BEAD	15.00			FB1-14,33
270-06671	FERRITE CHOKE,2.5 TURN	3.00			FB25-27
270-09799	FERRITESM,CHIP,600 OHM,1206	20.00			FB15-24,28-32,34-38
300-10563	DIODESM,DUAL,SERIES,GP,SOT23	26.00			D1-24,28,29
300-11599	DIODESM,GP,1N4002,MELF	10.00			D25-27,30-36
310-10566	TRANSISTORSM,2N4401,SOT23	3.00			Q1-3
330-13865	ICSM,DIGITAL,74VHC04,SOIC	1.00			U53
330-13882	ICSM,DIGITAL,74LCX14,SOIC	2.00			U76,91
330-14642	ICSM,DIGITAL,74VHCT14,SOIC	1.00			U96
330-15878	ICSM,DIGITAL,74LVC1G04,SC70	2.00			U94,95
340-01525	IC,LINEAR,7905,-5V REG	1.00			U73
340-10552	ICSM,LIN,MC33078,DU OPAMP,SOIC	25.00			U13,15,32-37,52 U54-57,68-71 U77-80,86-89
340-10877	ICSM,LIN,4556,DUAL OP AMP,SOIC	1.00			U30
340-11559	ICSM,LIN,LM317M,+ADJ REG,DPAK	3.00			U74,75,92
340-11597	ICSM,LIN,TL072,DUAL OPAMP,SOIC	13.00			U1-8,17,31,72,90,93
340-12062	ICSM,LIN,LM3940,5-3V REG,TO263	1.00			U85
340-15493	ICSM,LIN,PGA2311,VOL,5V,SOIC	7.00			U22,23,63-67
340-15699	ICSM,LIN,NE5532A,DUALOPAMP,SOI	4.00			U45-48
346-10549	ICSM,SS SWITCH,DG408,SOIC	6.00			U10-12,19-21
346-14451	ICSM,SS SW,DG411QUAD,1P1T,SOIC	13.00			U9,14,16,18,38U40-44,49-51
346-14583	ICSM,SS SW,ADG451QUAD,1P1T,SOI	6.00			U24-29
350-16126	ICSM,CPLD,RV8,ANALOG,V1.00	1.00			U39
355-14761	ICSM,DAC,AK4395,24BIT,VSOP	5.00			U58-62
355-15677	ICSM,ADC,PCM1804,24b,192kHz,SO	4.00			U81-84
410-11639	RELAY,2P2T,DIP,5V,HI SENS	8.00			RY1-8
510-03961	CONN,POST,100X025,HDR,2MCG	1.00			W1
510-13149	CONN,RCA,PCRA,1FCGX2V,WH/RED,G	15.00			J1-15
510-14079	CONN,POST,156X045,HDR,4MC,LOK	1.00			J19
510-15687	CONN,FFC,1.25MM,13 POS,VERT	1.00			J24
510-15688	CONN,FFC,1.25MM,16 POS,VERT	1.00			J23
510-15690	CONN,FFC,1.25MM,40 POS,VERT	1.00			J26
510-15694	CONN,FFC,1.25MM,6 POS,VERT	4.00			J17,18,21,27
510-15696	CONN,FFC,1.25MM,4 POS,VERT	1.00			J25
640-01701	SCRW,4-40X1/4,PNH,PH,ZN	1.00			U73
704-14452	HEATSINK,TO220,MTTAB,NUT,1.45H	1.00			U73
710-15570	PC BD,ANALOG I/O,RV8	1.00			PICK REV 4 PC BOARD
740-11287	LABEL,S/N,PCB,PRINTED	1.00			
3-Channel Amplifier Board Assembly					
201-16214	RES,TRM,1T,PC,1K OHM,SA,TOP	1.00			R168
201-16271	RES,TRM,1T,PC,1K OHM,SA,SIDE	2.00			R252,336
202-09794	RESSM,RO,0 OHM,0805	5.00			R74,77,126,169,173
202-16231	RESSM,RO,5%,1/4W,2.2M OHM	3.00			R131,215,299
202-16232	RES,CF,5%,1W,10 OHM,VERT	12.00			R140,141,143,145,224 R225,227,229,308,309 R311,313
202-16234	RES,MO,5%,2W,.68 OHM,VERT	24.00			R37,38,40,41,43,44 R110,111,194,195 R200-211,278,279
202-16255	RESSM,RO,5%,1W,30 OHM	6.00			R36,39,42,109 R193,277
203-11082	RESSM,RO,1%,1/10W,15.0K OHM	6.00			R87,90,171,174 R255,258
203-11732	RESSM,RO,1%,1/10W,1.82K OHM	3.00			R370,381,392
203-11980	RESSM,THIN,1%,1/10W,10.0K OHM	9.00			R137,162,163,221,246

PART NO	DESCRIPTION	QTY	EFFECT.	INACT.	REFERENCE INFO.
					R247,305,330,331
203-12722	RESSM,THIN,1%,1/10W,49.9K OHM	3.00			R138,222,306
203-13134	RESSM,THIN,1%,1/10W,1.00K OHM	9.00			R144,155,165,228,231 R249,312,315,333
203-13638	RESSM,THIN,1%,1/10W,2.49K OHM	15.00			R86,88,91,93,150 R170,172,175,177 R234,254,256,259 R261,318
203-14566	RESSM,THIN,1%,1/10W,20.0K OHM	9.00			R151,154,235,238,319 R322,372,383,394
203-14891	RESSM,THIN,1%,1/10W,9.09K OHM	6.00			R98,101,182,185 R266,269
203-16175	RESSM,RO,1%,1/4W,365K OHM	6.00			R239,240,242,245 R253,257
203-16235	RESSM,THIN,1%,1/10W,100 OHM	9.00			R118,119,121,147,159 R212,213,243,327
203-16236	RESSM,THIN,1%,1/10W,100K OHM	21.00			R136,152,153,157,160 R220,236,237,241,244 R304,320,321,325,328 R368,369,379,380 R390,391
203-16237	RESSM,THIN,1%,1/10W,12.1K OHM	3.00			R373,384,395
203-16239	RESSM,THIN,1%,1/10W,1.82K OHM	9.00			R107,167,191,251,275 R335,367,378,389
203-16241	RESSM,THIN,1%,1/10W,23.2K OHM	12.00			R365,366,371,376,377 R382,387,388,393 R405-407
203-16243	RESSM,THIN,1%,1/10W,280K OHM	3.00			R130,214,298
203-16244	RESSM,THIN,1%,1/10W,33.2K OHM	9.00			R132,135,146,216,219 R230,300,303,314
203-16245	RESSM,THIN,1%,1/10W,47.5 OHM	3.00			R96,180,264
203-16249	RESSM,THIN,1%,1/10W,750.0 OHM	9.00			R97,108,139,181,192 R223,265,276,307
203-16250	RESSM,THIN,1%,1/10W,75.0 OHM	3.00			R106,190,274
203-16251	RESSM,THIN,1%,1/10W,95.3 OHM	12.00			R104,105,114,115,188 R189,198,199,272,273 R282,283
203-16252	RESSM,THIN,1%,1/10W,5.11K OHM	12.00			R133,134,148,149,217 R218,232,233,301,302 R316,317
203-16253	RESSM,THIN,1%,1/4W,4.99K OHM	9.00			R95,164,166,179,248 R250,263,332,334
203-16254	RES,MF,1%,1W,49.9K OHM,VERT	6.00			R94,102,178,186 R262,270
203-16256	RESSM,RO,1%,1/4W,107 OHM	3.00			R142,226,310
203-16415	RESSM,THIN,1%,1/10W,825.0 OHM	12.00			R99,100,103,113,183 R184,187,197,267 R268,271,281
240-16257	CAP,ELEC,2.2uF,160V,RAD,20%	6.00			C58,61,97,100,136 C139
240-16260	CAPSM,ELEC,2.2uF,50V,20%	2.00			C82,121
240-16261	CAPSM,ELEC,10uF,50V,20%	3.00			C64,103,142
240-16262	CAPSM,ELEC,4.7uF,16V,NPOL,20%	6.00			C161,162,165,166 C169,170
240-16263	CAPSM,ELEC,33uF,16V,NPOL,20%	3.00			C41,80,119
244-16265	CAP,MYL,.0047uF,250V,RAD,5%	3.00			C68,107,146
244-16266	CAP,MYL,.01uF,250V,RAD,5%	6.00			C65,67,104,106 C143,145

PART NO	DESCRIPTION	QTY	EFFECT.	INACT.	REFERENCE INFO.
244-16267	CAP,MYL,.33uF,63V,RAD,10%	3.00			C66,105,144
245-10416	CAPSM,CER,1000pF,50V,COG,5%	6.00			C179-184
245-10544	CAPSM,CER,220pF,50V,COG,5%	12.00			C51,52,55,56,90,91 C94,95,129,130 C133,134
245-10561	CAPSM,CER,100pF,50V,COG,5%	6.00			C163,164,167,168 C171,172
245-10973	CAPSM,CER,22pF,50V,COG,5%	6.00			C40,42,79,81,118,120
245-16269	CAPSM,CER,22pF,200V,COG,5%	15.00			C44,47-50,83,86-89 C122,125-128
245-16270	CAPSM,CER,100pF,200V,COG,5%	6.00			C53,57,92,96,131,135
245-16293	CAPSM,CER,.1uF,50V,X7R,10%	37.00			C4,43,45,46,63,71-78 C84,85,102,110-117 C123,124,141,149-156 C327,328
245-16295	CAPSM,CER,4700pF,50V,COG,5%	1.00			C148
245-16296	CAPSM,CER,27pF,50V,COG,10%	3.00			C69,108,147
245-16297	CAPSM,CER,47pF,50V,COG,10%	3.00			C54,93,132
245-16411	CAPSM,CER,.01uF,100V,X7R,5%	6.00			C59,60,98,99,137,138
245-16412	CAPSM,CER,.47uF,50V,Z5U,5%	3.00			C62,101,140
270-16272	COIL,1.5uH,5%,RAD,.375LS	3.00			L2-4
300-10509	DIODESM,1N914,SOT23	48.00			D16,24-27,29-32 D34-36,39-41,47-50 D52-55,57,62-64 D70-73,75-78,80-82 D85-87,97,99-104
300-16200	DIODESM,ZENER,5.1V,225mW,SOT23	6.00			D43,44,66,67,89,90
300-16201	DIODESM,ZENER,17V,225mW,SOT23	6.00			D42,65,88,93-95
300-16202	DIODESM,ZENER,16V,500mW,SOD12	36.00			D45,46,68,69,91,92
300-16203	DIODESM,RECT,400V,50A,50NS,SMB	6.00			D37,38,60,61,83,84
300-16205	DIODESM,SW,250V,625mA,MELF	6.00			D28,33,51,56,74,79
310-10510	TRANSISTORSM,2N3904,SOT23	9.00			Q27,35,46,54,65,73 Q84,88,92
310-10565	TRANSISTORSM,2N3906,SOT23	6.00			Q34,53,72,83,87,91
310-16206	TRANSISTORSM,NPN,25V,225mW,SOT	3.00			Q81,85,89
310-16207	TRANSISTORSM,NPN,300V,1W,SOT	3.00			Q22,41,60
310-16208	TRANSISTORSM,PNP,50V,350mW,SOT	3.00			Q82,86,90
310-16209	TRANSISTORSM,PNP,300V,1W,SOT	3.00			Q23,42,61
310-16210	TRANSISTOR,NPN,300V,1W,TO92	9.00			Q28,29,37,47,48,56 Q66,67,75
310-16211	TRANSISTOR,PNP,300V,1W,TO92	9.00			Q24,25,38,43,44,57 Q62,63,76
310-16274	TRANSISTOR,MJE15032,NPN,TO220	3.00			Q26,45,64
310-16275	TRANSISTOR,MJE15033,PNP,TO220	3.00			Q12-14
330-15667	ICSM,DIGITAL,74HCT594,SOIC	1.00			U30
330-16215	ICSM,DIGITAL,74HCT597,SOIC	1.00			U50
340-10552	ICSM,LIN,MC33078,DU OPAMP,SOIC	3.00			U5,9,13
340-11045	ICSM,LIN,LM393,DUAL COMP,SOIC	3.00			U7,11,15
340-11948	ICSM,LIN,LM339,QUAD COMP,SOIC	3.00			U8,12,16
340-16219	ICSM,LIN,TLE2037,OPAMP,SOIC	3.00			U6,10,14
410-16222	RELAY,1P2T,24V,SEALED	3.00			K2-4
430-16223	LEDSM,GRN,10MCD,1206	3.00			E2-4
440-15874	FUSE,5X20MM,SLO-BLO,12.5A,250V	2.00			F1,2
480-16225	THERMISTORSM,NTC,20K OHM,0805	3.00			RT2-4
510-15694	CONN,FFC,1.25MM,6 POS,VERT	2.00			P1,2
510-15695	CONN,FFC,1.25MM,14 POS,VERT	1.00			J1
510-16278	CONN,.163,HDR,2X3MC,SHR,POL,LK	1.00			J6
510-16279	CONNSM,TEST POINT,1206	6.00			TP3-8
525-16229	TERM,SCRW,PC,SNAP,VERT,6-32	6.00			P5-10

PART NO	DESCRIPTION	QTY	EFFECT.	INACT.	REFERENCE INFO.
600-16416	FUSE CLIP,5X20MM,PC,.217"LS	4.00			HW4-7
600-16419	BUS BAR,CU,3CH,RV8	1.00			W1
680-16417	WIRE,16G,#6RINGX2/PC,80/150MM	1.00			W7
680-16418	WIRE,16G,#6RINGX2/PC,170/150MM	1.00			W8
710-16150	PC BD,AMP MOD,3CH,RV8	1.00			PICK REV 2 PC BOARD
740-11287	LABEL,S/N,PCB,PRINTED	1.00			PLACE NEXT TO TP8
4-Channel Amplifier Board Assembly					
201-16214	RES,TRM,1T,PC,1K OHM,SA,TOP	1.00			R168
201-16271	RES,TRM,1T,PC,1K OHM,SA,SIDE	3.00			R84,252,336
202-09794	RESSM,RO,0 OHM,0805	6.00			R72,74,77,126 R249,251
202-16231	RESSM,RO,5%,1/4W,2.2M OHM	4.00			R47,131,215,299
202-16232	RES,CF,5%,1W,10 OHM,VERT	16.00			R56,57,59,61,140,141 R143,145,224,225,227 R229,308,309,311,313
202-16234	RES,MO,5%,2W,.68 OHM,VERT	32.00			R26,27,34,35,37,38 R40,41,43,44,110,111 R169,173,176,194-196 R200-211,278,279
202-16255	RESSM,RO,5%,1W,30 OHM	8.00			R25,33,36,39,42,109 R193,277
203-11082	RESSM,RO,1%,1/10W,15.0K OHM	8.00			R3,6,87,90,171,174 R255,258
203-11732	RESSM,RO,1%,1/10W,1.82K OHM	4.00			R359,370,381,392
203-11980	RESSM,THIN,1%,1/10W,10.0K OHM	12.00			R53,78,79,137,162 R163,221,246,247 R305,330,331
203-12722	RESSM,THIN,1%,1/10W,49.9K OHM	4.00			R54,138,222,306
203-13134	RESSM,THIN,1%,1/10W,1.00K OHM	11.00			R8,32,81,144,155,165 R228,231,312,315,333
203-13638	RESSM,THIN,1%,1/10W,2.49K OHM	20.00			R2,4,7,9,66,86,88 R91,93,150,170,172 R175,177,234,254 R256,259,261,318
203-14566	RESSM,THIN,1%,1/10W,20.0K OHM	12.00			R67,70,151,154,235 R238,319,322,361,372 R383,394
203-14891	RESSM,THIN,1%,1/10W,9.09K OHM	8.00			R14,17,98,101,182 R185,266,269
203-16175	RESSM,RO,1%,1/4W,365K OHM	8.00			R129,161,239,240 R242,245,253,257
203-16235	RESSM,THIN,1%,1/10W,100 OHM	12.00			R75,112,116,118,119 R121,147,159,212 R213,243,327
203-16236	RESSM,THIN,1%,1/10W,100K OHM	28.00			R52,68,69,73,76,136 R152,153,157,160,220 R236,237,241,244,304 R320,321,325,328,345 R358,368,369,379,380 R390,391
203-16237	RESSM,THIN,1%,1/10W,12.1K OHM	4.00			R362,373,384,395
203-16239	RESSM,THIN,1%,1/10W,1.82K OHM	11.00			R23,83,107,167,191 R275,335,344,367 R378,389
203-16241	RESSM,THIN,1%,1/10W,23.2K OHM	16.00			R342,343,360,365,366 R371,376,377,382,387 R388,393,404-407

PART NO	DESCRIPTION	QTY	EFFECT.	INACT.	REFERENCE INFO.
203-16243	RESSM,THIN,1%,1/10W,280K OHM	4.00			R46,130,214,298
203-16244	RESSM,THIN,1%,1/10W,33.2K OHM	12.00			R48,51,62,132,135 R146,216,219,230,300 R303,314
203-16245	RESSM,THIN,1%,1/10W,47.5 OHM	4.00			R12,96,180,264
203-16249	RESSM,THIN,1%,1/10W,750.0 OHM	12.00			R13,24,55,97,108,139 R181,192,223,265,276 R307
203-16250	RESSM,THIN,1%,1/10W,75.0 OHM	4.00			R22,106,190,274
203-16251	RESSM,THIN,1%,1/10W,95.3 OHM	16.00			R20,21,30,31,104,105 R114,115,188,189,198 R199,272,273,282,283
203-16252	RESSM,THIN,1%,1/10W,5.11K OHM	16.00			R49,50,64,65,133,134 R148,149,217,218,232 R233,301,302,316,317
203-16253	RESSM,THIN,1%,1/4W,4.99K OHM	12.00			R11,80,82,95,164 R166,179,248,250 R263,332,334
203-16254	RES,MF,1%,1W,49.9K OHM,VERT	8.00			R10,18,94,102,178 R186,262,270
203-16256	RESSM,RO,1%,1/4W,107 OHM	4.00			R58,142,226,310
203-16415	RESSM,THIN,1%,1/10W,825.0 OHM	16.00			R15,16,19,29,99,100 R103,113,183,184,187 R197,267,268,271,281
240-16257	CAP,ELEC,2.2uF,160V,RAD,20%	8.00			C19,22,58,61,97,100 C136,139
240-16260	CAPSM,ELEC,2.2uF,50V,20%	2.00			C82,121
240-16261	CAPSM,ELEC,10uF,50V,20%	4.00			C25,64,103,142
240-16262	CAPSM,ELEC,4.7uF,16V,NPOL,20%	8.00			C157,158,161,162 C165,166,169,170
240-16263	CAPSM,ELEC,33uF,16V,NPOL,20%	4.00			C2,41,80,119
244-16265	CAP,MYL,.0047uF,250V,RAD,5%	4.00			C29,68,107,146
244-16266	CAP,MYL,.01uF,250V,RAD,5%	8.00			C26,28,65,67,104 C106,143,145
244-16267	CAP,MYL,.33uF,63V,RAD,10%	4.00			C27,66,105,144
245-10416	CAPSM,CER,1000pF,50V,COG,5%	8.00			C177-184
245-10544	CAPSM,CER,220pF,50V,COG,5%	16.00			C12,13,16,17,51,52 C55,56,90,91,94,95 C129,130,133,134
245-10561	CAPSM,CER,100pF,50V,COG,5%	8.00			C159,160,163,164 C167,168,171,172
245-10973	CAPSM,CER,22pF,50V,COG,5%	8.00			C1,3,40,42,79,81 C118,120
245-16269	CAPSM,CER,22pF,200V,COG,5%	20.00			C5,8-11,44,47-50,83 C86-89,122,125-128
245-16270	CAPSM,CER,100pF,200V,COG,5%	8.00			C14,18,53,57,92,96 C131,135
245-16293	CAPSM,CER,.1uF,50V,X7R,10%	48.00			C4,6,7,24,32-39,43 C45,46,63,71-78,84 C85,102,110-117,123 C124,141,149-156 C327,328
245-16295	CAPSM,CER,4700pF,50V,COG,5%	1.00			C148
245-16296	CAPSM,CER,27pF,50V,COG,10%	4.00			C30,69,108,147
245-16297	CAPSM,CER,47pF,50V,COG,10%	4.00			C15,54,93,132
245-16411	CAPSM,CER,.01uF,100V,X7R,5%	8.00			C20,21,59,60,98,99 C137,138
245-16412	CAPSM,CER,.47uF,50V,Z5U,5%	4.00			C23,62,101,140
270-16272	COIL,1.5uH,5%,RAD,.375LS	4.00			L1-4

PART NO	DESCRIPTION	QTY	EFFECT.	INACT.	REFERENCE INFO.
300-10509	DIODESM,1N914,SOT23	64.00			D1-4,6-9,11-13,16-18 D24-27,29-32,34-36 D39-41,47-50,52-55 D57-59,62-64,70-73 D75-78,80-82,85-87 D97,98-104
300-16200	DIODESM,ZENER,5.1V,225mW,SOT23	8.00			D20,21,43,44,66,67 D89,90
300-16201	DIODESM,ZENER,17V,225mW,SOT23	8.00			D19,42,65,88,93-96
300-16202	DIODESM,ZENER,16V,500mW,SOD123	8.00			D22,23,45,46,68,69 D91,92
300-16203	DIODESM,RECT,400V,50A,50NS,SMB	8.00			D14,15,37,38,60,61 D83,84
300-16205	DIODESM,SW,250V,625mA,MELF	8.00			D5,10,28,33,51,56 D74,79
310-10510	TRANSISTORSM,2N3904,SOT23	12.00			Q8,16,27,35,46,54,65 Q73,80,84,88,92
310-10565	TRANSISTORSM,2N3906,SOT23	8.00			Q15,34,53,72,79,83 Q87,91
310-16206	TRANSISTORSM,NPN,25V,225mW,SOT	4.00			Q77,81,85,89
310-16207	TRANSISTORSM,NPN,300V,1W,SOT	4.00			Q3,22,41,60
310-16208	TRANSISTORSM,PNP,50V,350mW,SOT	4.00			Q78,82,86,90
310-16209	TRANSISTORSM,PNP,300V,1W,SOT	4.00			Q4,23,42,61
310-16210	TRANSISTOR,NPN,300V,1W,TO92	12.00			Q9,10,18,28,29,37,47 Q48,56,66,67,75
310-16211	TRANSISTOR,PNP,300V,1W,TO92	12.00			Q5,6,19,24,25,38,43 Q44,57,62,63,76
310-16274	TRANSISTOR,MJE15032,NPN,TO220	4.00			Q7,26,45,64
310-16275	TRANSISTOR,MJE15033,PNP,TO220	4.00			Q11-14
330-15667	ICSM,DIGITAL,74HCT594,SOIC	1.00			U30
330-16215	ICSM,DIGITAL,74HCT597,SOIC	1.00			U50
340-10552	ICSM,LIN,MC33078,DU OPAMP,SOIC	4.00			U1,5,9,13
340-11045	ICSM,LIN,LM393,DUAL COMP,SOIC	4.00			U3,7,11,15
340-11948	ICSM,LIN,LM339,QUAD COMP,SOIC	4.00			U4,8,12,16
340-16219	ICSM,LIN,TLE2037,OPAMP,SOIC	4.00			U2,6,10,14
410-16222	RELAY,1P2T,24V,SEALED	4.00			K1-4
430-16223	LEDSM,GRN,10MCD,1206	4.00			E1-4
440-15874	FUSE,5X20MM,SLO-BLO,12.5A,250V	2.00			F1,2
480-16225	THERMISTORSM,NTC,20K OHM,0805	4.00			RT1-4
510-15694	CONN,FFC,1.25MM,6 POS,VERT	2.00			P1,2
510-15695	CONN,FFC,1.25MM,14 POS,VERT	1.00			J1
510-16278	CONN,.163,HDR,2X3MC,SHR,POL,LK	1.00			J6
510-16279	CONNSM,TEST POINT,1206	8.00			TP1-8
525-16229	TERM,SCRW,PC,SNAP,VERT,6-32	8.00			P3-10
600-16416	FUSE CLIP,5X20MM,PC,.217"LS	4.00			HW4-7
600-16420	BUS BAR,CU,4CH,RV8	1.00			W1
680-16417	WIRE,16G,#6RINGX2/PC,80/150MM	1.00			W7
680-16418	WIRE,16G,#6RINGX2/PC,170/150MM	1.00			W8
710-16160	PC BD,AMP MOD,4CH,RV8	1.00			PICK REV 2 PC BOARD
740-11287	LABEL,S/N,PCB,PRINTED	1.00			PLACE NEXT TO TP8
Speaker EMI Filter Board Assembly					
245-16182	CAPSM,CER,470pF,100V,X7R,10%	2.00			C1,2
710-16180	PC BD,SPKR EMI FILTER,RV8	1.00			PICK REV 0 PC BOARD

PART NO	DESCRIPTION	QTY	EFFECT.	INACT.	REFERENCE INFO.
Video Board Assembly					
202-09795	RESSM,RO,5%,1/10W,2.2K OHM	1.00			R77
202-09871	RESSM,RO,5%,1/10W,1K OHM	13.00			R4,11,17,85,88,108 R111-113,139,239 R241,244
202-09873	RESSM,RO,5%,1/10W,10K OHM	13.00			R84,107,136,146,170 R214,225,230,231,243 R247,249,250
202-09874	RESSM,RO,5%,1/10W,2.2M OHM	1.00			R240
202-09894	RESSM,RO,5%,1/10W,1M OHM	2.00			R75,232
202-09899	RESSM,RO,5%,1/10W,47 OHM	4.00			R79,80,224,226
202-10426	RESSM,RO,5%,1/10W,15K OHM	18.00			R20-28,114,117 R141,144,153,154 R194,197,216
202-10557	RESSM,RO,5%,1/10W,4.7K OHM	4.00			R81-83,147
202-10558	RESSM,RO,5%,1/10W,47K OHM	1.00			R78
202-10571	RESSM,RO,5%,1/10W,100K OHM	9.00			R134,135,167,168,173 R193,203,206,248
202-10573	RESSM,RO,5%,1/10W,470K OHM	11.00			R37,47,56,65,74 R191,219-223
202-10943	RESSM,RO,5%,1/10W,22K OHM	3.00			R246,254,255
202-10945	RESSM,RO,5%,1/10W,1.5K OHM	1.00			R251
202-10946	RESSM,RO,5%,1/10W,3.3K OHM	15.00			R30,35,40,45,49,54 R58,63,67,73,87 R110,138,227,238
202-10947	RESSM,RO,5%,1/10W,680K OHM	1.00			R245
202-10948	RESSM,RO,5%,1/10W,390 OHM	1.00			R252
202-10949	RESSM,RO,5%,1/10W,1.2K OHM	1.00			R76
202-11042	RESSM,RO,5%,1/10W,6.8K OHM	4.00			R119,121,148,150
202-12369	RESSM,RO,5%,1/10W,36K OHM	6.00			R131,133,166,169 R202,207
202-13579	RESSM,RO,5%,1/10W,22 OHM	10.00			R31,36,41,46,50 R55,59,64,68,72
202-16144	RESSM,RO,5%,1/10W,12 OHM	1.00			R228
203-10560	RESSM,RO,1%,1/10W,75.0 OHM	32.00			R29,32,39,42,48,51 R57,60,66,69,89,92 R94,95,97,100,101 R104,106,115,116,118 R120,142,145,149,151 R152,155,195,198,218
203-10579	RESSM,RO,1%,1/10W,2.49K OHM	2.00			R91,98
203-10837	RESSM,RO,1%,1/10W,475 OHM	6.00			R156,196,199,204 R209,242
203-10840	RESSM,RO,1%,1/10W,750 OHM	23.00			R38,93,96,105 R122-125,130,132,157 R158,161-165,177,180 R200,201,205,208
203-10895	RESSM,RO,1%,1/10W,681 OHM	2.00			R174,182
203-10896	RESSM,RO,1%,1/10W,1.00K OHM	4.00			R1,9,15,229
203-11080	RESSM,RO,1%,1/10W,1.15K OHM	12.00			R126-129,159,160,176 R178,179,183,211,212
203-11697	RESSM,RO,1%,1/10W,909 OHM	1.00			R102
203-11705	RESSM,RO,1%,1/10W,11.0K OHM	6.00			R2,6,8,13,14,19
203-11723	RESSM,RO,1%,1/10W,4.75K OHM	8.00			R5,10,16,171,184 R187,190,192
203-11726	RESSM,RO,1%,1/10W,301 OHM	2.00			R215,217
203-11734	RESSM,RO,1%,1/10W,4.32K OHM	1.00			R103

PART NO	DESCRIPTION	QTY	EFFECT.	INACT.	REFERENCE INFO.
203-11740	RESSM,RO,1%,1/10W,9.09K OHM	4.00			R3,7,12,18
203-11743	RESSM,RO,1%,1/10W,100K OHM	5.00			R34,44,53,62,71
203-11889	RESSM,RO,1%,1/10W,110 OHM	4.00			R233-236
203-12198	RESSM,RO,1%,1/10W,2.15K OHM	5.00			R172,185,186,188,189
203-12298	RESSM,RO,1%,1/10W,30.1K OHM	1.00			R253
203-12491	RESSM,RO,1%,1/10W,205 OHM	4.00			R140,143,210,213
203-12497	RESSM,RO,1%,1/10W,8.25K OHM	4.00			R86,109,137,237
203-12841	RESSM,RO,1%,1/10W,39.2K OHM	5.00			R33,43,52,61,70
203-12897	RESSM,RO,1%,1/10W,976 OHM	2.00			R175,181
203-16145	RESSM,RO,1%,1/10W,1.07K OHM	2.00			R90,99
205-15737	RESSM,NET,5%,ISOL,3.3KX4	1.00			RP1
240-09786	CAP,ELEC,100uF,25V,RAD,LOW ESR	3.00			C138-140
240-10758	CAPSM,ELEC,1uF,50V,20%,5.5mmH	2.00			C56,179
240-11111	CAPSM,ELEC,47uF,6V,NONPOL,20%	10.00			C11,15,17,21,25 C130-134
240-11827	CAPSM,ELEC,10uF,16V,20%	5.00			C106,107,122,129,183
240-13217	CAPSM,ELEC,47uF,16V,20%	4.00			C47,54,73,79
241-09798	CAPSM,TANT,10uF,10V,20%	3.00			C97,137,163
245-09876	CAPSM,CER,.01uF,50V,Z5U,20%	1.00			C120
245-09895	CAPSM,CER,10pF,50V,COG,10%	1.00			C99
245-10416	CAPSM,CER,1000pF,50V,COG,5%	3.00			C127,177,178
245-10452	CAPSM,CER,390pF,50V,COG,5%	3.00			C32,33,39
245-10544	CAPSM,CER,220pF,50V,COG,5%	2.00			C172,176
245-10561	CAPSM,CER,100pF,50V,COG,5%	3.00			C64,169,174
245-10972	CAPSM,CER,.068uF,50V,X7R,20%	1.00			C180
245-10975	CAPSM,CER,3300pF,50V,X7R,10%	1.00			C181
245-10976	CAPSM,CER,47pF,50V,COG,5%	1.00			C117
245-10977	CAPSM,CER,330pF,50V,COG,5%	1.00			C173
245-11591	CAPSM,CER,560pF,50V,COG,5%	3.00			C27,29,34
245-11625	CAPSM,CER,33pF,50V,COG,5%	1.00			C109
245-12070	CAPSM,CER,15pF,50V,COG,10%	1.00			C100
245-12460	CAPSM,CER,.056uF,50V,X7R,20%	6.00			C151-156
245-12485	CAPSM,CER,.1uF,25V,Z5U,20%	119.00			C1-10,12-14,16,18-20 C22-24,28,31,35-37 C40-46,48-53,55 C57-63,65-72,74-78 C80-96,98,101-105 C108,112,116,118,119 C121,123-126,128,135 C136,141-150,157-162 C164,165,167,168,170 C171,175,182
245-12522	CAPSM,CER,120pF,50V,COG,10%	3.00			C26,30,38
245-12524	CAPSM,CER,68pF,50V,COG,5%	1.00			C115
245-14762	CAPSM,CER,6.8pF,50V,COG,5%	1.00			C110
245-14763	CAPSM,CER,12pF,50V,COG,5%	2.00			C113,166
245-14764	CAPSM,CER,82pF,50V,COG,5%	1.00			C114
270-00779	FERRITE,BEAD	4.00			FB4-7
270-11289	INDUCTORSM,10uH,10%	1.00			L7
270-11545	FERRITESM,CHIP,600 OHM,0805	7.00			FB1-3,8-11
270-15693	INDUCTORSM,2.7uH,10%	6.00			L1-6
300-10509	DIODESM,1N914,SOT23	2.00			D1,11
300-10563	DIODESM,DUAL,SERIES,GP,SOT23	1.00			D10
300-11599	DIODESM,GP,1N4002,MELF	8.00			D2-9
310-10510	TRANSISTORSM,2N3904,SOT23	16.00			Q2,3,5,6,8-19
310-10565	TRANSISTORSM,2N3906,SOT23	7.00			Q1,4,7,20,24-26
310-10566	TRANSISTORSM,2N4401,SOT23	3.00			Q21-23
330-10417	ICSM,DIGITAL,74HC00,SOIC	1.00			U2

PART NO	DESCRIPTION	QTY	EFFECT.	INACT.	REFERENCE INFO.
330-10505	ICSM,DIGITAL,74HC02,SOIC	1.00			U42
330-12321	ICSM,DIGITAL,74VHCT08,TSSOP	1.00			U35
340-01525	IC,LINEAR,7905,-5V REG	1.00			U32
340-09244	ICSM,LINEAR,78LS05,5V REG,SOIC	1.00			U29
340-10502	ICSM,LIN,LF353,DUAL OPAMP,SOIC	2.00			U31,41
340-11495	ICSM,LIN,LT1229,VID OPAMP,SOIC	3.00			U18,28,30
340-13445	ICSM,LIN,TLC2933,PLL,TSOP	1.00			U1
340-14535	IC,LIN,1585A,3.3V REG,TO220	1.00			U24
340-15586	ICSM,LIN,MAX4310,VIDAMP,W/MUX	5.00			U4,15-17,38
340-15683	ICSM,LIN,AD8072,VIDAMPX2,SOIC	5.00			U3,5,6,19,27
345-10503	ICSM,INTER,NJM2229,SYNSEP,SOIC	1.00			U39
346-10507	ISCM,SS SWITCH,74HC4051,SOIC	11.00			U7-13,20-23
346-10508	ICSM,SS SWITCH,74HC4053,SOIC	1.00			U40
350-15672	ICSM,FLASH,128KX8,5V,90NS,PLCC	1.00			U25
350-16147	ICSM,CPLD,RV8,VIDEO,V1.00	1.00			U14
355-15678	ICSM,CODEC,SAA7109E,VIDEO,BGA	1.00			U34
365-13288	ICSM,uPROC,MB90092,OSDC,PQFP	1.00			U26
390-10516	RESONATOR,CER,503KHz	1.00			Y1
390-13857	CRYSTAL,OSCSM,14.31818MHz,TRI	1.00			U36
390-13858	CRYSTAL,OSCSM,17.73448MHz,TRI	1.00			U37
390-14544	CRYSTAL OSCSM,24.576MHz,TRI,3V	1.00			U33
410-11639	RELAY,2P2T,DIP,5V,HI SENS	6.00			RY1-6
510-13128	CONN,MINIDIN,4FC,PCRA,GND	9.00			J1-4,11-15
510-14079	CONN,POST,156X045,HDR,4MC,LOK	1.00			J18
510-15471	CONN,RCA,PCRA,1FCGX2V,GRN,GND	2.00			J7,10
510-15472	CONN,RCA,PCRA,1FCGX2V,RED,GND	2.00			J5,8
510-15473	CONN,RCA,PCRA,1FCGX2V,BLU,GND	2.00			J6,9
510-15688	CONN,FFC,1.25MM,16 POS,VERT	1.00			J20
640-01701	SCRW,4-40X1/4,PNH,PH,ZN	1.00			U32
704-06165	HEATSINK,TO220,.75X.5X.5,TAB	1.00			U24
704-09508	HEATSINK,TO220,MTTAB,W/4-40NUT	1.00			U32
710-15580	PC BD,VIDEO,RV8	1.00			PICK REV 4 PC BOARD
740-11287	LABEL,S/N,PCB,PRINTED	1.00			
Video In Board Assembly					
202-10946	RESSM,RO,5%,1/10W,3.3K OHM	5.00			R1,4,7,10,13
202-13579	RESSM,RO,5%,1/10W,22 OHM	5.00			R2,5,8,11,14
203-10560	RESSM,RO,1%,1/10W,75.0 OHM	5.00			R3,6,9,12,15
240-11827	CAPSM,ELEC,10uF,16V,20%	2.00			C11,12
245-12485	CAPSM,CER,.1uF,25V,Z5U,20%	10.00			C1-10
310-10510	TRANSISTORSM,2N3904,SOT23	5.00			Q1-5
510-13147	CONN,RCA,PCRA,1FCG,YEL,GND	5.00			J1-5
680-15684	CABLE,FFC,14CX.1,CRMPST/RA,2.5	1.00			J6
710-15500	PC BD,VIDEO IN,RV8	1.00			PICK REV 0 PC BOARD
740-11287	LABEL,S/N,PCB,PRINTED	1.00			
Video Out Board Assembly					
510-13147	CONN,RCA,PCRA,1FCG,YEL,GND	4.00			J1-4
680-16146	CABLE,FFC,14CX.1,CRMPST/RA,1.5	1.00			J5
710-15510	PC BD,VIDEO OUT,RV8	1.00			PICK REV 0 PC BOARD
Power Supply Board Subssembly					
022-16443	PL,ASSY,BRIDGE RECT,RV8	1.00			D26
202-09794	RESSM,RO,0 OHM,0805	1.00			R238
202-16233	RES,CF,5%,2W,27K OHM,VERT	10.00			R2-11
203-11980	RESSM,THIN,1%,1/10W,10.0K OHM	8.00			R207,210,215,218,220 R223-225
203-13134	RESSM,THIN,1%,1/10W,1.00K OHM	3.00			R221,227,228

PART NO	DESCRIPTION	QTY	EFFECT.	INACT.	REFERENCE INFO.
203-14566	RESSM,THIN,1%,1/10W,20.0K OHM	4.00			R211,213,214,216
203-16235	RESSM,THIN,1%,1/10W,100 OHM	2.00			R222,226
203-16238	RESSM,THIN,1%,1/10W,14.7K OHM	1.00			R212
203-16246	RESSM,THIN,1%,1/10W,6.19K OHM	2.00			R217,219
203-16247	RESSM,THIN,1%,1/10W,61.9K OHM	2.00			R208,209
240-16258	CAP,ELEC,5600uF,35V,SNAP,20%	2.00			C81,82
240-16259	CAP,ELEC,27000uF,80V,SNAP,20%	4.00			C40,77,78,79
240-16264	CAPSM,ELEC,10uF,50V,NPOL,20%	1.00			C70
244-16268	CAP,MYL,.1uF,250V,X2,RAD,20%	1.00			C80
245-16292	CAPSM,CER,.01uF,50V,X7R,10%	2.00			C65,66
245-16293	CAPSM,CER,.1uF,50V,X7R,10%	6.00			C67-69,71,75,83
245-16410	CAPSM,CER,.33uF,50V,X7R,5%	2.00			C74,76
300-10509	DIODESM,1N914,SOT23	4.00			D22-25
300-16204	DIODESM,RECT,100V,3A,20NS,SMC	4.00			D27-30
310-10566	TRANSISTORSM,2N4401,SOT23	3.00			Q23-25
340-11045	ICSM,LIN,LM393,DUAL COMP,SOIC	1.00			U42
340-16216	ICSM,LIN,7815,+15V REG,D2PAK	1.00			U1
340-16217	ICSM,LIN,7915,-15V REG,D2PAK	1.00			U2
340-16218	ICSM,LIN,LM324,4OPAMP,SOIC	1.00			U41
410-16220	RELAY,1PNO,5V,SEALED	1.00			K3
410-16221	RELAY,1PNO,24V,SEALED	1.00			K2
480-16224	THERMISTOR,PTC,6 OHM,265V	2.00			RT1,2
510-15694	CONN,FFC,1.25MM,6 POS,VERT	1.00			P1
510-16227	CONN,.163,HDR,2MC,SHR,POL,LK	1.00			J21
510-16228	CONN,.250,HDR,2X3MCG,SHR,POL	3.00			J4,14,15
510-16278	CONN,.163,HDR,2X3MC,SHR,POL,L	2.00			J2,5
525-16281	TERM,QDC,.250,PC,.2LS,LK	1.00			J12
525-16282	TERM,QDC,.250,PCRA,.2LS	2.00			J6,7
600-16230	FUSE CLIP,3AG/5X20MM,PC	2.00			HW1,2
710-16170	PC BD,PS,RV8	1.00			PICK REV 2 PC BOARD
740-11287	LABEL,S/N,PCB,PRINTED	1.00			PLACE OVER HW4
Chassis Assembly					
022-15610	PL,MECH ASSY,FP,RV8	1.00			
022-15611	PL,MECH ASSY,VIDEO,RV8	1.00			
022-15612	PL,MECH ASSY,TUNER/PREAMP,RV8	1.00			
022-15624	PL,FAN ASSY,RV8	4.00			CONNECT TO MAIN BD (J21,23,24,32)
022-16444	PL,MECH ASSY,AMP,3CH,RV8	1.00			
022-16445	PL,MECH ASSY,AMP,4CH,RV8	1.00			
023-15615	PL,MAIN BD ASSY,RV8	1.00			
023-15617	PL,ANLG I/O BD ASSY,RV8	1.00			
270-16120	FERRITE,FLAT CABLE,~1.8X1.1"	1.00			TUNER CABLE
454-13124	SW,ROCKER,2P1T,16A@250,BLK,VER	1.00			
470-15213	XFORMER,PWR,TOR,RV8/CX AMP	1.00			For 100-120V: WIRE TO "100V/120V" CONN ON PS BD For 220-240V: WIRE TO "220V/230V/240V" CONN ON PS BD
490-13144	CONN,PLUG,.200,4FC,RA,12-30G	1.00			REAR PANEL
490-15843	CONN,AC,3MC,SNAP,06TH,IEC,10A	1.00			
527-12974	CONN,DSUB,JSCKT,4-40,.187X.25	4.00			DCONN TO R.PANEL
530-02488	TIE,CABLE,NYL,.14"X5-5/8"	8.00			CABLES TO CHASSIS
540-14303	GROMMET,STRIP,SER,.037"GAP,NYL	15.50			(2) 7.75" PCS
541-15576	FOOT,50MM DX25MM H,ABS,BLK	4.00			CHASSIS
550-15844	HANDLE,"U",5X2H,3/8"D,BLK	2.00			
630-12533	WSHR,FL,.120IDX.25ODX.062,RUB	16.00			FANS TO CHASSIS

PART NO	DESCRIPTION	QTY	EFFECT.	INACT.	REFERENCE INFO.
635-15322	SPCR,M3X8MM,RD,HEXHD,BLIND,ZN	16.00			FANS TO CHASSIS
640-01711	SCRW,6-32X1/4,FH,PH,ZN	4.00			PS TO PS MTG PLATE
640-01721	SCRW,8-32X3/8,PNH,PH,ZN	4.00			HANDLES TO R.PANEL
640-02377	SCRW,4-40X1/4,PNH,PH,BLK	1.00			MAIN BD TO R.PANEL
640-10498	SCRW,M3X6MM,PNH,PH,BZ	6.00			CTR PLT TO CHAS L&R
640-10498	SCRW,M3X6MM,PNH,PH,BZ	2.00			OPT PNL TO REAR PNL
640-10498	SCRW,M3X6MM,PNH,PH,BZ	4.00			MAIN BD TO CTR PLATE
640-10498	SCRW,M3X6MM,PNH,PH,BZ	5.00			ANLG BD TO CTR PLATE
640-10498	SCRW,M3X6MM,PNH,PH,BZ	4.00			VIDEO DBs TO R.PNL
640-10498	SCRW,M3X6MM,PNH,PH,BZ	2.00			TUNER ASSY TO R.PNL
640-10498	SCRW,M3X6MM,PNH,PH,BZ	2.00			BTM PLATE TO FP
640-11284	SCRW,M3X8MM,FH,PH,BZ	16.00			FANS TO CHASSIS
640-13645	SCRW,M4X10MM,FH,SCKT,BZ	13.00			COVER TO CHASSIS
640-15346	SCRW,M5X16MM,PNH,PH,ZN	4.00			FEET TO CHASSIS
640-15476	SCRW,M4X8MM,PNH,PH,ZN	4.00			XFRMR TO BRKT
640-15476	SCRW,M4X8MM,PNH,PH,ZN	6.00			PS & TORROID ASSY TO CHASSIS
640-15476	SCRW,M4X8MM,PNH,PH,ZN	6.00			3CH AMP TO CHASSIS AND R. PANEL
640-15476	SCRW,M4X8MM,PNH,PH,ZN	2.00			PS MTG PLATE TO CHAS
640-15476	SCRW,M4X8MM,PNH,PH,ZN	8.00			4CH AMP TO CHASSIS AND R.PANEL
640-15476	SCRW,M4X8MM,PNH,PH,ZN	4.00			F.PANEL TO CHASSIS
640-16140	SCRW,4-40X5/16,THMB,RH,SS	1.00			TUNER/PREAMP TO RP
641-01703	SCRW,TAP,AB,4X1/4,PNH,PH,ZN	8.00			ACCESS PLATE TO CHAS
641-11466	SCRW,TAP,#4X3/8,PNH,PH,BZ,TRI	20.00			RCA CONN TO R.PNL; ALIGN HOLES W/CONNS BEFORE TORQUING SCREWS.
643-10492	NUT,M4X.7MM,KEP,ZN	1.00			CHASSIS GND
644-01741	WSHR,INT STAR,#8,ZN	4.00			REAR HANDLES
644-01747	WSHR,INT STAR,#4,ZN	4.00			DSUB JSCKT
644-10494	WSHR,FL,M4CLX9ODX.8MM THK	1.00			CHASSIS GND
680-15630	WIRE,14G,G/Y,3.5"187QDCRA/LUG8	1.00			AC IN TO CHASSIS GND
680-15631	CABLE,FFC,4CX1.25MM,15"L,COS	1.00			HEADPHONE TO ANLG BD
680-15632	CABLE,FFC,13CX1.25MM,15"L,COS	1.00			TUNER TO ANLG BD
680-15633	CABLE,FFC,16CX1.25MM,10"L,COS	1.00			VIDEO BD TO MAIN BD
680-15634	CABLE,FFC,16CX1.25MM,14"L,COS	1.00			PHONO PREAMP TO ANLG
680-15636	CABLE,FFC,40CX1.25MM,6"L,COS	1.00			ANLG BD TO MAIN BD
680-15637	CABLE,FFC,40CX1.25MM,12"L,COS	1.00			FP TO MAIN BD
680-15639	CABLE,FFC,14CX1.25MM,4"L,COS	1.00			4CH AMP TO MAIN BD
680-15640	CABLE,FFC,6CX1.25MM,4"L,COS	3.00			AMPS TO ANLG BD (2); CROWN PS TO MN BD(1)
680-15641	CABLE,FFC,6CX1.25MM,6"L,COS	1.00			3CH AMP TO ANLG BD
680-15641	CABLE,FFC,6CX1.25MM,6"L,COS	1.00			4CH AMP TO ANLG BD
680-15642	CABLE,HSGX2,10C/4CX3,16.5"	1.00			PS TO MAIN, ANLG & VIDEO BDs
680-15643	CABLE,HSG/QDC,18/14AWG,22.5"	1.00			PWR SW TO PWR SUP
680-15697	CABLE,PWR,187RA/250QDC,SLV,7.5	1.00			AC CONN TO PWR SW
680-15698	CABLE,HSG/HSG,16G,6C,12"	2.00			3&4CH AMPS TO PS
680-16122	CABLE,FFC,14CX1.25MM,4"L,FOLD	1.00			3CH AMP TO MAIN BD
700-15809	COVER,4U,RV8	1.00			
700-15810	CHASSIS,LEFT,RV8	1.00			
700-15811	CHASSIS,RIGHT,RV8	1.00			
700-15812	PLATE,CENTER,CHASSIS,RV8	1.00			
702-15803	PANEL,REAR,RV8	1.00			

PART NO	DESCRIPTION	QTY	EFFECT.	INACT.	REFERENCE INFO.
702-15806	PLATE,BOTTOM,RV8	1.00			CHASSIS BOTTOM
702-15807	PLATE,MTG,PS,RV8	1.00			
702-15808	PANEL,OPTION,BLANK,RV8	1.00			REAR PANEL
720-15425	PAD,FOOT,1.438OD,.563IDX.06THK	4.00			
720-16123	TAPE,FOAM,DBL-STK,1.75X.4X.025	1.00			FERRITE TO TUNER CBL
740-08556	LABEL,GROUND SYMBOL,0.5"DIA	1.00			
740-09538	LABEL,S/N,CHASSIS,PRINTED	1.00			REAR PANEL
740-14888	LABEL,LIC/PAT/WARN,MC12	1.00			CHASSIS BOTTOM
740-16015	LABEL,100-120V,50-60Hz,1300W	1.00			For 100-120V: REAR PANEL, ABOVE AC CONN
740-16017	LABEL,220-240V,50-60Hz,1300W	1.00			For 220-240V: REAR PANEL, ABOVE AC CONN
750-15827	PWR SUP,+5V/+-15V,65W,"U" BRKT	1.00			
750-15828	REMOTE CONTROL,RV8	1.00			
FP Mechanical Assembly					
023-14068	PL,IR/ENC BD ASSY,MC12/B	1.00			
023-15616	PL,SW/LED BD ASSY,RV8	1.00			
023-15622	PL,HEADPHONE BD ASSY,RV8	1.00			
430-13143	DISPLAY,VF,20X2 CHAR,5X8DOT	1.00			
550-13633	BUTTON,.276X.572,BLK	16.00			
550-13634	BUTTON,.276X.572,BLK,W/LTPIPE	29.00			
550-14090	KNOB,2.00X.95H,6MM,ALUM,PEWTER	1.00			ENCODER
635-14526	SPCR,M3CLX6MM,6MMRD	1.00			IR/ENC BD
640-01841	SCRW,2-56X1/4,PNH,PH,ZN	4.00			DISPLAY TO FP
640-10495	SCRW,M3X12MM,PNH,PH,ZN	1.00			IR/ENC BD
640-10498	SCRW,M3X6MM,PNH,PH,BZ	10.00			SHIELD TO FP
640-10498	SCRW,M3X6MM,PNH,PH,BZ	11.00			SW/LED BD TO FP
640-10498	SCRW,M3X6MM,PNH,PH,BZ	2.00			HEADPHONE BRKT
640-15476	SCRW,M4X8MM,PNH,PH,ZN	6.00			SPT BRKTS TO FP
680-14693	CABLE,100,PLUG/SCKT,2X7C,10.5"	1.00			SOLDER TO DSPLY. DSPLY TO SW/LED BD.
701-14858	SHIELD,6.7X1.8X.4"H	1.00			
701-15454	BRACKET,SUPPORT,COVER,MC8	1.00			
701-15816	BRACKET,HEADPHONE BD,RV8	1.00			
701-15847	BRACKET,"L",SUPPORT,COVER,RV8	2.00			FP TO COVER
702-15800	PANEL,FRONT,RV8	1.00			
703-14098	LENS,6.36X1.55,MC12	1.00			
720-15849	LIGHT PIPE,LED,VERT,.13D	7.00			
Video Mechanical Assembly					
023-15618	PL,VIDEO BD ASSY,RV8	1.00			
023-15619	PL,VIDEO IN BD ASSY,RV8	1.00			
023-15620	PL,VIDEO OUT BD ASSY,RV8	1.00			
640-10498	SCRW,M3X6MM,PNH,PH,BZ	4.00			VIDEO BD TO BRKT
641-13116	SCRW,TAP,AB,4X3/8,FH,PH,BZ	15.00			VIDEO BD TO BRKT
701-15815	BRACKET,VIDEO BD,RV8	1.00			
Tuner/Preamp Mechanical Assembly					
023-15621	PL,MIC/PREAMP BD ASSY,RV8	1.00			
023-15627	PL,TUNER BD ASSY,RV8	1.00			
635-15337	SPCR,M3X25MM,6MM HEX	1.00			TUNER BD TO BRKT
640-02715	SCRW,4-40X1/4,FH,PH,ZN	1.00			TUNER BD KEYSTONE TO BRKT
640-10498	SCRW,M3X6MM,PNH,PH,BZ	1.00			SPCR TO BRKT
640-10498	SCRW,M3X6MM,PNH,PH,BZ	2.00			MIC/PREAMP TO BRKT
640-10498	SCRW,M3X6MM,PNH,PH,BZ	1.00			TUNER BD TO SPCR

PART NO	DESCRIPTION	QTY	EFFECT.	INACT.	REFERENCE INFO.
641-13116	SCRW,TAP,AB,4X3/8,FH,PH,BZ	1.00			RCA CONN TO BRKT
641-13116	SCRW,TAP,AB,4X3/8,FH,PH,BZ	2.00			TUNER BD TO BRKT
701-15814	BRACKET,TUNER,RV8	1.00			
Fan Assembly					
410-15839	FAN,60X60X10MM,12VDC,10CFM	1.00			
525-12536	CONN,CONT,CRIMP,22-26AWG,AMP	2.00			
527-12537	CONN,HSG,CRIMP,.100X2,POL,LK	1.00			
Power Supply Mechanical Assembly					
023-15826	PL,PS BD SUBASSY,RV8	1.00			
440-16212	FUSE,5X20MM,SLO-BLO,6.3A,250V	1.00			(For 220-240V) HW1-2
440-16213	FUSE,3AG,FAST,15A,250V	1.00			(For 120V) HW1-2
635-16285	SPCR,6-32X1.25,.25HEX,ALUM	2.00			
640-16291	SCRW,6-32X.25,PNH,TORX,SEMS,BZ	2.00			
641-16299	SCRW,TAP,6-32X.25,PNH,TX,SMS,Z	4.00			
701-16426	BRACKET,TOROID/PS,RV8	1.00			
Bridge Rectifier Assembly					
300-16273	DIODE,RECT,200V,50A,W/HS	1.00			
635-16286	SPCR,8-32X.5,.375HEX,ALUM	1.00			
640-16287	SCRW,8-32X.75,PNH,TORX,SEMS,BZ	1.00			
704-16433	HEATSINK,BRIDGE RECT,RV8	1.00			
VCO Mechanical Assembly					
023-16129	PL,VCO BD ASSY,MCLK	1.00			
700-14838	HOUSING,VCO,MC12	1.00			
700-14839	COVER,VCO,MC12	1.00			
3-Channel Amp Bd Mechanical Assembly					
022-16446	PL,HS ASSY,SGL,POS,RV8	1.00			
022-16447	PL,HS ASSY,SGL,NEG,RV8	1.00			
022-16448	PL,HS ASSY,DBL,POS,RV8	1.00			
022-16449	PL,HS ASSY,DBL,NEG,RV8	1.00			
023-15824	PL,AMP BD ASSY,3CH,RV8	1.00			
023-15890	PL,SPKR EMI FILTER BD ASSY,RV8	3.00			
490-16280	CONN,BDGPOSTX2G,10-32,RED/BLK	3.00			
630-16283	WSHR,SHLDR,.312SHNK,#6CL,NYL	4.00			
630-16284	SPCR,#6CLX.090,.25RD,NYL	4.00			
640-01710	SCRW,6-32X1/4,PNH,PH,ZN	6.00			P5-10
640-16298	SCRW,6-32X.25,UFH,PH,ZN	2.00			
641-16288	SCRW,TAP,6-32X.312,PNH,TORX,ZN	20.00			
643-16290	NUT,6-32,KEP,CONICAL WSHR,ZN	4.00			
644-03668	WSHR,LOCK,EXT STAR,#6,SS	4.00			
680-16422	HARNESS,AMP,3CH,RV8	1.00			
701-16424	BRACKET,AMP,3CH,RV8	1.00			
702-16427	PLATE,AMP,3CH,RV8	1.00			
703-16429	INSUL,AMP,3CH,RV8	1.00			
4-Channel Amp Bd Mechanical Assembly					
022-16448	PL,HS ASSY,DBL,POS,RV8	2.00			
022-16449	PL,HS ASSY,DBL,NEG,RV8	2.00			
023-15825	PL,AMP BD ASSY,4CH,RV8	1.00			
023-15890	PL,SPKR EMI FILTER BD ASSY,RV8	4.00			

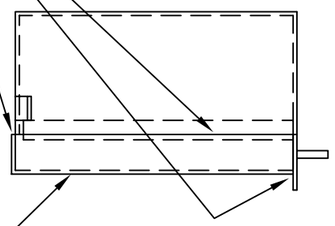
PART NO	DESCRIPTION	QTY	EFFECT.	INACT.	REFERENCE INFO.
490-16280	CONN,BDGPOSTX2G,10-32,RED/BLK	4.00			
630-16283	WSHR,SHLDR,.312SHNK,#6CL,NYL	4.00			
630-16284	SPCR,#6CLX.090,.25RD,NYL	4.00			
640-01710	SCRW,6-32X1/4,PNH,PH,ZN	8.00			P3-10
640-16298	SCRW,6-32X.25,UFH,PH,ZN	2.00			
641-16288	SCRW,TAP,6-32X.312,PNH,TORX,ZN	24.00			
643-16290	NUT,6-32,KEP,CONICAL WSHR,ZN	4.00			
644-03668	WSHR,LOCK,EXT STAR,#6,SS	4.00			
680-16423	HARNESS,AMP,4CH,RV8	1.00			
701-16425	BRACKET,AMP,4CH,RV8	1.00			
702-16428	PLATE,AMP,4CH,RV8	1.00			
703-16430	INSUL,AMP,4CH,RV8	1.00			
Single Positive Heatsink Assembly					
100-01759	CHEM,HEATSINK COMP,SILICONE	0.003 oz			
310-16276	TRANSISTOR,MJ21194,NPN,TO3	2.00			
630-16421	INSUL,SIL RUB,.94X.66	1.00			
641-16289	SCRW,TAP,6-32X.25,PNH,TORX,ZN	4.00			
704-16431	HEATSINK,AMP,SGL,RV8	1.00			
Single Negative Heatsink Assembly					
100-01759	CHEM,HEATSINK COMP,SILICONE	0.003 oz			
310-16277	TRANSISTOR,MJ21193,PNP,TO3	2.00			
630-16421	INSUL,SIL RUB,.94X.66	1.00			
641-16289	SCRW,TAP,6-32X.25,PNH,TORX,ZN	4.00			
704-16431	HEATSINK,AMP,SGL,RV8	1.00			
Double Positive Heatsink Assembly					
100-01759	CHEM,HEATSINK COMP,SILICONE	0.003 oz			
310-16276	TRANSISTOR,MJ21194,NPN,TO3	4.00			
630-16421	INSUL,SIL RUB,.94X.66	2.00			
641-16289	SCRW,TAP,6-32X.25,PNH,TORX,ZN	8.00			
704-16432	HEATSINK,AMP,DBL,RV8	1.00			
Double Negative Heatsink Assembly					
100-01759	CHEM,HEATSINK COMP,SILICONE	0.003 oz			
310-16277	TRANSISTOR,MJ21193,PNP,TO3	4.00			
630-16421	INSUL,SIL RUB,.94X.66	2.00			
641-16289	SCRW,TAP,6-32X.25,PNH,TORX,ZN	8.00			
704-16432	HEATSINK,AMP,DBL,RV8	1.00			
Mounting Bracket Assembly (Option)					
630-08670	WSHR,FIN,#10,NYL,BLK	4.00			
640-08671	SCRW,10-32X3/4,FH,PH,BLK	4.00			
640-14680	SCRW,M4X14MM,FH,SCKT,SS	4.00			
701-15813	BRACKET,MTG,RACK,4U,RV8	2.00			
Power Cord Options					
680-15223	CORD,POWER,IEC,15A,14G,2M,NA	1.00	N.America		
680-15217	CORD,POWER,IEC,10A,1MM,2M,EURO	1.00	Europe		
680-15202	CORD,POWER,IEC,10A,1MM,2M,UK	1.00	United Kingdom		
Packaging/Miscellaneous					
070-15838	GUIDE,USER,RV8	1.00			
070-16011	NOTES,RELEASE,RV8	1.00			

PART NO	DESCRIPTION	QTY	EFFECT.	INACT.	REFERENCE INFO.
460-08452	BAT,ALK,AAA	4.00			
480-15840	ANTENNA,AM,LOOP,75X168MM	1.00			
480-15841	ANTENNA,FM,"F",1.5M L	1.00			
480-15842	ANTENNA,FM,PAL,1.5M L	1.00			
560-16125	ADPTR,RF CONN,F-MALE>PAL-MALE	1.00			
730-15818	BOX,26.75X23.375X15.25,BLANK	1.00			OUTER BOX
730-15819	BOX,25.875X22.5X14,LEXICON	1.00			INNER BOX
730-15821	INSERT,FOAM,BASE,4UX19	1.00			
730-15822	INSERT,FOAM,TOP,4UX19	1.00			
730-15823	BOX,18.75X12.625X2.5	1.00			
730-15829	TRAY,ACCESSORY,RV8	1.00			

REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
1	ADD ASSEMBLY SEQUENCE, CHG BOM NO. PER DCR #010109-01	AN 1/11/01 RL 1/17/01 WH 1/17/01	CW 1/17/01 KB 1/17/01
2	ADD 023-16129 VCO ASSY PER ECO #030314-00	AN 5/5/03 CLC 5/8/03	CW 5/9/03 KAB 5/12/03

STEP 5

SOLDER SEAM BETWEEN COVER & HOUSING
TYPICAL – 4 EDGES



STEP 3

INSTALL COVER
#700-14839
ONTO HOUSING

STEP 4

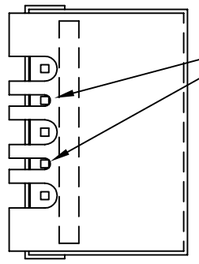
SOLDER BOX SEAMS
TYPICAL – 4 CORNERS

STEP 1

SOLDER BD ASSY
TO HOUSING
#700-14838
AT TAB

STEP 2

SOLDER 2 PINS
TO HOUSING



0.07 [1.8MM] MIN LENGTH
OF PIN TO BE FREE OF SOLDER

VCO BD ASSY
#023-14837
OR
#023-16129

RELEASED COPY

MAY 15 2003

NOTES

1. PART NO.'S SHOWN FOR REFERENCE ONLY SEE BOM #022-14458.
2. STEPS 4 & 5: ALL HOUSING SEAMS & SEAMS BETWEEN THE COVER & HOUSING ARE TO BE SOLDERED PER PCB WORKMANSHIP STANDARDS. JOINTS SHOULD BE SMOOTH AND NEAT WITH NO EXCESS BUILDUP.

	PCM-96
	RV-8
	MC-12/8
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS: .XX ±.010 .XXX ±.005
ANGLES: ±1/2°

MATERIAL

FINISH

DO NOT SCALE DRAWING

ACAD 2000 FILE NAME
14834-2

APPROVALS		DATE
DRAWN	AN	11/13/00
CHECKED	RL	11/13/00
Q.C.	CW	11/13/00
ISSUED	KB	11/13/00

lexicon

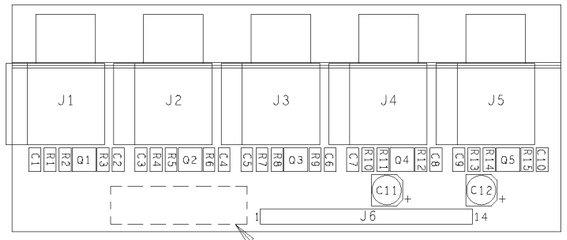
TITLE
ASSY DWG, MECH,
VCO, MCLK

SIZE	FSCM NO.	DWG. NO.	REV.
B		080-14834	2

SCALE 2/1 SHEET 1 OF 1

LEXICON, INC.

REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.



S/N LABEL 740-11287
OR EQUIVALENT
(BOTTOM SIDE)

NOTES

1. LEXICON BOM NO. 023-15619 SUPERSEDES ANY INFORMATION ON THIS DRAWING.
2. PCB ASSEMBLY TO BE PACKAGED IN A STATIC-SHIELDING (FARADAY CAGE) BAG THAT HAS AN ANTI-STATIC (NON-CONDUCTIVE) INNER LAYER. ALSO, THE ASSEMBLY IS TO BE PROPERLY PACKAGED TO PREVENT ANY DAMAGE DURING SHIPMENT.
3. SOLDER PASTE MASK (TOP SIDE) PER LEXICON DOC. NO. 030-15507.

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710- 15500	
NEXT ASSY.	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .01 .005

MATERIAL

FINISH

DO NO SCALE DRAWING

CONTRACT NO.

APPROVALS		DATE
DRAWN	CW	8/6/02
CHECKED	CLC	8/14/02
Q.C.	RWH	8/14/02
ISSUED	MAG	8/15/02

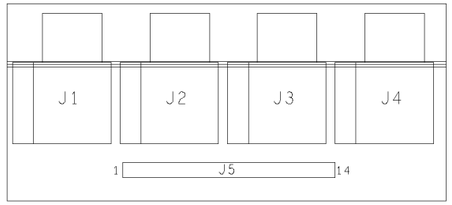
lexicon

PC BD, VIDEO IN BD, RV8
ASSEMBLY DRAWING

SIZE	FSCM NO.	DWG. NO.	REV
B		080-15508	0

SCALE 1:1 SHEET 1 OF 1

REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.



NOTES

1. LEXICON BOM NO. 023-15620 SUPERSEDES ANY INFORMATION ON THIS DRAWING.
2. PCB ASSEMBLY TO BE PACKAGED IN A STATIC-SHIELDING (FARADAY CAGE) BAG THAT HAS AN ANTI-STATIC (NON-CONDUCTIVE) INNER LAYER. ALSO, THE ASSEMBLY IS TO BE PROPERLY PACKAGED TO PREVENT ANY DAMAGE DURING SHIPMENT.

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	710- 15510
NEXT ASSY.	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .01 .005

MATERIAL

FINISH

DO NO SCALE DRAWING

CONTRACT NO.

APPROVALS		DATE
DRAWN	CW	8/6/02
CHECKED	CLC	8/14/02
Q.C.	RWH	8/14/02
ISSUED	MAG	8/15/02

exicon

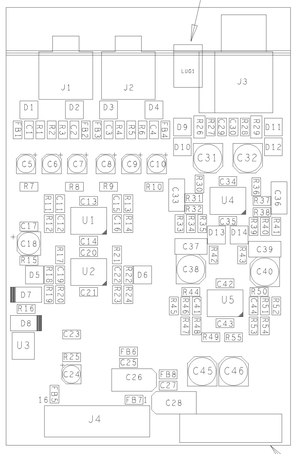
PC BD, VIDEO OUT BD, RV8
ASSEMBLY DRAWING

SIZE	FSCM NO.	DWG. NO.	REV
B		080-15518	0

SCALE 1:1 SHEET 1 OF 1

REV	DESCRIPTION	DRAFTER/ CHECKER	Q.C./ AUTH.
1	CHANGED PER DCR 021030-00	CW 11/20/02 CLC 11/25/02	RWH 11/26/02 MAG 11/26/02
2	CHANGED PER DCR 030317-00	RWH 5/21/03 CLC 5/22/03	CW 5/22/03 MAG 5/22/03
3	ADD LUG1 DETAIL PER DCR 040624-00	RWH 7/1/04 CLC 7/1/04	CW 7/1/04 MAG 7/2/04

#701-09640 KEYSTONE
MOUNTS ON BACK WITH
SHORT SIDE OF BRACKET
ON PCB.
SCRW,4-40X1/4,PNH,PH,BLK
640-02377



S/N LABEL 740-11287
OR EQUIVALENT

NOTES

1. LEXICON BOM NUMBER 023-15621 SUPERSEDES ANY INFORMATION ON THIS DRAWING.
2. ALL COMPONENTS TO BE INSTALLED FROM TOP SIDE OF PCB.
3. LEAD PROTRUSIONS .100" MAXIMUM FROM BOTTOM SIDE OF PCB.
4. UNLESS OTHERWISE SPECIFIED, MOUNT ALL COMPONENTS FLUSH AND PERPENDICULAR (90°+/-1°) TO PCB.
5. PCB ASSEMBLY TO BE PACKAGED IN A STATIC-SHIELDING (FARADAY CAGE) BAG THAT HAS AN ANTI-STATIC (NON-CONDUCTIVE) INNER LAYER. ALSO, THE ASSEMBLY IS TO BE PROPERLY PACKAGED TO PREVENT ANY DAMAGE DURING SHIPMENT.
6. SOLDER PASTE MASK PER LEXICON DOC. NO. 030-15527.
7. BREAK PCB AND CUT EXCESS FLUSH WITH EDGES. THROW OUT BLANK PCB MATERIAL AFTER WAVE SOLDERING.
8. NUTS SUPPLIED WITH CONNECTORS MUST BE BAGGED AND KEPT WITH PCB ASSY. FOR USE DURING MECHANICAL ASSEMBLY.

JUL 09 2004

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NEXT ASSY.	710-15520
APPLICATION	USED ON

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.01
.005

MATERIAL

FINISH

DO NO SCALE DRAWING

CONTRACT NO.

lexicon

APPROVALS		DATE
DRAWN	RWH	8/15/02
CHECKED	CLC	8/19/02
Q.C.	CW	8/26/02
ISSUED	MAG	8/16/02

PC BD,MIC/PREAMP,RV8

ASSEMBLY DRAWING

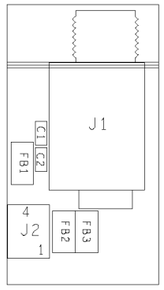
SIZE	FSCM NO.	DWG. NO.	REV
D		080-15528	3

SCALE 1.5 SHEET 1 OF 1

REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 021029-00	CW 11/4/02 CLC 11/14/02	RWH 11/14/02 MAG 11/14/02
2	CHANGED PER DCR 030515-00	RWH 5/22/03 CLC 5/23/03	CW 5/23/03 RWH 5/22/03

NOTES

1. LEXICON BOM NO. 023-15622 SUPERSEDES ANY INFORMATION ON THIS DRAWING.
2. PCB ASSEMBLY TO BE PACKAGED IN A STATIC-SHIELDING (FARADAY CAGE) BAG THAT HAS AN ANTI-STATIC (NON-CONDUCTIVE) INNER LAYER. ALSO, THE ASSEMBLY IS TO BE PROPERLY PACKAGED TO PREVENT ANY DAMAGE DURING SHIPMENT.
3. SOLDER PASTE MASK PER LEXICON DOC. NO. 030-15537.



JUL 22 2005

RELEASED COPY

	710-15530
NEXT ASSY.	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .01 .005

MATERIAL

FINISH

DO NO SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN CW	8/14/02
CHECKED CLC	8/20/02
Q.C. RWH	8/16/02
ISSUED MAG	8/16/02

lexicon

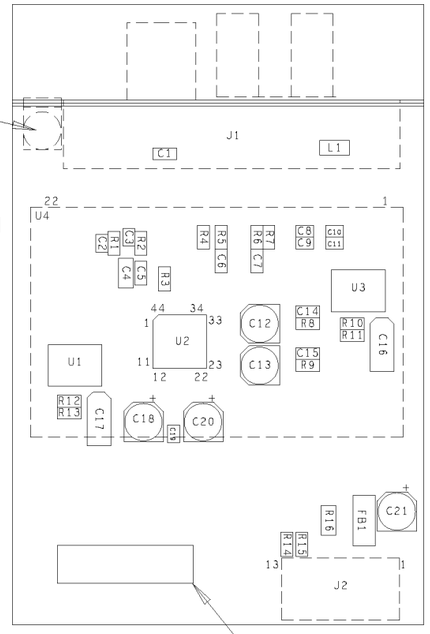
PC BD, HEADPHONE BD, RV8
ASSEMBLY DRAWING

SIZE	FSCM NO.	DWG. NO.	REV
B		080-15538	2

SCALE 1:1 SHEET 1 OF 1

REV	DESCRIPTION	DRAFTER	Q.C.
		CHECKER	AUTHOR.
1	CHANGED PER DCR 030410-00	RWH 4/15/03	CW 4/17/03
		CLC 4/17/03	KAB 4/29/03

#701-09640 KEYSTONE
MOUNTS ON BACK WITH
SHORT SIDE OF BRACKET
ON PCB.
SCRW,4-40X1/4,PNH,PH,ZN
640-01701



S/N LABEL P/N 740-11287
OR EQUIVALENT

NOTES

1. LEXICON BOM NUMBER 023-15627 SUPERSEDES ANY INFORMATION ON THIS DRAWING.
2. ALL COMPONENTS TO BE INSTALLED FROM TOP SIDE OF PCB UNLESS OTHERWISE SPECIFIED.
3. LEAD PROTRUSIONS .100" MAXIMUM FROM BOTTOM SIDE OF PCB.
4. UNLESS OTHERWISE SPECIFIED, MOUNT ALL COMPONENTS FLUSH AND PERPENDICULAR (90^{O}/-1^{O}) TO PCB.
5. PCB ASSEMBLY TO BE PACKAGED IN A STATIC-SHIELDING (FARADAY CAGE) BAG THAT HAS AN ANTI-STATIC (NON-CONDUCTIVE) INNER LAYER. THE ASSEMBLY IS TO BE PROPERLY PACKAGED TO PREVENT ANY DAMAGE DURING SHIPMENT.
6. SOLDER PASTE MASK PER LEXICON DOC. NO. 030-15547.
7. BREAK PCB AND CUT EXCESS FLUSH WITH EDGES. THROW OUT BLANK PCB MATERIAL AFTER WAVE SOLDERING.

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		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MM. TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .X +/-.2 .XX +/- .1	APPROVALS
	710-15540	MATERIAL	DRAWN RWH 12/03/02
NEXT ASSY.	USED ON	FINISH	CHECKED CLC 12/09/02
APPLICATION		DO NO SCALE DRAWING	Q.C. CW 12/09/02
			ISSUED MAG 12/09/02

lexicon

PC BD,TUNER BD,RV8
ASSEMBLY DRAWING

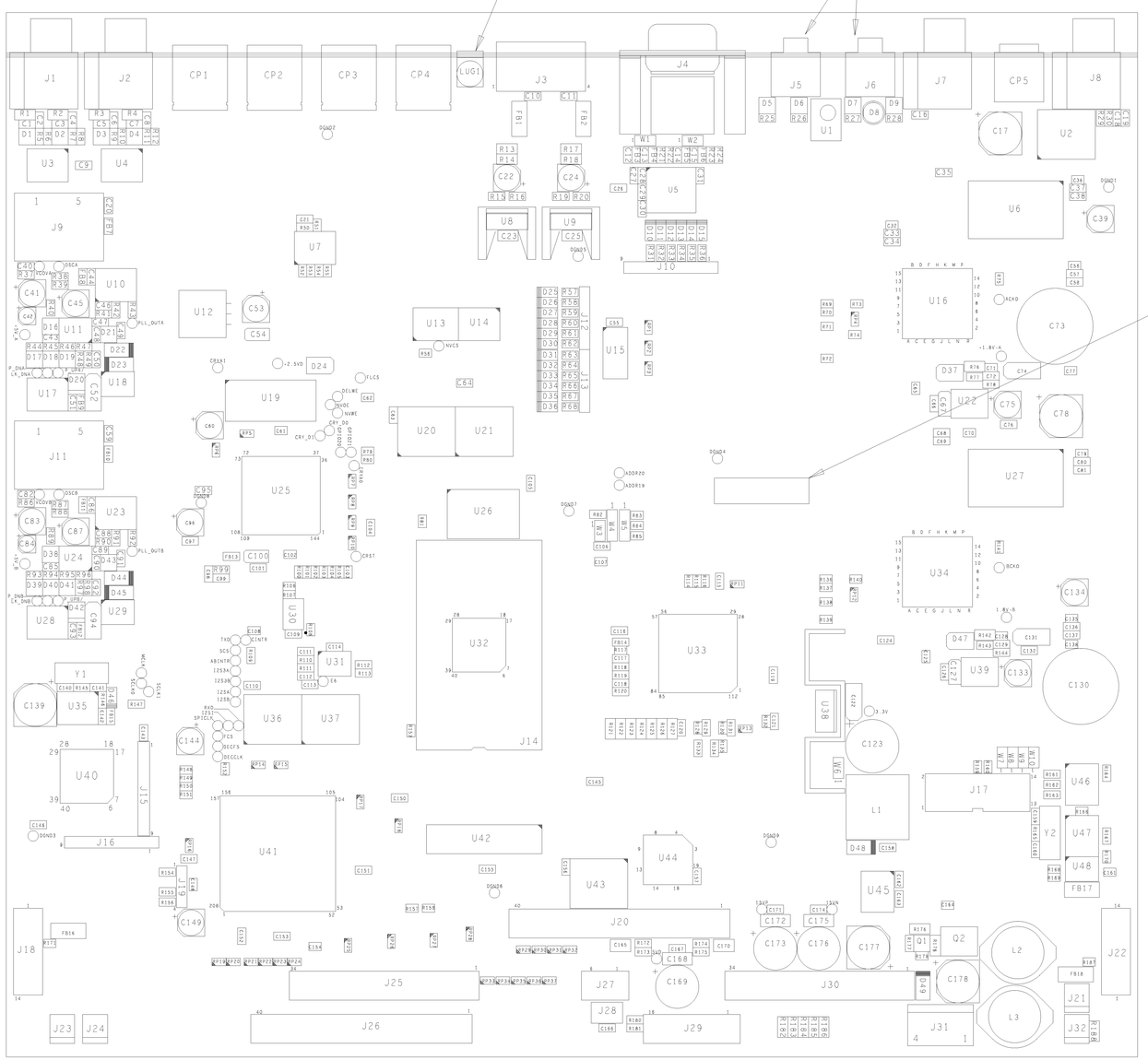
SIZE	FSCM NO.	DWG. NO.	REV
A3		080-15548	1

SCALE 1:1 SHEET 1 OF 1

#701-09640 KEYSTONE
MOUNTS ON BACK WITH
SHORT SIDE OF BRACKET
ON PCB.
SCRW,4-40X1/4,PNH,PH,ZN
640-01701

SEE NOTE 8

SERIAL NUMBER LABEL
740-11287 OR EQUIVALENT



REV	DESCRIPTION	DRAFTER/ CHECKER	Q.C./ AUTH.
1	CHANGED PER DCR 020913-00	RWH 10/22/02	CW 11/06/02
		CLC 11/06/02	MAG 11/06/02
2	CHANGED PER DCR 030307-00	RWH 5/2/03	CW 5/20/03
		CLC 5/19/03	MAG 5/20/03
3	CHANGED PER DCR 030307-00-A	RWH 5/22/03	CW 5/22/03
		CLC 5/22/03	MAG 5/22/03
4	CHANGED PER DCR 030626-00	RWH 9/30/03	ECM 10/9/03
		CLC 10/6/03	MAG 10/9/03
5	CHANGED PER ECO 040422-00	RWH 4/27/04	CW 4/29/04
		CLC 4/29/04	KAB 5/2/04
6	ADDED LUG1 DETAIL PER DCR 040624-00	RWH 7/1/04	CW 7/1/04
		CLC 7/1/04	MAG 7/2/04

NOTES

1. LEXICON BOM NUMBER 023-15615 SUPERSEDES ANY INFORMATION ON THIS DRAWING.
2. ALL COMPONENTS TO BE INSTALLED FROM TOP SIDE OF PCB UNLESS OTHERWISE SPECIFIED.
3. LEAD PROTRUSIONS .100" MAXIMUM FROM BOTTOM SIDE OF PCB.
4. UNLESS OTHERWISE SPECIFIED, MOUNT ALL COMPONENTS FLUSH AND PERPENDICULAR (90°+/-1°) TO PCB.
5. PCB ASSEMBLY TO BE PACKAGED IN A STATIC-SHIELDING (FARADAY CAGE) BAG THAT HAS AN ANTI-STATIC (NON-CONDUCTIVE) INNER LAYER. ALSO, THE ASSEMBLY IS TO BE PROPERLY PACKAGED TO PREVENT ANY DAMAGE DURING SHIPMENT.
6. SOLDER PASTE MASK PER LEXICON DOC. NO. 030-15557.
7. BREAK PCB AND CUT EXCESS FLUSH WITH EDGES. THROW OUT BLANK PCB MATERIAL AFTER WAVE SOLDERING AND PRIOR TO ICT.
8. NUTS SUPPLIED WITH J5 OR J6 CONNECTORS (IF INSTALLED) MUST BE BAGGED AND KEPT WITH PCB ASSY FOR USE DURING MECHANICAL ASSEMBLY.

JUL 15 2004

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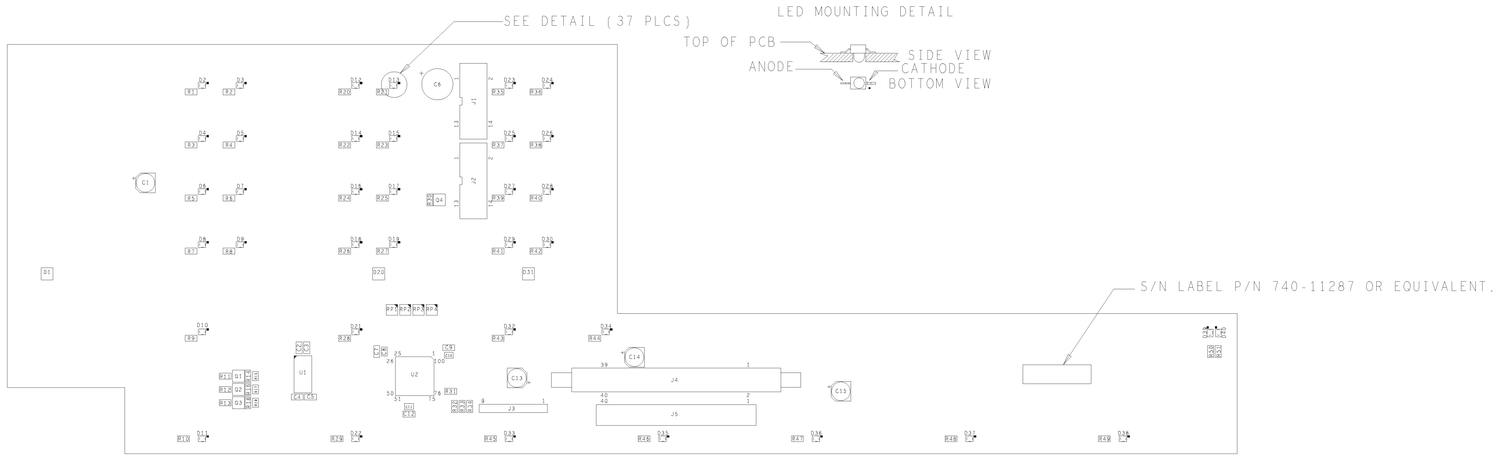
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .01 .005	CONTRACT NO.	lexicon	
MATERIAL	APPROVALS	DATE	PC BD,MAIN BD,RV8
	DRAWN RWH	4/26/02	ASSEMBLY DRAWING
	CHECKED CLC	5/1/02	
710-15550	Q.C. CW	5/1/02	SIZE D / FSCM NO. / DWG. NO. 080-15558 / REV 6
FINISH	ISSUED JV	4/30/02	
NEXT ASSY. / USED ON	SCALE 1.5		SHEET 1 OF 1
APPLICATION / DO NO SCALE DRAWING			

REV	DESCRIPTION	DRAFTER/CHECKER	Q.C./AUTH.
1	CHANGED PER DCR 030821-00	RWH 9/19/03 CLC 9/26/03	CW 11/17/03 KB 9/26/03



LED MOUNTING DETAIL

TOP

NOTES

1. LEXICON BOM NUMBER 023-15616 SUPERSEDES ANY INFORMATION ON THIS DRAWING.
2. COMPONENTS TO BE INSTALLED ON BOTH SIDES OF PCB.
3. LEAD PROTRUSIONS .100" MAXIMUM FROM CIRCUIT SIDE OF PCB.
4. UNLESS OTHERWISE SPECIFIED, MOUNT ALL COMPONENTS FLUSH AND PERPENDICULAR (90°+/-1°) TO PCB.
5. PCB ASSEMBLY TO BE PACKAGED IN A STATIC-SHIELDING (FARADAY CAGE) BAG THAT HAS AN ANTI-STATIC (NON-CONDUCTIVE) INNER LAYER. ALSO, THE ASSEMBLY IS TO BE PROPERLY PACKAGED TO PREVENT ANY DAMAGE DURING SHIPMENT.
6. SOLDER PASTE MASK PER LEXICON DOC. NO. 030-15567.
7. BREAK PCB AND CUT EXCESS FLUSH WITH EDGES. THROW OUT BLANK PCB MATERIAL AFTER SOLDERING AND PRIOR TO IN-CIRCUIT TESTING.

JUL 22 2005

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DOCUMENT CONTROL BLOCK	
SHEET 1	REV 1
SHEET 2	REV 1

710-15560	
NEXT ASSY.	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .01 .005

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

lexicon

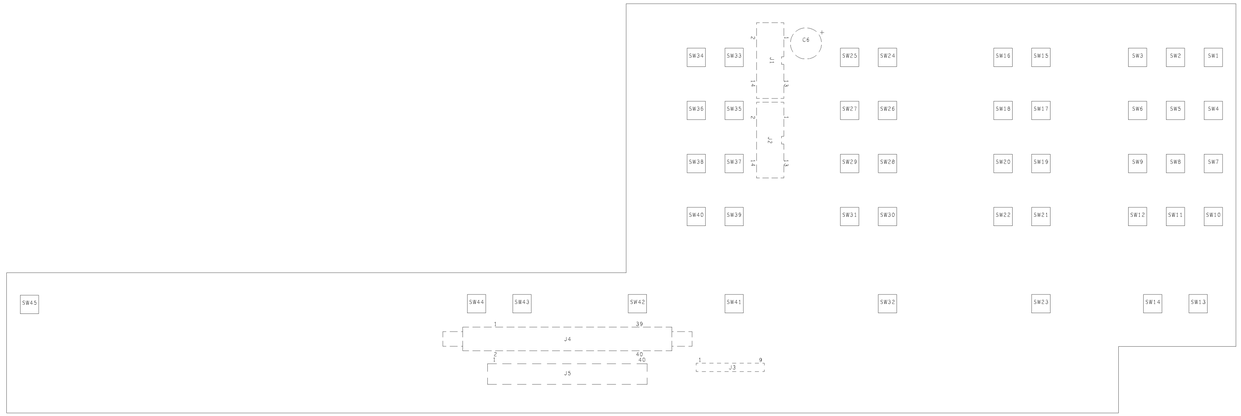
APPROVALS		DATE
DRAWN	CW	7/5/02
CHECKED	CLC	7/9/02
Q.C.	RWH	7/10/02
ISSUED	MAG	7/8/02

PC BD, SW/LED BD, RV8
ASSEMBLY DRAWING

SIZE	FSCM NO.	DWG. NO.	REV
D		080-15568	1

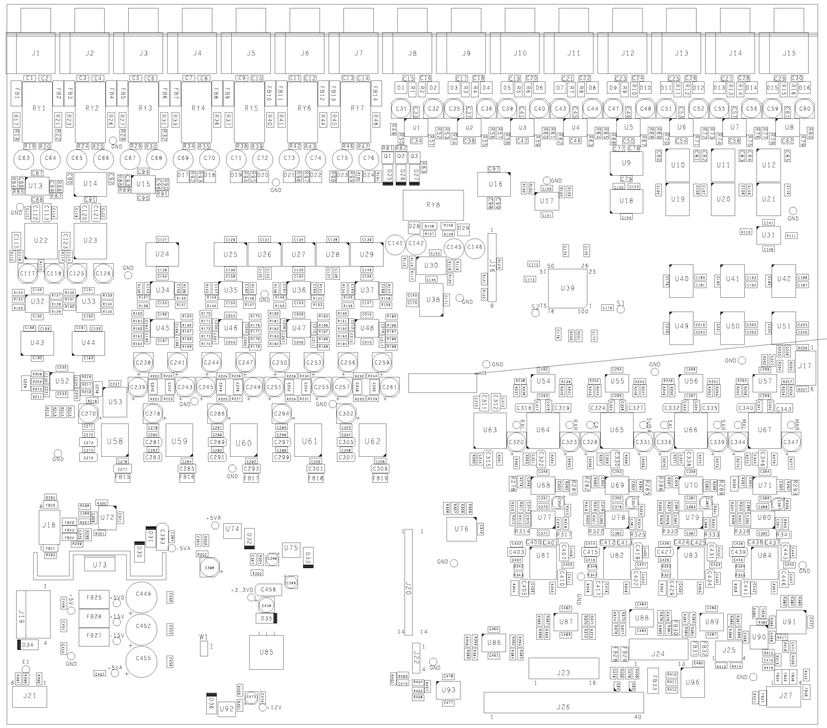
SCALE 1:1 SHEET 1 OF 2

REV	DESCRIPTION	DRAFTER/CHECKER	Q.C./AUTH.
1	CHANGED PER DCR 030821-00	RWH 9/19/03 CLC 9/26/03	CW 11/17/03 KB 9/26/03



BOTTOM

		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .01 .005	CONTRACT NO.	exicon	
			APPROVALS / DATE	PC BD, SW/LED, RV8	
		MATERIAL	DRAWN CW 7/5/02	ASSEMBLY DRAWING	
	710-15560	FINISH	CHECKED CLC 7/9/02	SIZE D / FSCM NO. / DWG. NO. 080-15568	REV 1
NEXT ASSY.	USED ON		Q.C. RWH 7/10/02	SCALE 1:1	SHEET 2 OF 2
APPLICATION		DO NO SCALE DRAWING	ISSUED MAG 7/8/02		



REV	DESCRIPTION	DRAFTER/CHECKER	Q.C./AUTH.
1	CHANGED PER DCR 021107-00	RWH 11/14/02 CLC 11/21/02	CW 11/21/02 MAG 11/21/02
2	CHANGED PER DCR 030407-00	RWH 5/21/03 CLC 5/23/03	CW 5/23/03 MAG 5/23/03
3	CHANGED PER DCR 030729-00	RWH 9/29/03 CLC 10/6/03	CW 10/7/03 MAG 10/7/03
4	CHANGED PER DCR 031125-00	RWH 1/14/04 CBV 1/15/04	ECM 1/30/04 MAG 1/30/04

NOTES

1. LEXICON BOM NUMBER 023-15617 SUPERSEDES ANY INFORMATION ON THIS DRAWING.
2. ALL COMPONENTS TO BE INSTALLED FROM TOP SIDE OF PCB UNLESS OTHERWISE INDICATED.
3. LEAD PROTRUSIONS .100" MAXIMUM FROM BOTTOM SIDE OF PCB.
4. UNLESS OTHERWISE SPECIFIED, MOUNT ALL COMPONENTS FLUSH AND PERPENDICULAR (90°+/-1°) TO PCB.
5. PCB ASSEMBLY TO BE PACKAGED IN A STATIC-SHIELDING (FARADAY CAGE) BAG THAT HAS AN ANTI-STATIC (NON-CONDUCTIVE) INNER LAYER. ALSO, THE ASSEMBLY IS TO BE PROPERLY PACKAGED TO PREVENT ANY DAMAGE DURING SHIPMENT.
6. SOLDER PASTE MASK PER LEXICON DOC. NO. 030-15577.
7. BREAK PCB AT V-GROOVES AND THROW OUT BLANK PCB MATERIAL AFTER WAVE SOLDERING AND PRIOR TO IN-CIRCUIT TESTING.

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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .01 .005		CONTRACT NO.	lexicon
	MATERIAL	APPROVALS	DATE
		DRAWN RWH	8/27/02
		CHECKED CLC	8/29/02
710-15570	FINISH	Q.C. CW	8/29/02
NEXT ASSY. USED ON		ISSUED MAG	8/29/02
APPLICATION	DO NOT SCALE DRAWING	SIZE D / FSCM NO. / DWG. NO. 080-15578 / REV 4	
		SCALE 1:1	SHEET 1 OF 1

PC BD, ANLG I/O, RV8

ASSEMBLY DRAWING

REV	DESCRIPTION	DRAFTER/ CHECKER	Q.C./ AUTH.
1	CHANGED PER DCR 030106-00	RWH 1/13/03	CW 1/14/03
		CLC 1/14/03	MAG 1/14/03
2	CHANGED PER DCR 030421-00	RWH 5/20/03	CW 5/22/03
		CLC 5/22/03	MAG 5/22/03
3	CHANGED HEATSINK ON U32 PER 030623-00	RWH 10/8/03	CW 10/16/03
		CLC 10/16/03	MAG 10/16/03
4	CHANGED PER DCR 031218-00	RWH 12/23/03	CW 12/30/03
		MJD 12/27/03	MAG 12/30/03

NOTES

1. LEXICON BOM NUMBER 023-15618 SUPERSEDES ANY INFORMATION ON THIS DRAWING.
2. ALL COMPONENTS TO BE INSTALLED FROM TOP SIDE OF PCB UNLESS OTHERWISE SPECIFIED.
3. LEAD PROTRUSIONS .100" MAXIMUM FROM BOTTOM SIDE OF PCB.
4. UNLESS OTHERWISE SPECIFIED, MOUNT ALL COMPONENTS FLUSH AND PERPENDICULAR (90° +/-1°) TO PCB.
5. PCB ASSEMBLY TO BE PACKAGED IN A STATIC-SHIELDING (FARADAY CAGE) BAG THAT HAS AN ANTI-STATIC (NON-CONDUCTIVE) INNER LAYER. ALSO, THE ASSEMBLY IS TO BE PROPERLY PACKAGED TO PREVENT ANY DAMAGE DURING SHIPMENT.
6. SOLDER PASTE MASK PER LEXICON DOC. NO. 030-15587.
7. BREAK PCB AND CUT EXCESS FLUSH WITH EDGES. THROW OUT BLANK PCB MATERIAL AFTER WAVE SOLDERING AND PRIOR TO ICT.

S/N LABEL 740-11287
OR EQUIVALENT

JUL 22 2005

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	710-15580
NEXT ASSY.	USED ON
APPLICATION	DO NO SCALE DRAWING

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .01 .005

MATERIAL

FINISH

CONTRACT NO.

lexicon

APPROVALS		DATE
DRAWN	RWH	8/12/02
CHECKED	CLC	8/14/02
Q.C.	CW	8/15/02
ISSUED	MAG	8/15/02

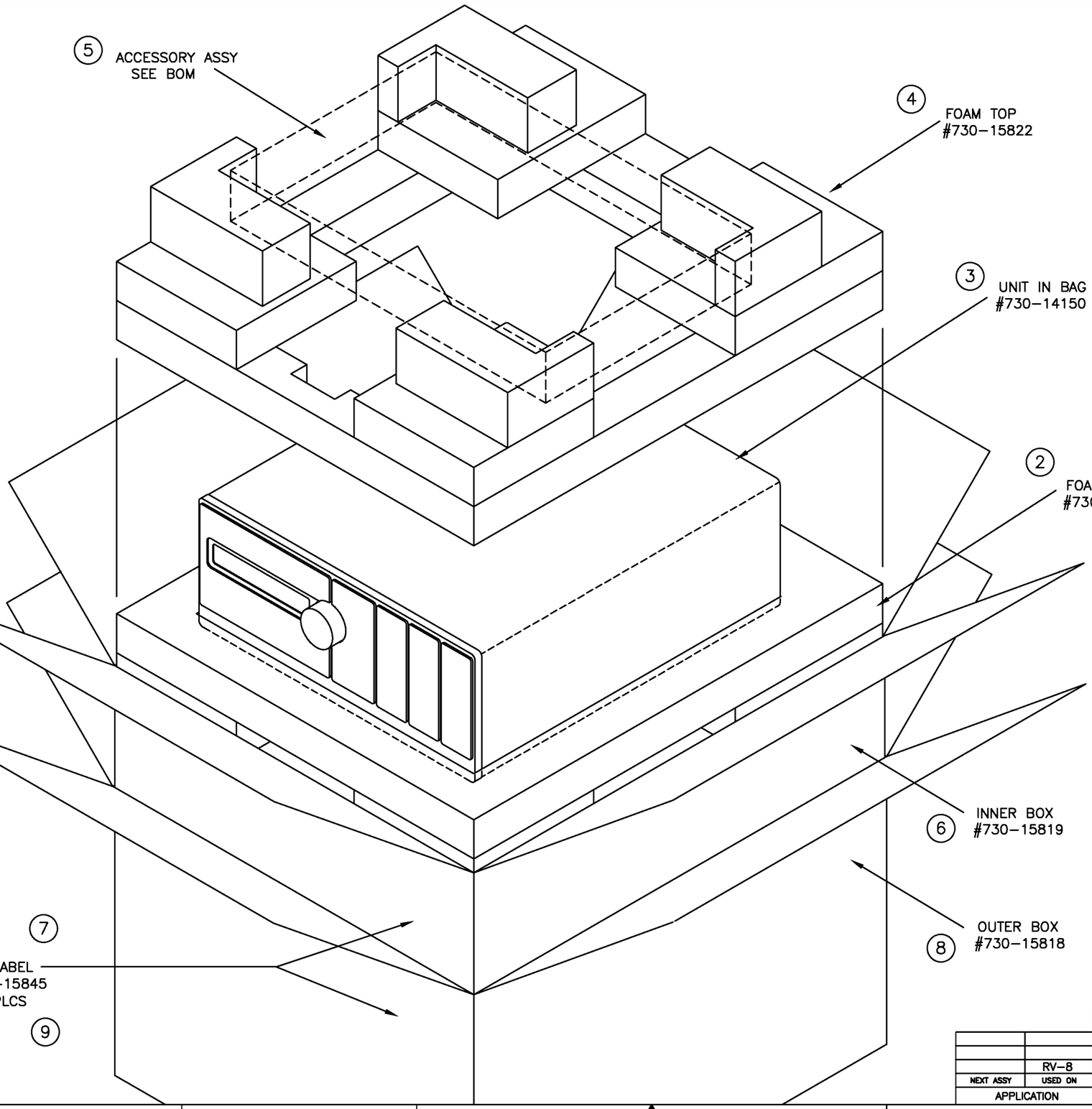
PC BD, VIDEO BD, RV8

ASSEMBLY DRAWING

SIZE	FSCM NO.	DWG. NO.	REV
D		080-15588	4

SCALE 1.5 SHEET 1 OF 1

REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH



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MAY 14 2004

NOTES

1. PART NUMBERS SHOWN ARE FOR REFERENCE ONLY & DO NOT SUPERSEDE BOM'S.
2. PLACE BOTTOM FOAM INSERT IN BOTTOM OF BOX.
3. PLACE UNIT IN BAG. FOLD AND TAPE BAG WITH CREASES AND TAPE ON BOTTOM SIDE OF UNIT. USE CLEAR TAPE. SET UNIT IN BOTTOM INSERT.
4. PLACE TOP FOAM INSERT AROUND UNIT.
5. PLACE ACCESSORY KIT ON TOP OF UNIT BETWEEN NOTCHED FOAM BLOCKS.
6. CLOSE INNER BOX FLAPS AND TAPE.
7. ADD ID LABEL TO INNER BOX IN SPACE PROVIDED.
8. SLIP INNER BOX INTO OUTER SHIPPING BOX, CLOSE FLAPS AND TAPE.
9. PLACE SECOND ID LABEL ON OUTER SHIPPING BOX.

MAY 14 2004

RV-8	
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS: ANGLES:
XX ±.010 ±1/2°
XXX ±.005
MATERIAL
FINISH
DO NOT SCALE DRAWING

ACAD 2002 FILE NAME: 15644-0

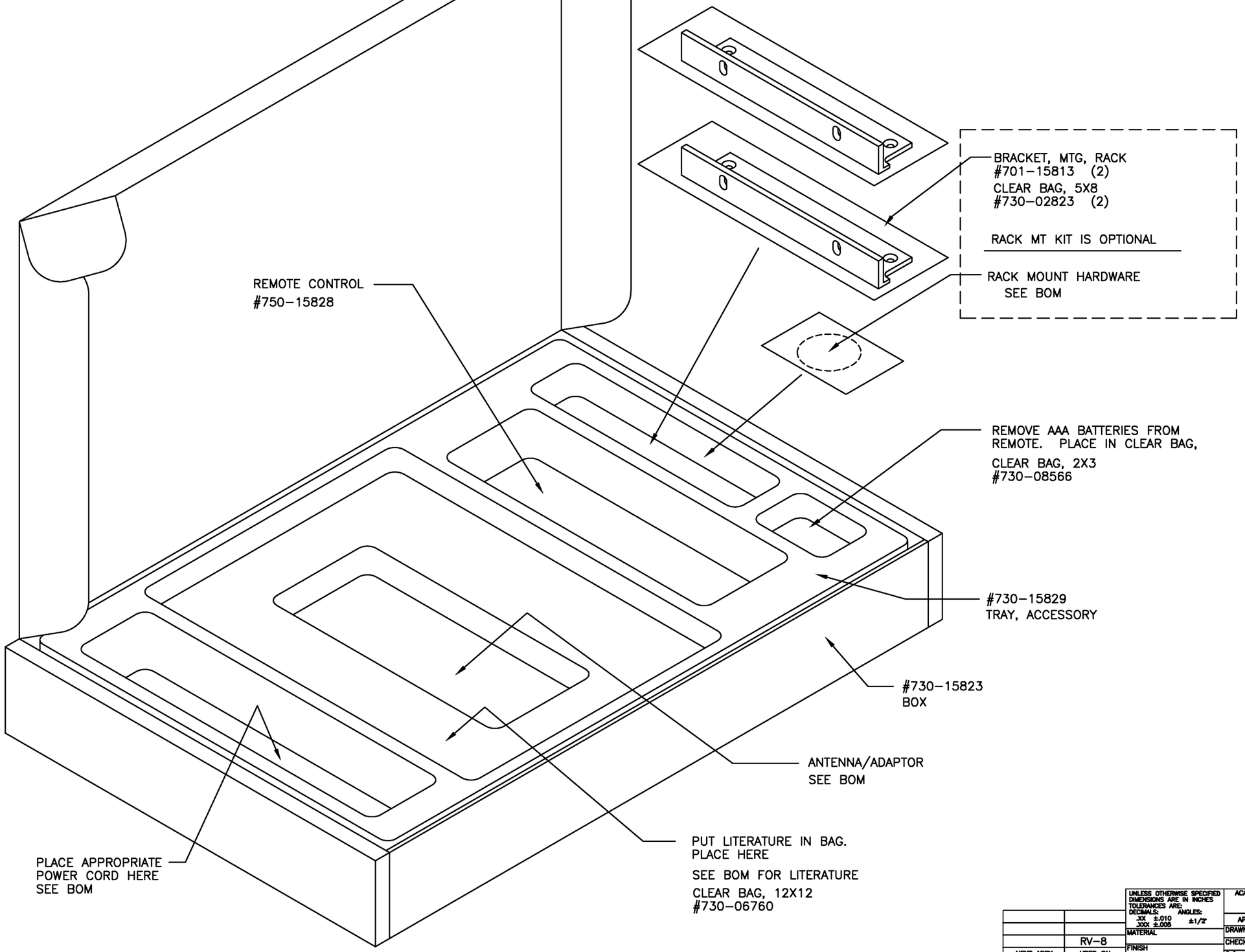
APPROVALS		DATE
DRAWN	AN	4/23/03
CHECKED	MJD	1/8/04
Q.C.	CW	5/13/04
ISSUED	KB	5/13/04

TITLE: ASSEMBLY DWG, SHIPMENT, RV-8

SIZE	FSCM NO.	DWG. NO.	REV.
B		080-15644	0

SCALE N/A SHEET 1 OF 1

REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
1	CHG BATTERY CALLOUT PER ECO 041013-00	AN 11/8/04 CLC 11/18/04	CW 12/14/04 MAG 12/14/04



NOTES

1. PART NUMBERS SHOWN ARE FOR REFERENCE ONLY AND DO NOT SUPERSEDE BOM'S.
2. PLACE ITEMS IN TRAY CAVITIES AS SHOWN.
3. CLOSE COVER OF COMPLETED KIT AND TAPE.

	RV-8
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS: .XX ±.010 .XXX ±.005 ANGLES: ±1/2°
MATERIAL
FINISH
DO NOT SCALE DRAWING

ACAD 2002 FILE NAME: 15645-1

APPROVALS		DATE
DRAWN	AN	8/12/03
CHECKED	MJD	1/8/04
Q.C.	CW	5/13/04
ISSUED	KB	5/13/04

lexicon

TITLE: ASSY DWG, ACCESS, RV-8

SIZE	FSCM NO.	DWG. NO.	REV.
B		080-15645	1

SCALE 1/2 SHEET 1 OF 1

12/15/04

RELEASED COPY

REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
1	ADD LOCTITE TO HANDLES PER DCR #040624–01	AN 7/12/04 CLC 7/13/04	DMC 7/13/04 MAG 7/13/04
2	ADD WSHRS (ITEM 36 & 39) PER ECO #040803–00	AN 8/13/04 CLC 8/16/04	CW 8/28/04 MAG 8/26/04
3	CHG COVER SCRW (ITEM 28) PER ECO #040831–00	AN 9/21/04 CLC 9/23/04	CW 9/30/04 MAG 10/1/04
4	SCR'S ITEM 32 WERE ITEM 30 PER ECO #050503–00	AN 5/26/05 CLC 5/27/05	CW 6/22/05 MAG 7/5/05

12
TORQUE 10–14 IN/LBS 4 PLCS
32
78
RED & BLU WIRES
WHT & BLK WIRES
13 PLCS (COVER) TORQUE 8–10 IN/LBS
28
59
2 PLCS
17
1 SEE #080–15647 FOR FRONT PANEL ASSY
43
REF TO MAIN BD J29
45
56
2 PLCS TO AMPS
51
TO MAIN BD J27
FUSE
230
120
BRN
BLU
55
REF
9
70 SEE NOTE 2
44
30 2 PLCS TORQUE 8–10 IN/LBS
17 3 PLCS
2
SEE DWG #080–15648 FOR VIDEO ASSY
REF 54
52
FROM PHONO & MAIN BD
61
51
54
23 4 PLCS TORQUE 4–6 IN/LBS
65
TORQUE 8–10 IN/LBS 6 PLCS
32
79
63
77
30
8 PLCS (4 CHAN AMP) TORQUE 8–10 IN/LBS
5 PLCS TORQUE 4–6 IN/LBS
26
7
62
55 REF
30 2 PLCS TORQUE 8–10 IN/LBS
18 REF
52
17 2 PLCS
51
REF 20
72
60
37
38
TORQUE 8–10 IN/LBS
30 REF
71
4 PLCS (VIDEO) TORQUE 4–6 IN/LBS
26
15 PLCS (RCA CONN) TORQUE 2–4 IN/LBS
35
55
42
6 PLCS (3 CHAN AMP) TORQUE 8–10 IN/LBS
30
74
76
14
11
SEE DETAIL A ON SHT 2 FOR AC INPUT WIRING

NOTES

1. SEE SHT 3 FOR PARTS LIST
2. LOOP TUNER FFC (ITEM 44) 1 ½ TURNS THRU FERRITE (ITEM 9). CENTER TAPE (ITEM 70) ON SIDE OF FERRITE AND MOUNT TO FOLD OF CENTER PANEL.

DOCUMENT CONTROL BLOCK

DOC. #	DESCRIPTION	REV.
080–15646	SHT 1 OF 3	4
080–15646	SHT 2 OF 3	2
080–15646	SHT 3 OF 3	4

NEXT ASSY	RV–8
APPLICATION	USED ON
DO NOT SCALE DRAWING	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS: .XX ±.010 .XXX ±.005 ANGLES: ±1/2°
MATERIAL
FINISH

ACAD 2002 FILE NAME: 15646–41

APPROVALS		DATE
DRAWN	AN	4/2/03
CHECKED	MJD	1/8/04
Q.C.	CW	5/13/04
ISSUED	KB	5/13/04

lexicon

TITLE: ASSY DWG, CHASSIS, RV–8

SIZE	FSCM NO.	DWG. NO.	REV.
D		080–15646	4

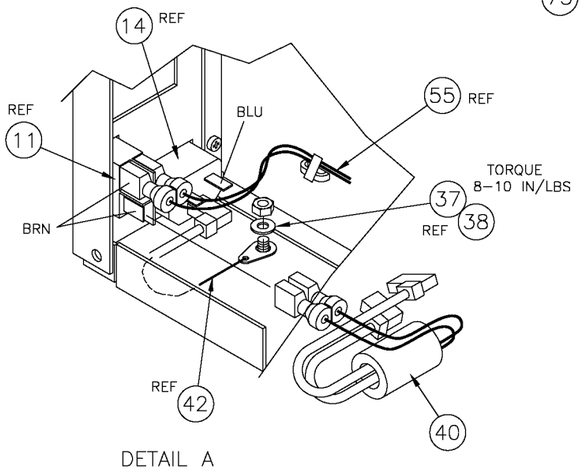
SCALE 1/1 SHEET 1 OF 3

RELEASED COPY

JULY 05 2005

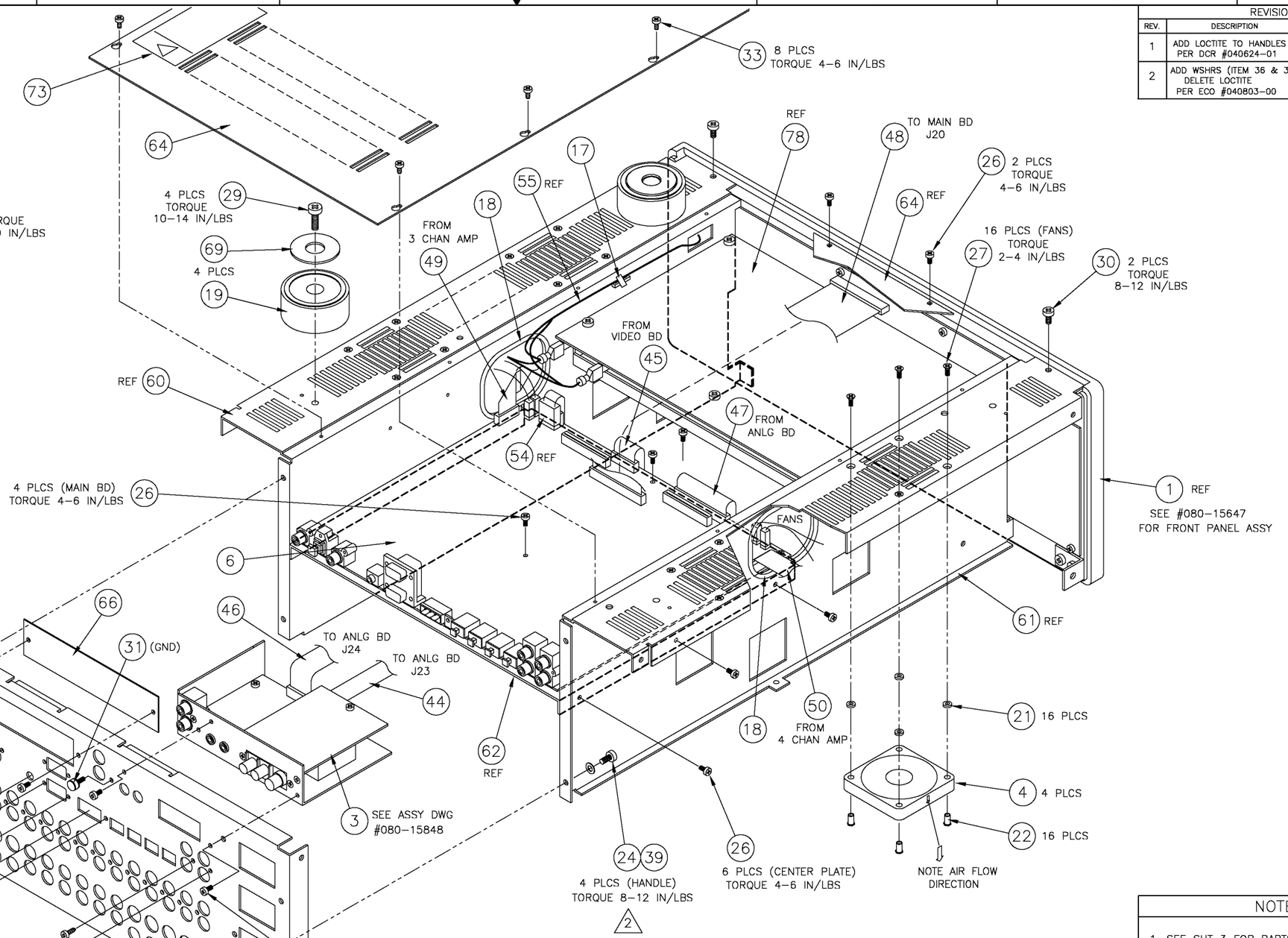
JULY 05 2005

REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
1	ADD LOCTITE TO HANDLES PER DCR #040624-01	AN 7/12/04 CLC 7/13/04	DMC 7/13/04 MAG 7/13/04
2	ADD WSHRS (ITEM 36 & 39), DELETE LOCTITE PER ECO #040803-00	AN 8/13/04 CLC 8/16/04	CW 8/26/04 MAG 8/26/04



DETAIL A

AC INPUT WIRING



NOTES

1. SEE SHT 3 FOR PARTS LIST

	RV-8
NEXT ASSY	USED ON
APPLICATION	DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS: .XX ±.010 .XXX ±.005
ANGLES: ±1/2°
MATERIAL
FINISH

ACAD 2002 FILE NAME: 15646-22

APPROVALS		DATE
DRAWN	AN	12/2/03
CHECKED	MJD	1/6/04
Q.C.	CW	5/13/04
ISSUED	TB	5/13/04

lexicon

TITLE: ASSY DWG, CHASSIS, RV-8

SIZE	FSCM NO.	DWG. NO.	REV.
D		080-15646	2

SCALE 1/1 SHEET 2 OF 3

ITEM#	PART#	DESCRIPTION	QTY	WHERE USED
1.	022-15610	PL, MECH ASSY, FP	1	
2.	022-15611	PL, MECH ASSY, VIDEO	1	
3.	022-15612	PL, MECH ASSY, TUNER/PREAMP	1	
4.	022-15624	PL, FAN ASSY	4	
5.				
6.	023-15615	PL, MAIN BD ASSY	1	
7.	023-15617	PL, ANLG I/O BD ASSY	1	
8.				
9.	270-16120	FERRITE, FLAT CABLE, 1.8 X 1.1	1	TUNER CABLE
10.				
11.	454-13124	SWITCH, ROCKER, 2P1T	1	
12.	470-15213	XFORMER, PWR, TOR	1	
13.	490-13144	CONN, PLUG, .200, 4FC, RA	1	
14.	490-15843	CONN, AC, 3C, SNAP, IEC	1	
15.				
16.	527-12974	CONN, DSUB, JSCKT, 4-40	4	D CONN TO REAR PNL
17.	530-02488	TIE, CABLE, NYL	8	CABLES TO CHASSIS
18.	540-14303	GROMMET, STRIP, SER, NYL	15.5"	CHASSIS
19.	541-15576	FOOT, BLK	4	CHASSIS
20.	550-15844	HANDLE, "U", BLK	2	REAR PANEL
21.	630-12533	WSHR, FL, .12 ID, .25 OD, RUB	16	FANS TO CHASSIS
22.	635-15322	SPCR, M3X8MM, RD, HEX HD	16	FANS TO CHASSIS
23.	640-01711	SCRW, 6-32X1/4, FH, PH, ZN	4	PS TO PS MTG PLATE
24.	640-01721	SCRW, 8-32X3/8, PNH, PH, ZN	4	HANDLES TO REAR PNL
25.	640-02377	SCRW, 4-40X1/4, PNH, PH	1	MAIN BD TO REAR PNL
26.	640-10498	SCRW, M3X6MM, PNH, PH	25	CTR PLATE TO CHAS (6) MAIN BD TO CTR PLATE (4) ANLG BD TO CTR PLATE (5) VIDEO ASSY TO REAR PNL (4) TUNER/PREAMP TO REAR PNL (2) OPTION PNL TO REAR PNL (2) BOTTOM PLATE TO FP (2)
27.	640-11284	SCRW, M3X8MM, FH, PH	16	FANS TO CHAS
28.	640-13645	SCRW, M4X10MM, FH, SCKT, BZ	13	COVER TO CHAS
29.	640-15346	SCRW, M5X16MM, PNH, PH	4	FEET TO CHAS
30.	640-15476	SCRW, M4X8MM, PNH, PH	20	FP TO CHAS (4) AMPS TO CHAS & REAR PNL (14) PS MTG PLATE TO CHAS (2)
31.	640-16140	SCRW, 4-40X5/16, THUMB, RH, SS	1	TUNER/PREAMP TO REAR PNL
32.	640-17394	SCR, M4X8MM, PNH, PH, ZN, IT	10	PS&TOROID ASSY TO CHAS (6) XFRMR TO BRKT (4)
33.	641-01703	SCRW, TAP, AB, #4X1/4, PNH, PH	8	BOTTOM PLATE TO CHAS
34.				
35.	641-11466	SCRW, TAP, #4X3/8, PNH, PH, TRI	20	RCA & OPTO CONN TO REAR PNL
36.	644-01747	WSHR, INT STAR, #4	4	D CONN TO REAR PNL
37.	643-10492	NUT, M4X.7MM, KEP	1	CHASSIS GND
38.	644-10494	WSHR, FL, M4 CL X 9 OD X .8MM THK	1	CHASSIS GND
39.	644-01741	WSHR, INT STAR, #8	4	HANDLES TO REAR PNL
40.	680-15697	CABLE, PWR, .187RA/.250 QDC, SLV, 7.5"	1	AC CONN TO PWR SW
41.				
42.	680-15630	WIRE, 14G, G/Y, 3.5", .187 QDC/LUG #8	1	AC CONN TO CHASSIS GND
43.	680-15631	CABLE, FFC, 4C, 14"	1	HEADPHONE BD TO ANLG BD
44.	680-15632	CABLE, FFC, 13C, 15"	1	TUNER TO ANLG BD
45.	680-15633	CABLE, FFC, 16C, 10"	1	VIDEO BD TO MAIN BD
46.	680-15634	CABLE, FFC, 16C, 14"	1	PREAMP BD TO ANLG BD
47.	680-15636	CABLE, FFC, 40C, 6"	1	ANLG BD TO MAIN BD
48.	680-15637	CABLE, FFC, 40C, 12"	1	FP TO MAIN BD
49.	680-16122	CABLE, FFC, 14C, 4", FOLD	1	3 CHAN AMP TO MAIN BD
50.	680-15639	CABLE, FFC, 14C, 4"	1	4 CHAN AMP TO MAIN BD
51.	680-15640	CABLE, FFC, 6C, 4"	3	3 CH & 4 CH AMP TO ANLG BD, PS & TOR ASSY TO MAIN BD
52.	680-15641	CABLE, FFC, 6C, 6"	2	3 CH & 4 CH AMP TO ANLG BD
53.				

ITEM#	PART#	DESCRIPTION	QTY	WHERE USED
54.	680-15642	CABLE, HSGX2, 10C/4C X 3, 16.5"	1	PWR SUP TO MAIN, ANLG & VIDEO BDS
55.	680-15643	CABLE, HSG/QDC, 18/14AWG, 22.5"	1	PWR SW TO PWR SUPPLIES
56.	680-15698	CABLE, HSG/HSG, 6C, 12"	2	PWR SUP TO AMPS
57.				
58.				
59.	700-15809	COVER, 4U	1	
60.	700-15810	CHASSIS, LEFT	1	
61.	700-15811	CHASSIS, RIGHT	1	
62.	700-15812	PLATE, CENTER, CHASSIS	1	
63.	702-15803	PANEL, REAR	1	
64.	702-15806	PLATE, BOTTOM	1	
65.	702-15807	PANEL, MTG, PS	1	
66.	702-15808	PANEL, OPTION, BLANK	1	REAR PANEL
67.				
68.				
69.	720-15425	PAD, FOOT	4	FOOT
70.	720-16123	TAPE, FOAM, DBL-STK, 1.75X.4X.025	1	FERRITE TO CTR PLATE
71.	740-08556	LABEL, GROUND SYMBOL, 0.5" DIA	1	CHASSIS
72.	740-09538	LABEL, S/N, CHASSIS	1	REAR PANEL
73.	740-14888	LABEL, LIC/PAT/WARN	1	BOTTOM PLATE
74.	740-16015 740-16017	LABEL, 100-120V LABEL, 220-240V	1	REAR PANEL
75.				
76.	022-16444	MECH ASSY, AMP, 3 CHAN	1	
77.	022-16445	MECH ASSY, AMP, 4 CHAN	1	
78.	022-16442	MECH ASSY, PS	1	
79.	750-15827	PWR SUP, +-5V/+-15V, 65W	1	
80.				

REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
1	ADD LOCTITE TO HANDLES PER DCR #040624-01	AN 7/12/04 CLC 7/13/04	DMC 7/13/04 MAG 7/13/04
2	DELETE LOCTITE (ITEM 10), ADD WSHRS (ITEM 38 & 39) PER ECO #040803-00	AN 8/13/04 CLC 8/16/04	CW 8/28/04 MAG 8/26/04
3	SCRW (ITEM 28) WAS 640-16121 PER ECO #040831-01	AN 9/21/04 CLC 9/23/04	CW 9/30/04 MAG 10/1/04
4	SCR'S ITEM 32 WERE ITEM 30 PER ECO #050503-00	AN 5/26/05 CLC 5/27/05	CW 6/22/05 MAG 7/5/05

NOTES

1. PART NUMBER LISTING IS FOR REFERENCE ONLY AND DOES NOT SUPERSEDE THE BOM:
   #022-15609 CHASSIS ASSY

	RV-8	
NEXT ASSY	USED ON	
APPLICATION		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS: .XX ±.010 .XXX ±.005
ANGLES: ±1/2°
MATERIAL
FINISH
DO NOT SCALE DRAWING

ACAD 2002 FILE NAME: 15646-43

APPROVALS		DATE
DRAWN	AN	4/2/04
CHECKED	MJD	1/8/04
Q.C.	CW	5/13/04
ISSUED	KB	5/13/04

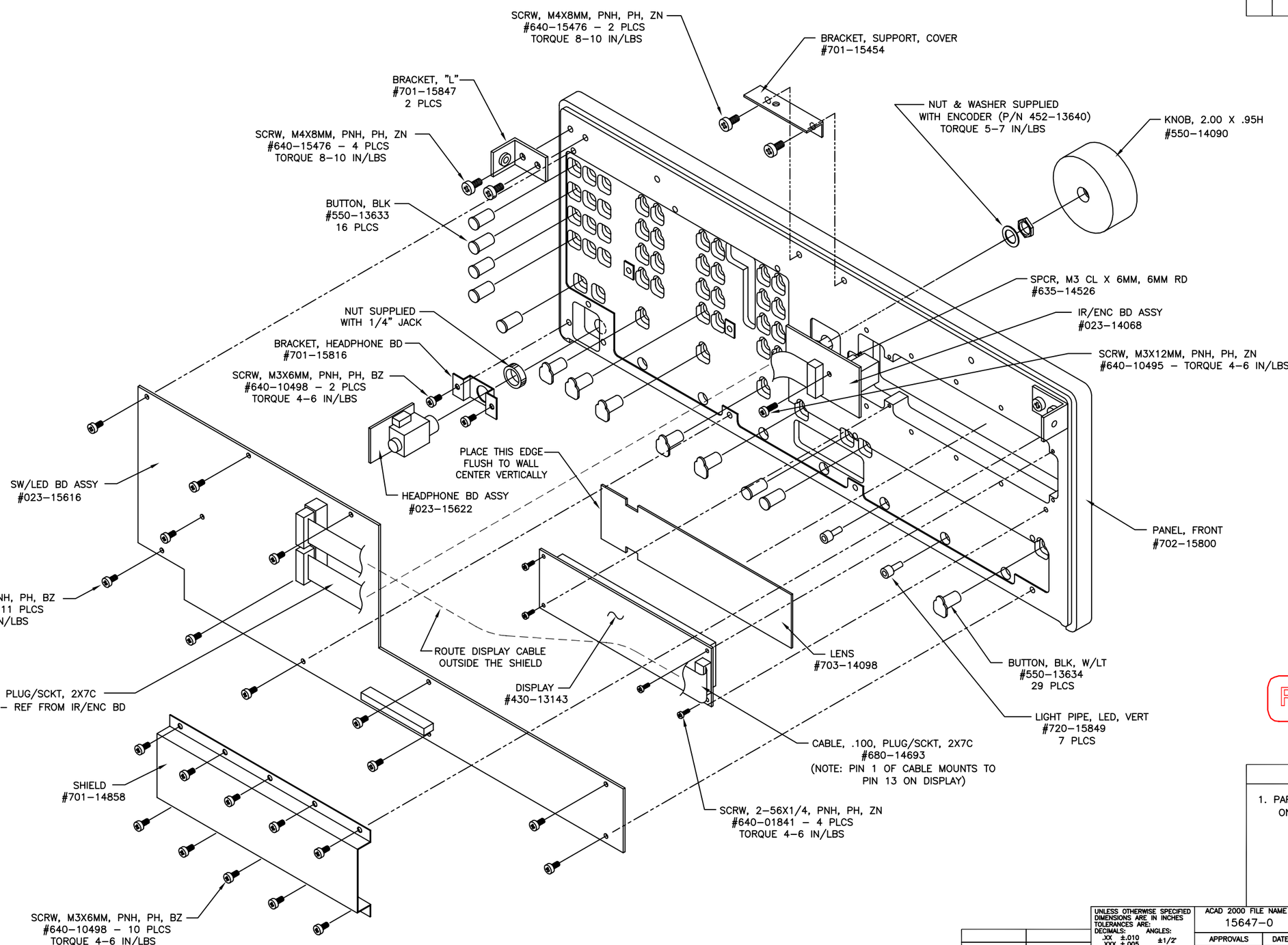
exicon

TITLE: ASSY DWG, CHASSIS, RV-8

SIZE	FSCM NO.	DWG. NO.	REV.
B		080-15646	4

SCALE: NONE SHEET 3 OF 3

REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH



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MAY 20 2004

NOTES

1. PART NUMBER LISTING IS FOR REFERENCE ONLY AND DOES NOT SUPERSEDE BOM.

	RV–8
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS: .XX ±.010 .XXX ±.005
ANGLES: ±1/2°
MATERIAL
FINISH
DO NOT SCALE DRAWING

ACAD 2000 FILE NAME: 15647–0

APPROVALS		DATE
DRAWN	AN	4/1/03
CHECKED	CLC	6/4/03
Q.C.	CW	6/23/03
ISSUED	MAG	6/24/03

lexicon

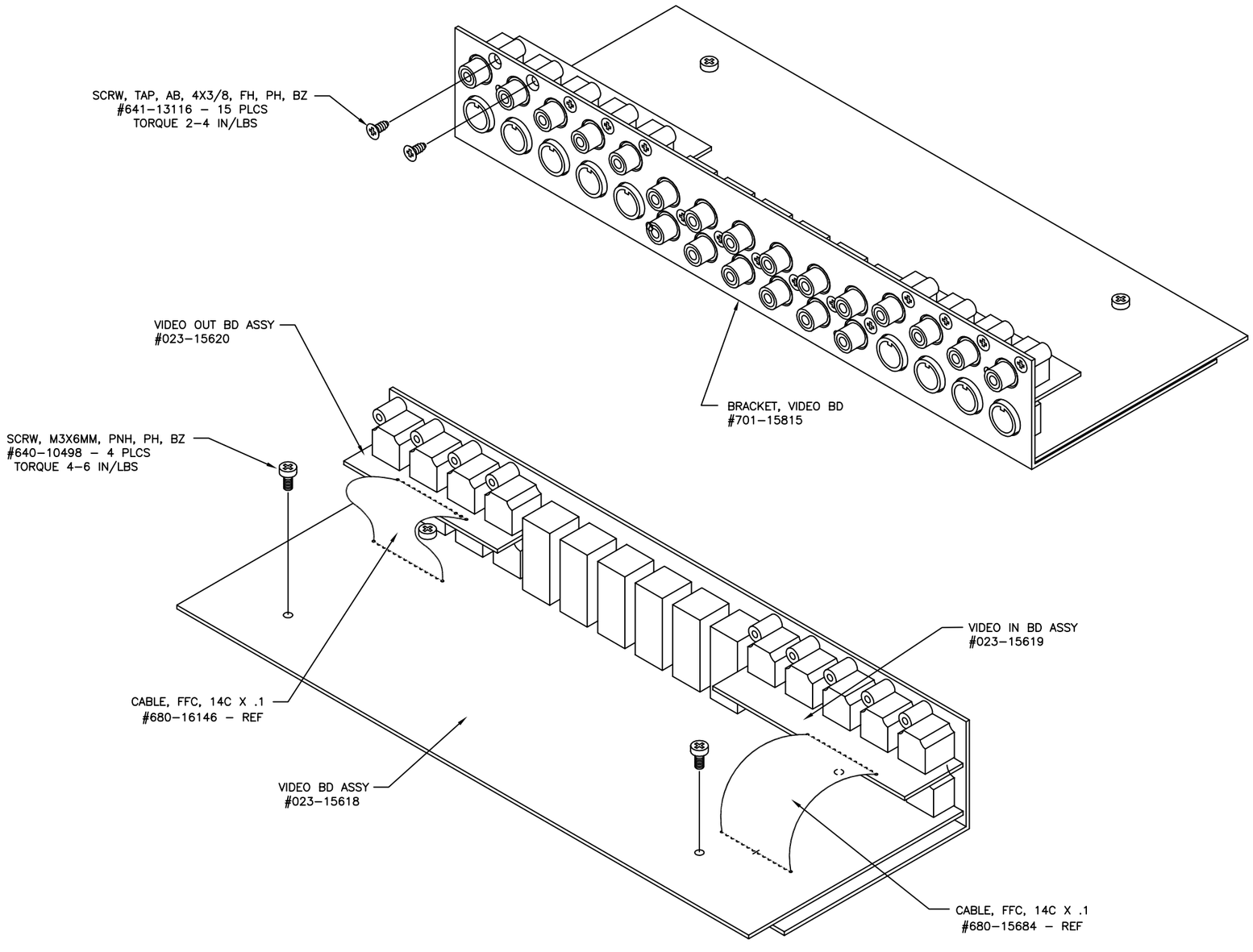
TITLE: ASSY DWG, MECH, FP, RV–8

SIZE	FSCM NO.	DWG. NO.	REV.
B		080–15647	0

SCALE 1/2 SHEET 1 OF 1

LEXICON, INC.

REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH



NOTES

1. PART NUMBER LISTING IS FOR REFERENCE ONLY AND DOES NOT SUPERSEDE BOM.

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JAN 07 2004

RV-8	
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS: ANGLES:
.XX ±.010 ±1/2°
.XXX ±.005
MATERIAL
FINISH
DO NOT SCALE DRAWING

ACAD 2000 FILE NAME: 15648-0

APPROVALS		DATE
DRAWN	AN	1/15/03
CHECKED	CLC	6/4/03
Q.C.	CW	6/23/03
ISSUED	MAG	6/24/03

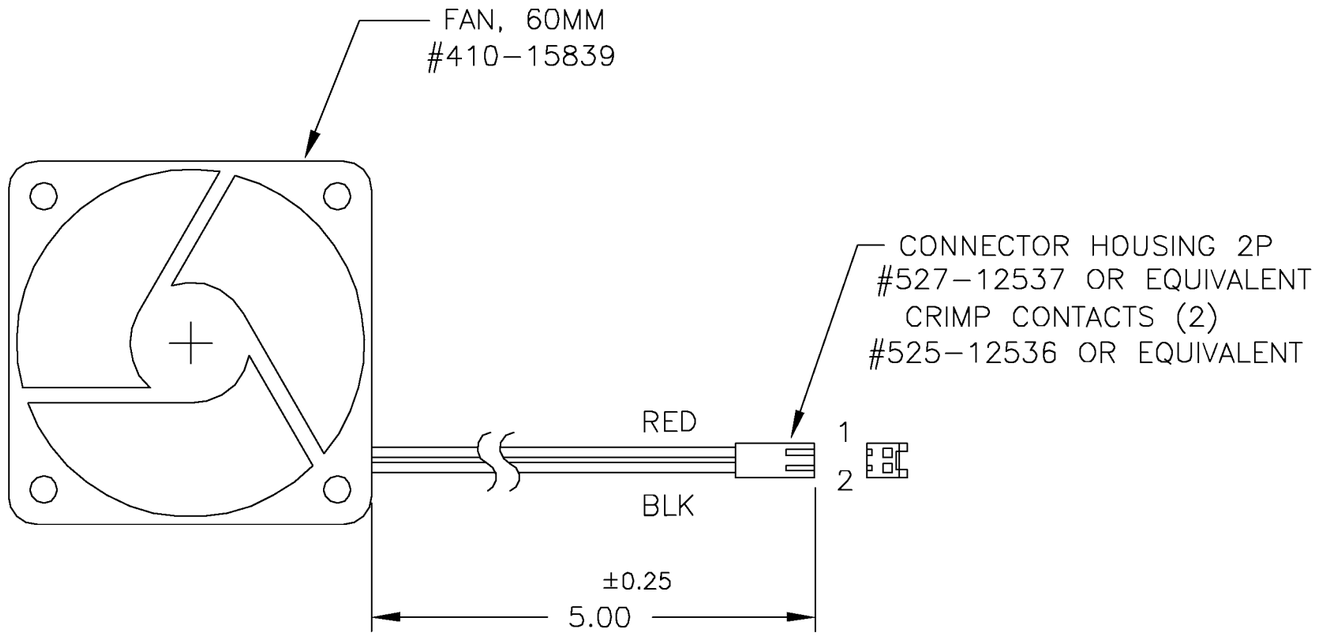
lexicon

TITLE: ASSEMBLY DWG, MECH, VIDEO, RV-8

SIZE	FSCM NO.	DWG. NO.	REV.
B		080-15648	0

SCALE 1/2 SHEET 1 OF 1

LEXICON, INC.



NOTE:

LEXICON P/N'S 527-12537 & 525-12536 REFER TO AMP P/N'S. EQUIVALENT PARTS FROM OTHER VENDORS ARE ALLOWED, PROVIDED BOTH THE HOUSING & THE CONTACT ARE MADE BY THE SAME VENDOR.

REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH

NOTES

1. PART NUMBER LISTING IS FOR REFERENCE ONLY & DOES NOT SUPERSEDE BOM.

APR 2 2004

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	RV-8
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS: .XX ±.D10 .XXX ±.005
ANGLES: ±1/2°

MATERIAL

FINISH

DO NOT SCALE DRAWING

ACAD 2000 FILE NAME
15649-0

APPROVALS		DATE
DRAWN	AN	1/9/03
CHECKED	CLC	6/4/03
Q.C.	CW	6/23/03
ISSUED	MAG	6/24/03

lexicon

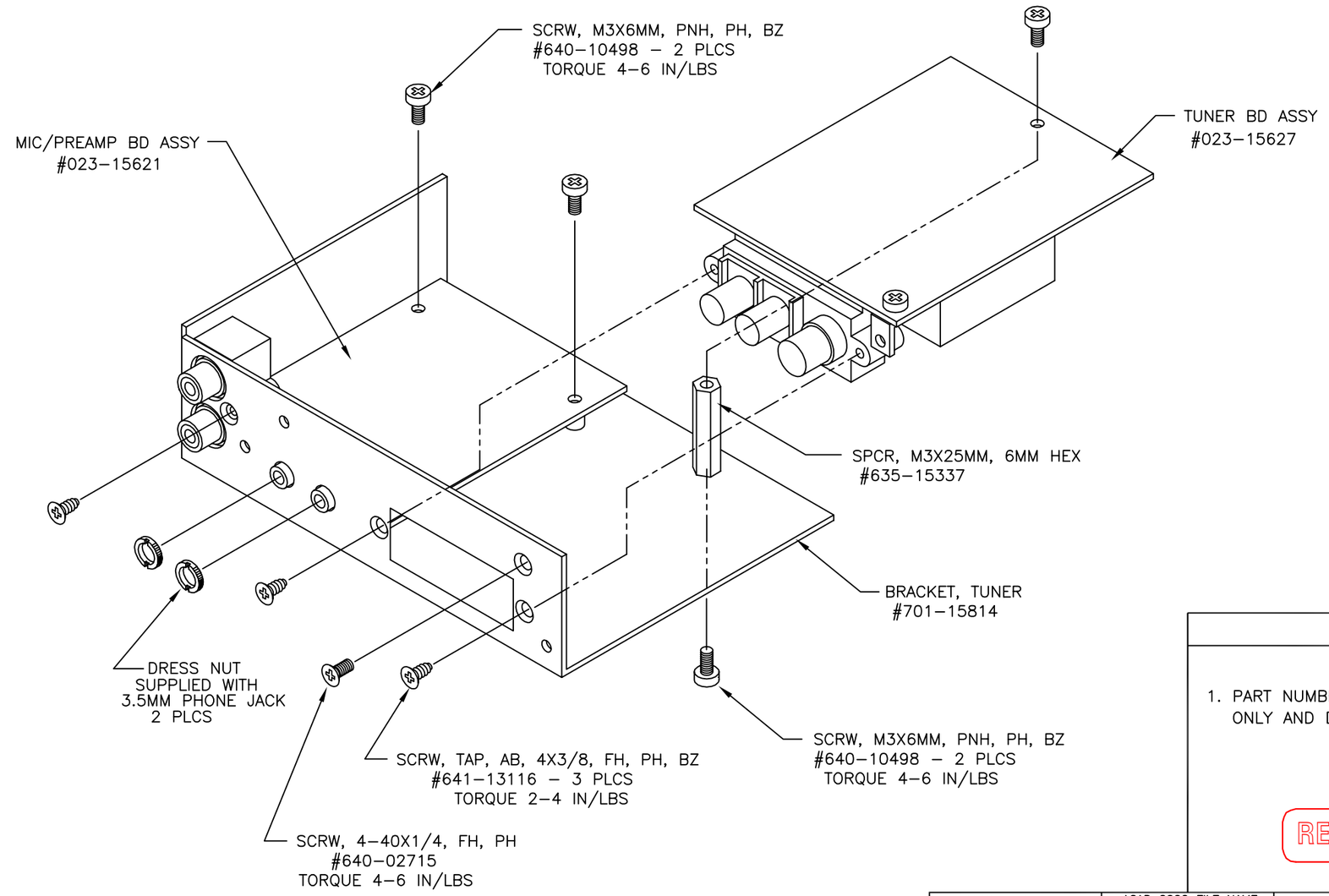
TITLE
ASSY DWG,
FAN, 60MM, 12VDC

SIZE	FSCM NO.	DWG. NO.	REV.
B		080-15649	0

SCALE N/A SHEET 1 OF 1

LEXICON, INC.

REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH



NOTES

1. PART NUMBER LISTING IS FOR REFERENCE ONLY AND DOES NOT SUPERSEDE THE BOM.

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DEC 18 2003

	RV–8
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS: .XX ±.010 .XXX ±.005 ANGLES: ±1/2°

MATERIAL

FINISH

DO NOT SCALE DRAWING

ACAD 2002 FILE NAME
15848–0

APPROVALS		DATE
DRAWN	AN	8/12/03
CHECKED	CLC	12/12/03
Q.C.	CW	12/18/03
ISSUED	MAG	12/18/03

lexicon

TITLE
ASSY DWG, MECH,
TUNER/PREAMP, RV–8

SIZE	FSCM NO.	DWG. NO.	REV.
C		080–15848	0

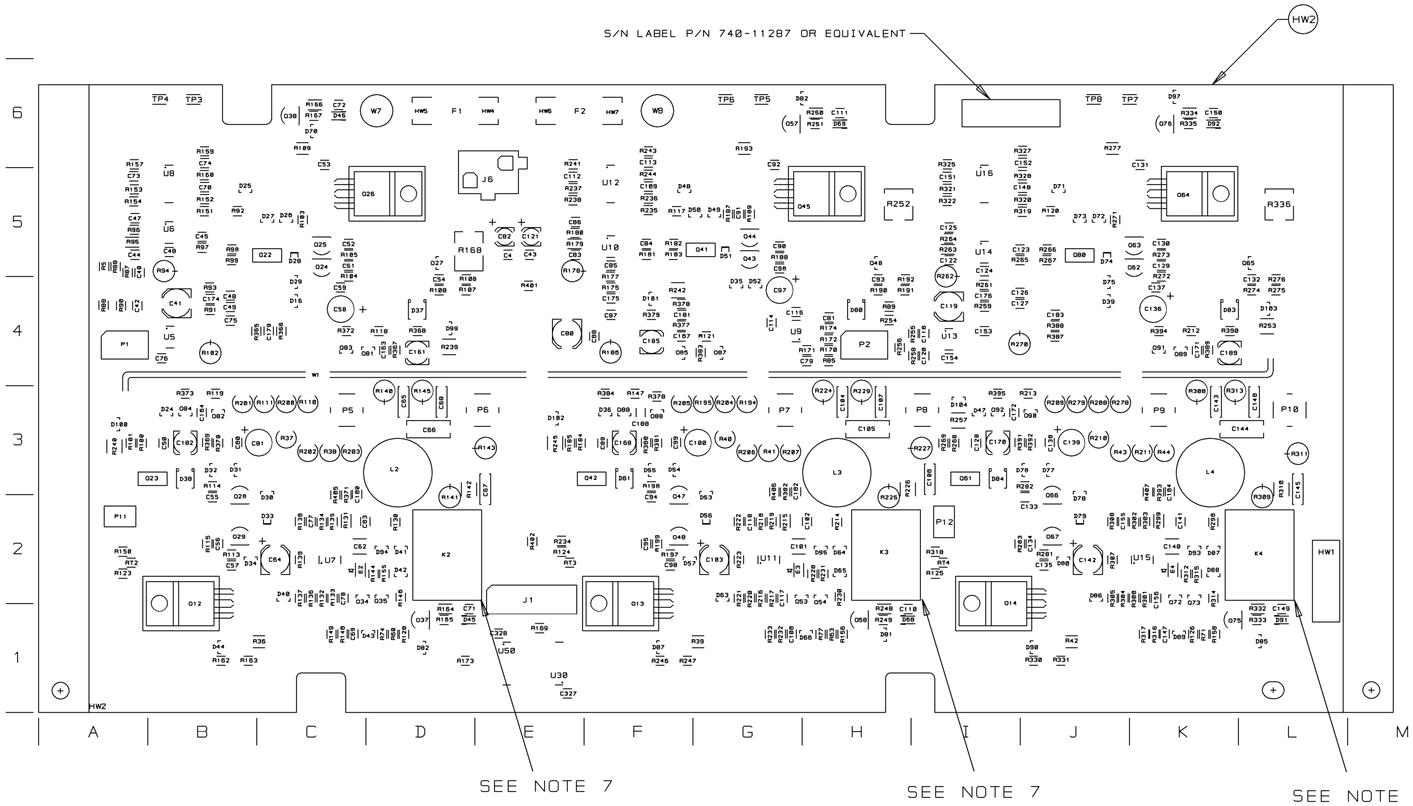
SCALE 1/1 SHEET 1 OF 1

LEXICON, INC.

REVISION HISTORY							
E.C.N.	ZONE	REV	DESCRIPTION	DATE	APPROVED		
					DWN	CM	PE
		1	INITIAL RELEASE	6-26-03	MES		MES
		2	ADD S/N LABEL & NOTES PER ECO 040409-00	4-23-04	MES		MES

RELEASED COPY

COMPONENT MAP
TOP SIDE



NOTES:
1. HSG BOM NUMBER 023-15824 SUPERSEDES ANY INFORMATION ON THIS DRAWING.
2. COMPONENTS TO BE INSTALLED ON TOP SIDE OF PCB, UNLESS OTHERWISE NOTED BY AN ASTERISK (*).
3. ALL LEADS TO BE TRIMMED TO 0.093" OR LESS.
4. UNLESS OTHERWISE SPECIFIED, MOUNT ALL COMPONENTS FLUSH AND PERPENDICULAR (90 DEG +/- 1 DEG) TO PCB.
5. PCB ASSEMBLY TO BE PACKAGED IN A STATIC-SHIELDING (FARADAY CAGE) BAG THAT HAS AN ANTI-STATIC (NON-CONDUCTIVE) INNER LAYER. THE ASSEMBLY IS TO BE PROPERLY PACKAGED TO PREVENT ANY DAMAGE DURING SHIPMENT.
6. SOLDER PASTE MASK PER HSG DOC. NO. 030-16177.
7. THE VENT HOLE ON TOP OF RELAYS K2-4 MUST BE OPENED AFTER THE CLEANING PROCESS, BY EITHER REMOVING THE SEALING TAPE OR CUTTING OFF THE CIRCULAR TAB WITH AN "EXACTO" KNIFE OR SIMILAR CUTTING TOOL. WARNING: THIS STEP MUST BE DONE AFTER THE CLEANING PROCESS, NOT BEFORE. WATER OR CLEANING SOLVENTS ENTERING THE RELAY VENT HOLE WILL DAMAGE THE RELAY.

CROWN DOCUMENT INFORMATION:

WAS CROWN PART NUMBER: 135266-2
FOR SCHEMATIC SEE: 060-16159

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DISTRIBUTION			DWN	MES	6-26-03
			CM		
FILENAME			PE	MES	6-26-03
080-16158_2.TIF					
TOLERANCE UNLESS OTHERWISE SPECIFIED					
.00 = ±.02"					
.000 = ±.010"					
DRILLS = ±.003"					
DO NOT SCALE DRAWING					

CROWN INTERNATIONAL, INC.
1718 W. MISHAWAKA RD.
ELKHART IN. 46517
PHONE 574-294-8000
WWW.CROWNINTL.COM

TITLE: PC, ASSY DWG, AMP MOD, 3CH, RV8

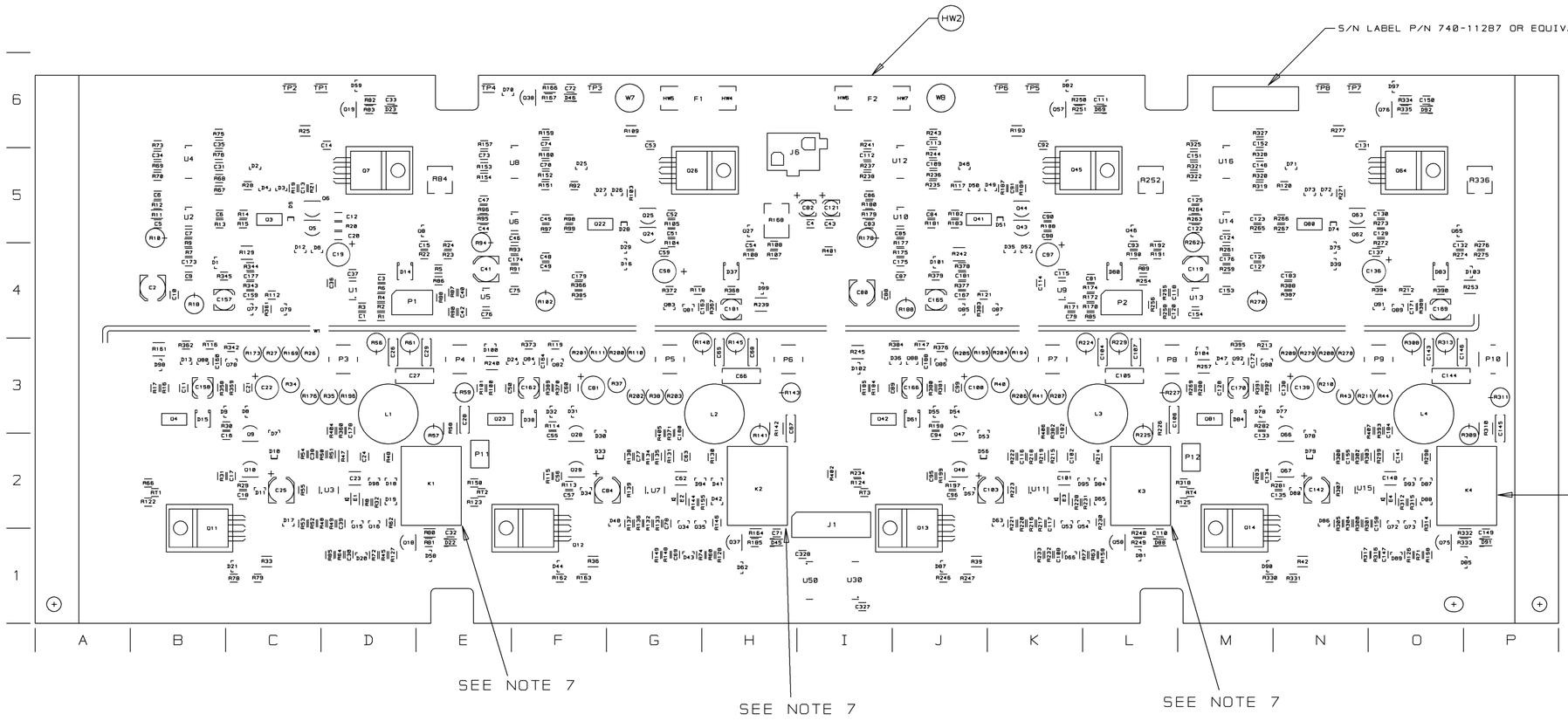
SIZE	DWG NO.	REV
C	080-16158	2

SCALE NONE | PROJ NO. MD500D0 | SHEET 1 OF 1

REVISION HISTORY							
E.C.N.	ZONE	REV	DESCRIPTION	DATE	APPROVED		
					DWN	CM	PE
		1	INITIAL RELEASE	6-26-03	MES		MES
		2	ADD S/N LABEL & NOTES PER ECO 040409-00	4-23-04	MES		MES

RELEASED COPY

COMPONENT MAP
TOP SIDE



NOTES:
1. HSG BOM NUMBER 023-15825 SUPERSEDES ANY INFORMATION ON THIS DRAWING.
2. COMPONENTS TO BE INSTALLED ON TOP SIDE OF PCB, UNLESS OTHERWISE NOTED BY AN ASTERISK (*).
3. ALL LEADS TO BE TRIMMED TO 0.093" OR LESS.
4. UNLESS OTHERWISE SPECIFIED, MOUNT ALL COMPONENTS FLUSH AND PERPENDICULAR (90 DEG +/- 1 DEG) TO PCB.
5. PCB ASSEMBLY TO BE PACKAGED IN A STATIC-SHIELDING (FARADAY CAGE) BAG THAT HAS AN ANTI-STATIC (NON-CONDUCTIVE) INNER LAYER. THE ASSEMBLY IS TO BE PROPERLY PACKAGED TO PREVENT ANY DAMAGE DURING SHIPMENT.
6. SOLDER PASTE MASK PER HSG DOC. NO. 030-16177.
7. THE VENT HOLE ON TOP OF RELAYS K1-4 MUST BE OPENED AFTER THE CLEANING PROCESS, BY EITHER REMOVING THE SEALING TAPE OR CUTTING OFF THE CIRCULAR TAB WITH AN "EXACTO" KNIFE OR SIMILAR CUTTING TOOL. WARNING: THIS STEP MUST BE DONE AFTER THE CLEANING PROCESS, NOT BEFORE. WATER OR CLEANING SOLVENTS ENTERING THE RELAY VENT HOLE WILL DAMAGE THE RELAY.

CROWN DOCUMENT INFORMATION:

WAS CROWN PART NUMBER: 135264-3
FOR SCHEMATIC SEE: 060-16169

UNCONTROLLED
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DISTRIBUTION	DWN	MES	6-26-03
	CM		
FILENAME: 080-16168_2.TIF	PE	MES	6-26-03
TOLERANCE UNLESS OTHERWISE SPECIFIED: .00 = ±.02" .000 = ±.010" DRILLS = ±.003"			
DO NOT SCALE DRAWING			

CROWN INTERNATIONAL, INC.
1718 W. MISHAWAKA RD.
ELKHART IN, 46517
PHONE 574-294-8000
www.CROWNINTL.COM

TITLE: PC, ASSY DWG, AMP MOD, 4CH, RV8

SIZE	DWG NO.	REV
C	080-16168	2

SCALE NONE | PROJ NO. MD508D0 | SHEET 1 OF 1

REVISION HISTORY							
E.C.N.	ZONE	REV	DESCRIPTION	DATE	APPROVED		
					DWN	CM	PE
		1	INITIAL RELEASE	4-21-03	MES		MES
		2	ADD S/N LABEL & NOTES PER ECO 040409-00	4-23-04	MES		MES

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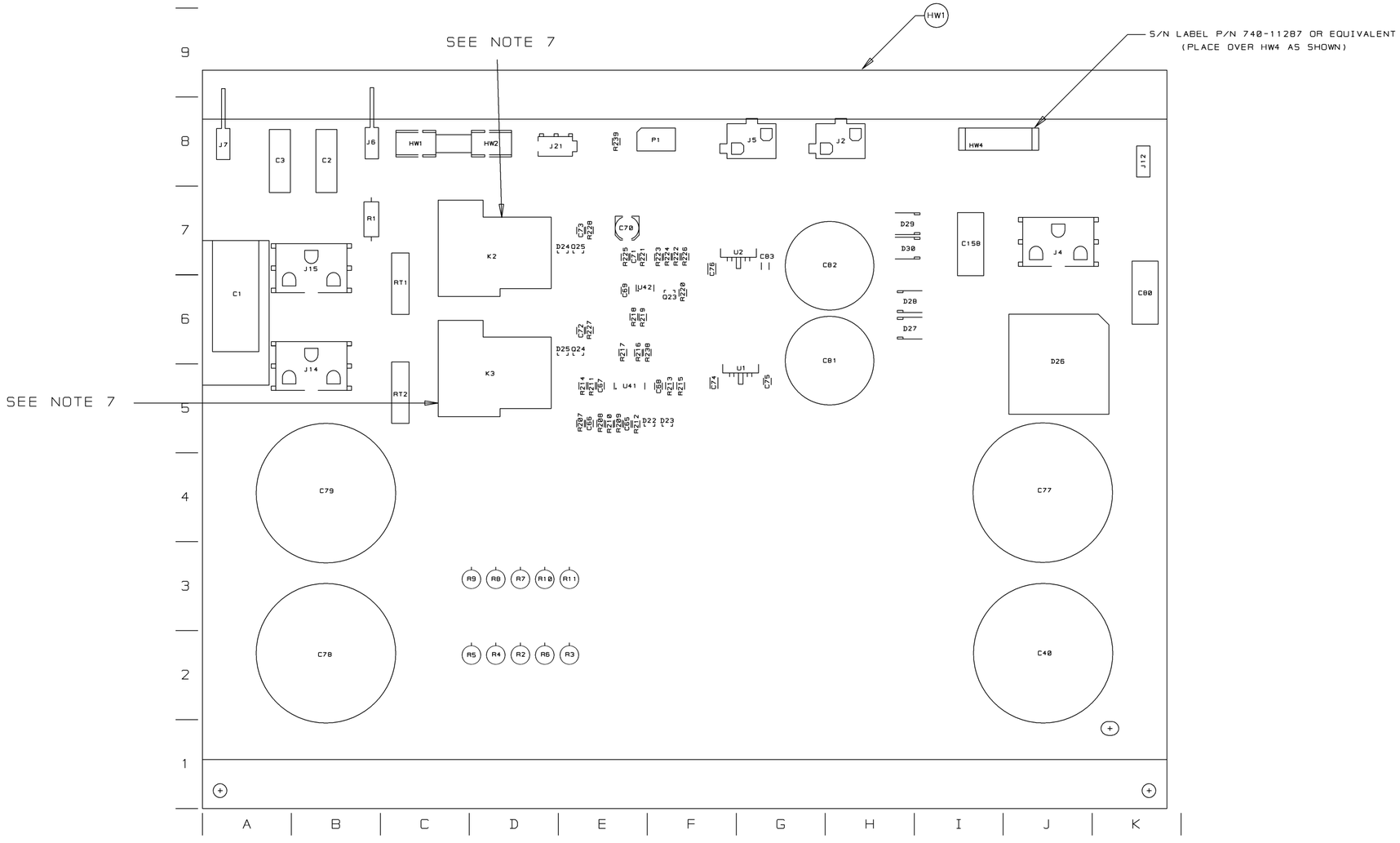
COMPONENT MAP
TOP SIDE



NOTES:
1. HSG BOM NUMBER 023-15826 SUPERSEDES ANY INFORMATION ON THIS DRAWING.
2. COMPONENTS TO BE INSTALLED ON TOP SIDE OF PCB, UNLESS OTHERWISE NOTED BY AN ASTERISK (*).
3. ALL LEADS TO BE TRIMMED TO 0.093" OR LESS.
4. UNLESS OTHERWISE SPECIFIED, MOUNT ALL COMPONENTS FLUSH AND PERPENDICULAR (90 DEG +/- 1 DEG) TO PCB.
5. PCB ASSEMBLY TO BE PACKAGED IN A STATIC-SHIELDING (FARADAY CAGE) BAG THAT HAS AN ANTI-STATIC (NON-CONDUCTIVE) INNER LAYER. THE ASSEMBLY IS TO BE PROPERLY PACKAGED TO PREVENT ANY DAMAGE DURING SHIPMENT.
6. SOLDER PASTE MASK PER HSG DOC. NO. 030-16177.
7. THE VENT HOLE ON TOP OF RELAYS K2-3 MUST BE OPENED AFTER THE CLEANING PROCESS, BY EITHER REMOVING THE SEALING TAPE OR CUTTING OFF THE CIRCULAR TAB WITH AN "EXACTO" KNIFE OR SIMILAR CUTTING TOOL. WARNING: THIS STEP MUST BE DONE AFTER THE CLEANING PROCESS, NOT BEFORE. WATER OR CLEANING SOLVENTS ENTERING THE RELAY VENT HOLE WILL DAMAGE THE RELAY.

CROWN DOCUMENT INFORMATION:

WAS CROWN PART NUMBER: 135263-3
FOR SCHEMATIC SEE: 060-16179

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DISTRIBUTION	DWN	MES	4-21-03
	CM		
FILENAME: 080-16178_2.TIF	PE	MES	4-21-03
TOLERANCE UNLESS OTHERWISE SPECIFIED: .00 = ±.02", .000 = ±.010", DRILLS = ±.003"			
DO NOT SCALE DRAWING			

CROWN INTERNATIONAL, INC.
1718 W. MISHAWAKA RD.
ELKHART IN, 46517
PHONE(219)294-8000
WWW.CROWNINTL.COM

TITLE: PC, ASSY DWG, PS BD, RV8

SIZE	DWG NO.	REV
C	080-16178	2

SCALE NONE | PROJ NO. MD508D0 | SHEET 1 OF 1

REV	DESCRIPTION	DRAFTER / CHECKER	Q.C. / AUTHOR.

NOTES

1. LEXICON BOM NUMBER 023-15890 SUPERSEDES ANY INFORMATION ON THIS DRAWING.
2. ALL COMPONENTS TO BE INSTALLED FROM TOP SIDE OF PCB.
3. UNLESS OTHERWISE SPECIFIED, MOUNT ALL COMPONENTS FLUSH AND PERPENDICULAR (90^{O} +/- 1^{O}) TO PCB.
4. PCB ASSEMBLY TO BE PACKAGED IN A STATIC-SHIELDING (FARADAY CAGE) BAG THAT HAS AN ANTI-STATIC (NON-CONDUCTIVE) INNER LAYER. THE ASSEMBLY IS TO BE PROPERLY PACKAGED TO PREVENT ANY DAMAGE DURING SHIPMENT.
5. SOLDER PASTE MASK PER LEXICON DOC. NO. 030-16187
6. BREAK PCB AND CUT EXCESS FLUSH WITH EDGES. THROW OUT BLANK PCB MATERIAL.

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UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN MM.
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.X +/-.2
.XX +/- .1

			APPROVALS	DATE
	710-16180	MATERIAL	DRAWN RWH	5/1/03
NEXT ASSY.	USED ON	FINISH	CHECKED CLC	5/6/03
APPLICATION		DO NO SCALE DRAWING	Q.C. CW	5/8/03
			ISSUED MAG	5/8/03

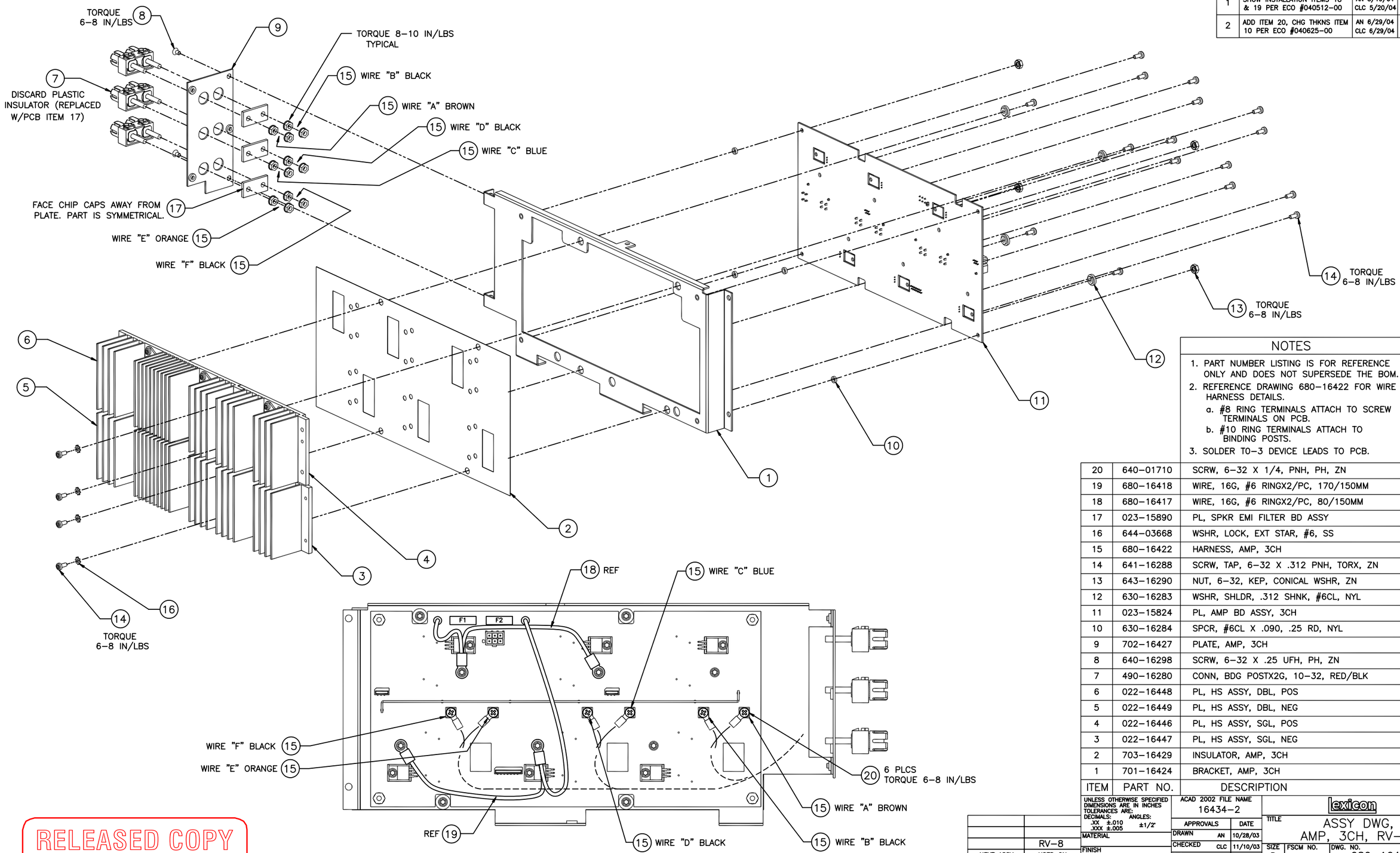
lexicon

PC BD, SPKR EMI FILT, RV8
ASSEMBLY DRAWING

SIZE	FSCM NO.	DWG. NO.	REV
A3		080-16188	0

SCALE 1:1 SHEET 1 OF 1

REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
1	SHOW INSTALLATION ITEMS 18 & 19 PER ECO #040512-00	AN 5/19/04 CLC 5/20/04	CW 5/20/04 KB 5/20/04
2	ADD ITEM 20, CHG THKNS ITEM 10 PER ECO #040625-00	AN 6/29/04 CLC 6/29/04	CW 6/30/04 MAG 6/30/04



NOTES

1. PART NUMBER LISTING IS FOR REFERENCE ONLY AND DOES NOT SUPERSEDE THE BOM.
2. REFERENCE DRAWING 680-16422 FOR WIRE HARNESS DETAILS.
   a. #8 RING TERMINALS ATTACH TO SCREW TERMINALS ON PCB.
   b. #10 RING TERMINALS ATTACH TO BINDING POSTS.
3. SOLDER TO-3 DEVICE LEADS TO PCB.

ITEM	PART NO.	DESCRIPTION	QTY
20	640-01710	SCRW, 6-32 X 1/4, PNH, PH, ZN	6
19	680-16418	WIRE, 16G, #6 RINGX2/PC, 170/150MM	REF
18	680-16417	WIRE, 16G, #6 RINGX2/PC, 80/150MM	REF
17	023-15890	PL, SPKR EMI FILTER BD ASSY	3
16	644-03668	WSHR, LOCK, EXT STAR, #6, SS	4
15	680-16422	HARNESS, AMP, 3CH	1
14	641-16288	SCRW, TAP, 6-32 X .312 PNH, TORX, ZN	20
13	643-16290	NUT, 6-32, KEP, CONICAL WSHR, ZN	4
12	630-16283	WSHR, SHLDR, .312 SHNK, #6CL, NYL	4
11	023-15824	PL, AMP BD ASSY, 3CH	1
10	630-16284	SPCR, #6CL X .090, .25 RD, NYL	4
9	702-16427	PLATE, AMP, 3CH	1
8	640-16298	SCRW, 6-32 X .25 UFH, PH, ZN	2
7	490-16280	CONN, BDG POSTX2G, 10-32, RED/BLK	3
6	022-16448	PL, HS ASSY, DBL, POS	1
5	022-16449	PL, HS ASSY, DBL, NEG	1
4	022-16446	PL, HS ASSY, SGL, POS	1
3	022-16447	PL, HS ASSY, SGL, NEG	1
2	703-16429	INSULATOR, AMP, 3CH	1
1	701-16424	BRACKET, AMP, 3CH	1

NEXT ASSY	RV-8
APPLICATION	USED ON

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS: .XX ±.010 .XXX ±.005 ANGLES: ±1/2°
MATERIAL
FINISH
DO NOT SCALE DRAWING

ACAD 2002 FILE NAME 16434-2

APPROVALS		DATE
DRAWN	AN	10/28/03
CHECKED	CLC	11/10/03
Q.C.	CW	11/24/03
ISSUED	MAG	11/24/03

lexicon

TITLE: ASSY DWG, AMP, 3CH, RV-8

SIZE D | FSCM NO. | DWG. NO. 080-16434 | REV. 2

SCALE N/A | SHEET 1 OF 1

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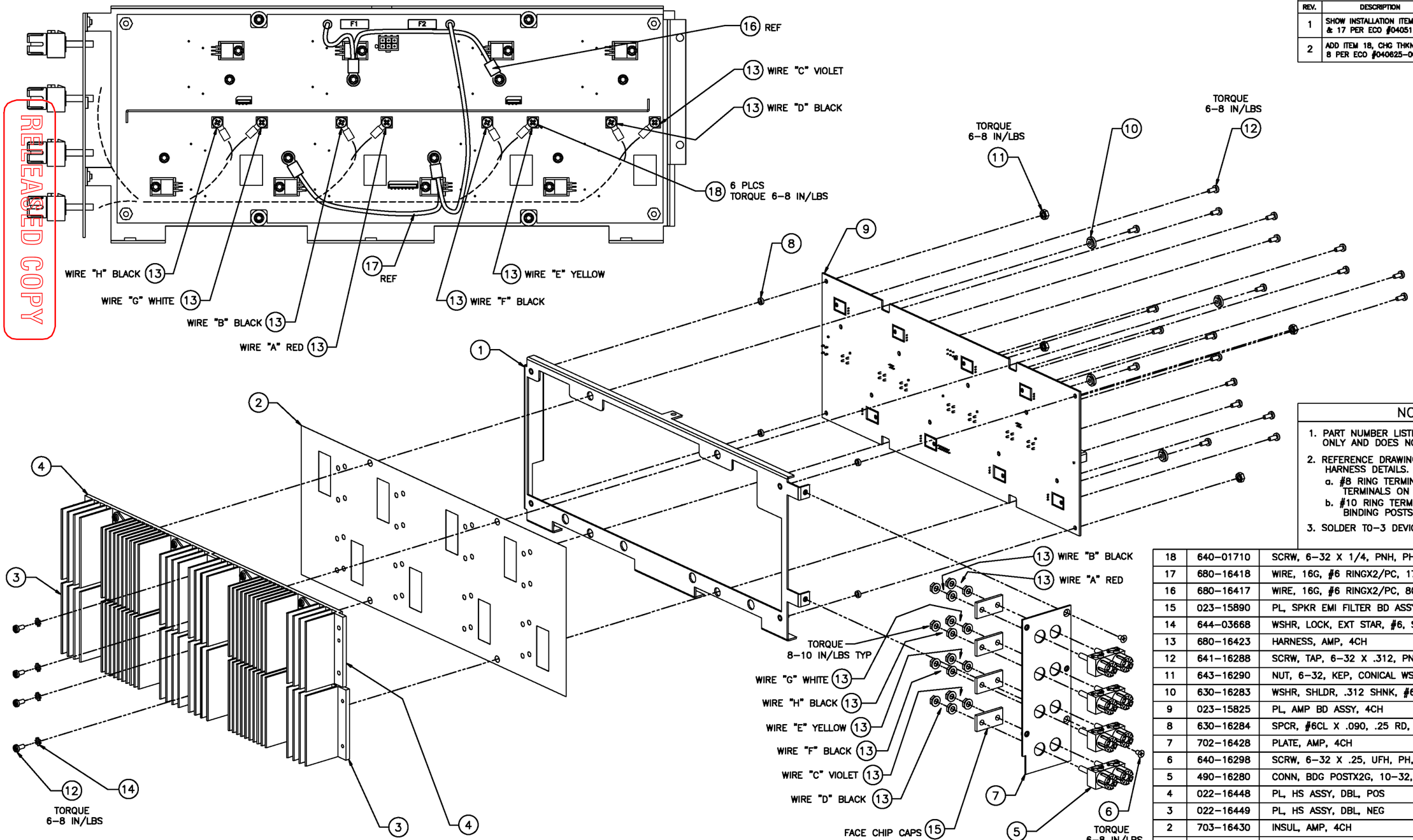
JUL 09 2004

REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
1	SHOW INSTALLATION ITEMS 16 & 17 PER ECO #040512-00	AN 5/19/04 CLC 5/20/04	CW 5/20/04 KB 5/20/04
2	ADD ITEM 18, CHG THKNS ITEM 8 PER ECO #040625-00	AN 6/29/04 CLC 6/29/04	CW 6/30/04 MAG 6/30/04



NOTES

1. PART NUMBER LISTING IS FOR REFERENCE ONLY AND DOES NOT SUPERSEDE THE BOM.
2. REFERENCE DRAWING 680-16423 FOR WIRE HARNESS DETAILS.
   a. #8 RING TERMINALS ATTACH TO SCREW TERMINALS ON PCB.
   b. #10 RING TERMINALS ATTACH TO BINDING POSTS.
3. SOLDER TO-3 DEVICE LEADS TO PCB.

ITEM	PART NO.	DESCRIPTION	QTY
18	640-01710	SCRW, 6-32 X 1/4, PNH, PH, ZN	8
17	680-16418	WIRE, 16G, #6 RINGX2/PC, 170/150MM	REF
16	680-16417	WIRE, 16G, #6 RINGX2/PC, 80/150MM	REF
15	023-15890	PL, SPKR EMI FILTER BD ASSY	4
14	644-03668	WSHR, LOCK, EXT STAR, #6, SS	4
13	680-16423	HARNESS, AMP, 4CH	1
12	641-16288	SCRW, TAP, 6-32 X .312, PNH, TORX, ZN	24
11	643-16290	NUT, 6-32, KEP, CONICAL WSHR, ZN	4
10	630-16283	WSHR, SHLDR, .312 SHNK, #6CL, NYL	4
9	023-15825	PL, AMP BD ASSY, 4CH	1
8	630-16284	SPCR, #6CL X .090, .25 RD, NYL	4
7	702-16428	PLATE, AMP, 4CH	1
6	640-16298	SCRW, 6-32 X .25, UFH, PH, ZN	2
5	490-16280	CONN, BDG POSTX2G, 10-32, RED/BLK	4
4	022-16448	PL, HS ASSY, DBL, POS	2
3	022-16449	PL, HS ASSY, DBL, NEG	2
2	703-16430	INSUL, AMP, 4CH	1
1	701-16425	BRACKET, AMP, 4CH	1

NEXT ASSY	RV-8
APPLICATION	USED ON

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS: .XX ±.010 .XXX ±.005
ANGLES: ±1/2°
MATERIAL
FINISH
DO NOT SCALE DRAWING

ACAD 2002 FILE NAME: 16435-2

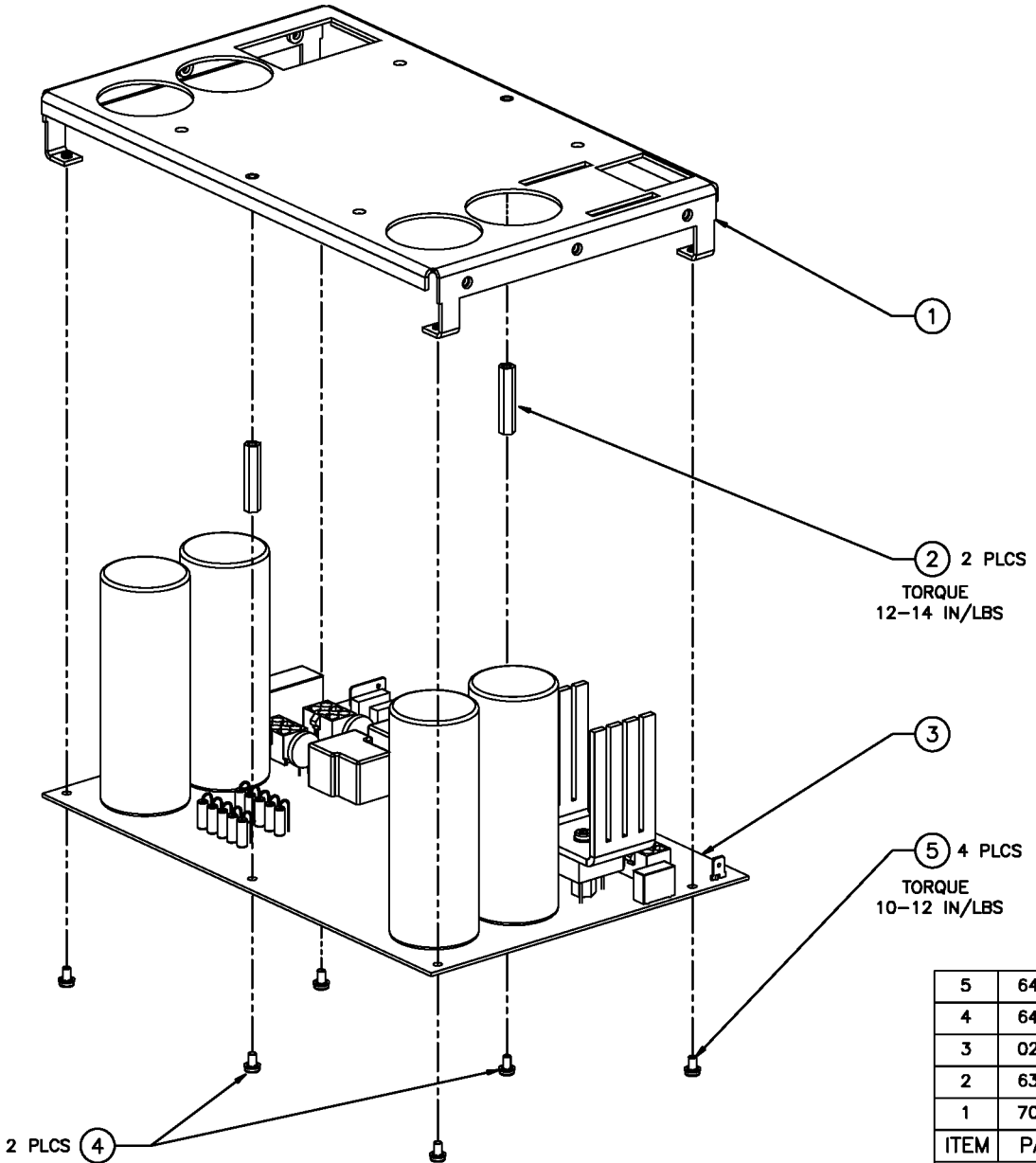
APPROVALS		DATE
DRAWN	AN	10/28/03
CHECKED	CLC	11/10/03
Q.C.	CW	11/24/03
ISSUED	MAG	11/24/03

lexicon

TITLE: ASSY DWG, AMP, 4CH, RV-8

SIZE	FSCM NO.	DWG. NO.	REV.
D		080-16435	2

SCALE 1/1 SHEET 1 OF 1



REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH

NOTES

1. PART NUMBER LISTING IS FOR REFERENCE ONLY AND DOES NOT SUPERSEDE THE BOM.

ITEM	PART NO.	DESCRIPTION	QTY
5	641–16299	SCRW, TAP, 6–32 X 1/4 PNH, TX, SEMS, Z	4
4	640–16291	SCRW, 6–32 X 1/4 PNH, TORX, SEMS, BZ	2
3	023–15826	PL, PS BD SUBASSY	1
2	635–16285	SPCR, 6–32 X 1.25, 1/4 HEX, ALUM	2
1	701–16426	BRACKET, TOROID/PS	1

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS: .XX ±.010 .XXX ±.005
ANGLES: ±1/2°
MATERIAL
FINISH
DO NOT SCALE DRAWING

ACAD 2002 FILE NAME: 16436–0

APPROVALS		DATE
DRAWN	AN	10/28/03
CHECKED	CLC	11/3/03
Q.C.	CW	11/18/03
ISSUED	MAG	11/24/03

lexicon

TITLE: ASSY DWG, MECH, PS, RV–8

SIZE	FSCM NO.	DWG. NO.	REV.
C		080–16436	0

SCALE 1/1 SHEET 1 OF 1

NEXT ASSY	USED ON
	RV–8

APPLICATION

DEC 05 2003

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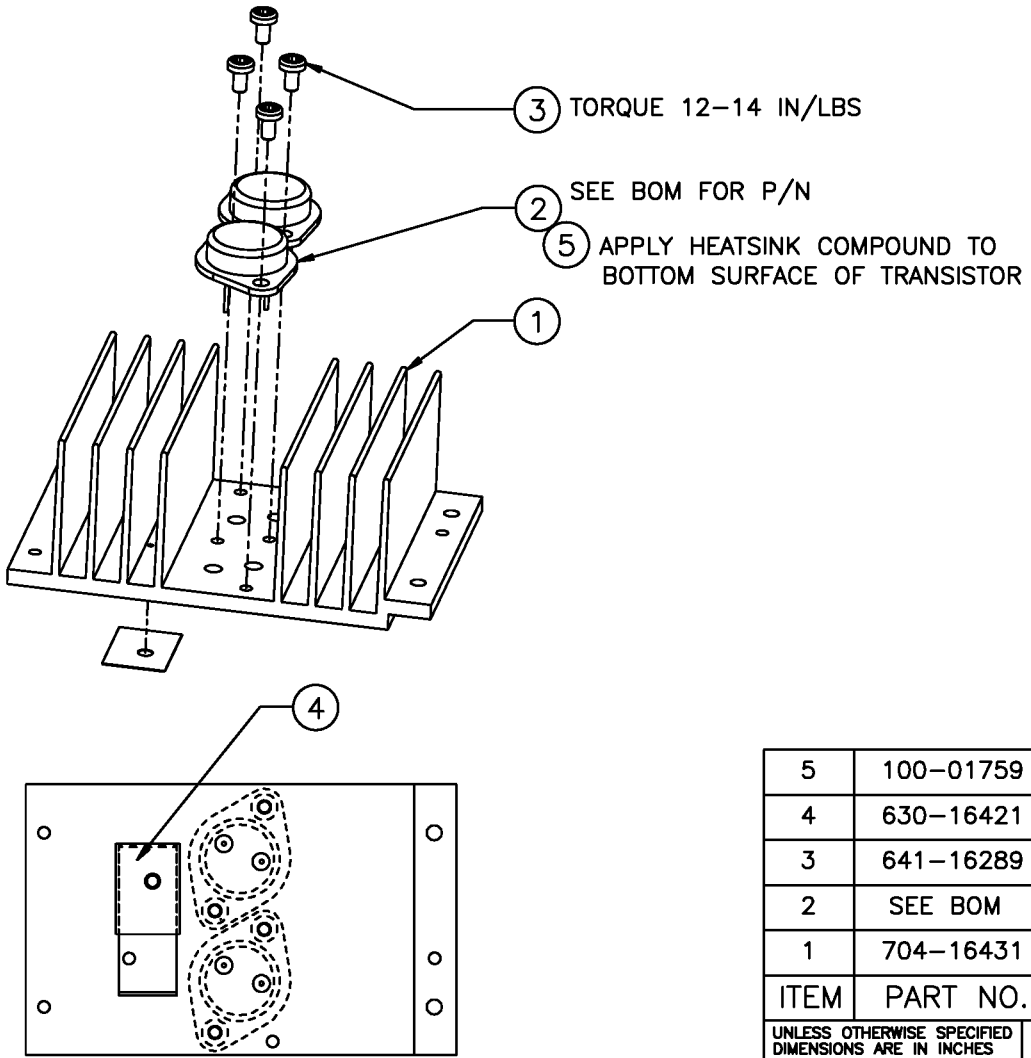

REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH

NOTES

1. PART NUMBER LISTING IS FOR REFERENCE ONLY & DOES NOT SUPERSEDE THE BOMS.

ITEM	PART NO.	DESCRIPTION	QTY
5	100–01759	HEATSINK COMPOUND	X
4	630–16421	INSUL, SIL RUB, .94 X .66	1
3	641–16289	SCRW, TAP, 6–32 X 1/4, PNH, TORX, ZN	4
2	SEE BOM	TRANSISTOR	2
1	704–16431	HEATSINK, AMP, SGL	1

NEXT ASSY	USED ON
APPLICATION	RV–8

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS: .XX ±.010 .XXX ±.005
ANGLES: ±1/2°

MATERIAL

FINISH

DO NOT SCALE DRAWING

ACAD 2002 FILE NAME
16438–0

APPROVALS		DATE
DRAWN	AN	10/28/03
CHECKED	CLC	11/10/03
Q.C.	CW	11/18/03
ISSUED	MAG	11/24/03

lexicon

TITLE
ASSY DWG,
HS, SGL, RV–8

SIZE	FSCM NO.	DWG. NO.	REV.
B		080–16438	0

SCALE 1/1 SHEET 1 OF 1

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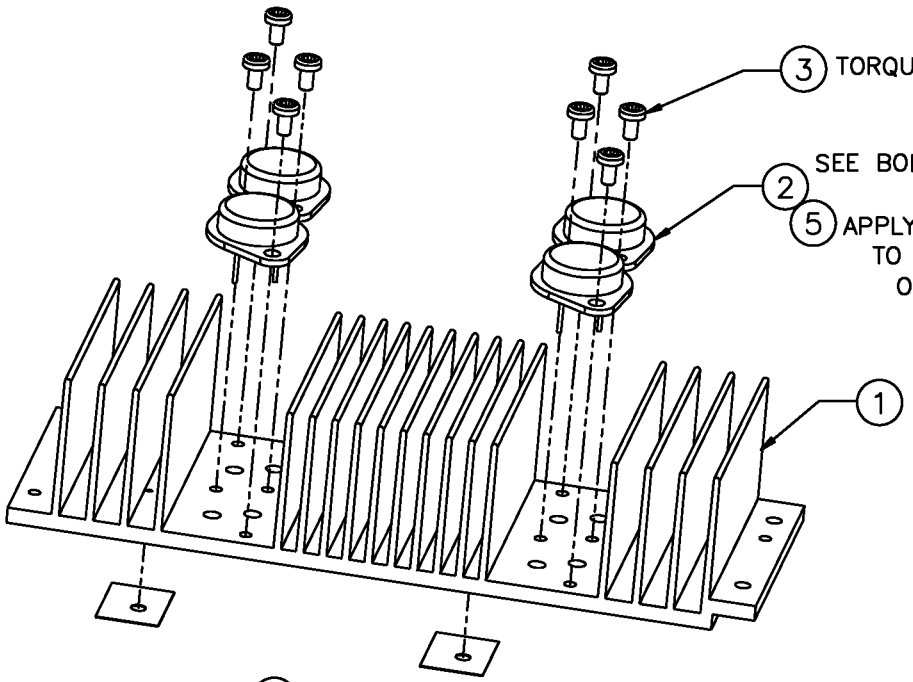
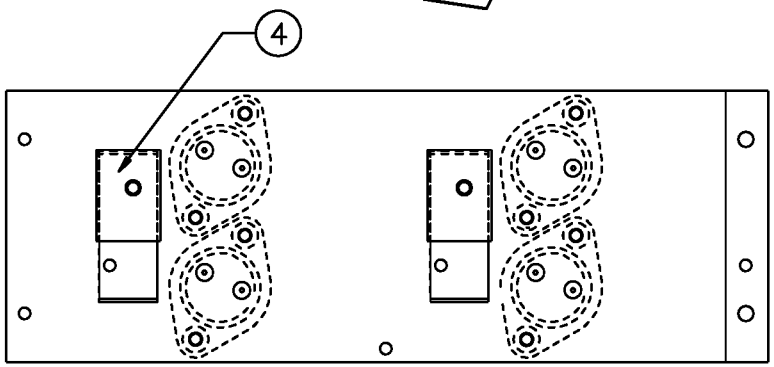
DEC 05 2003

DEC 05 2003





REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH

NOTES

1. PART NUMBER LISTING IS FOR REFERENCE ONLY & DOES NOT SUPERSEDE THE BOMS.

ITEM	PART NO.	DESCRIPTION	QTY
5	100–01759	HEATSINK COMPOUND	X
4	630–16421	INSUL, SIL RUB, .94 X .66	2
3	641–16289	SCRW, TAP, 6–32 X 1/4, PNH, TORX, ZN	8
2	SEE BOM	TRANSISTOR	2
1	704–16432	HEATSINK, AMP, DBL	1

	RV–8
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS: .XX ±.010 .XXX ±.005
ANGLES: ±1/2°

MATERIAL

FINISH

DO NOT SCALE DRAWING

ACAD 2002 FILE NAME
16439–0

APPROVALS		DATE
DRAWN	AN	10/28/03
CHECKED	CLC	11/10/03
Q.C.	CW	11/18/03
ISSUED	MAG	11/24/03

lexicon

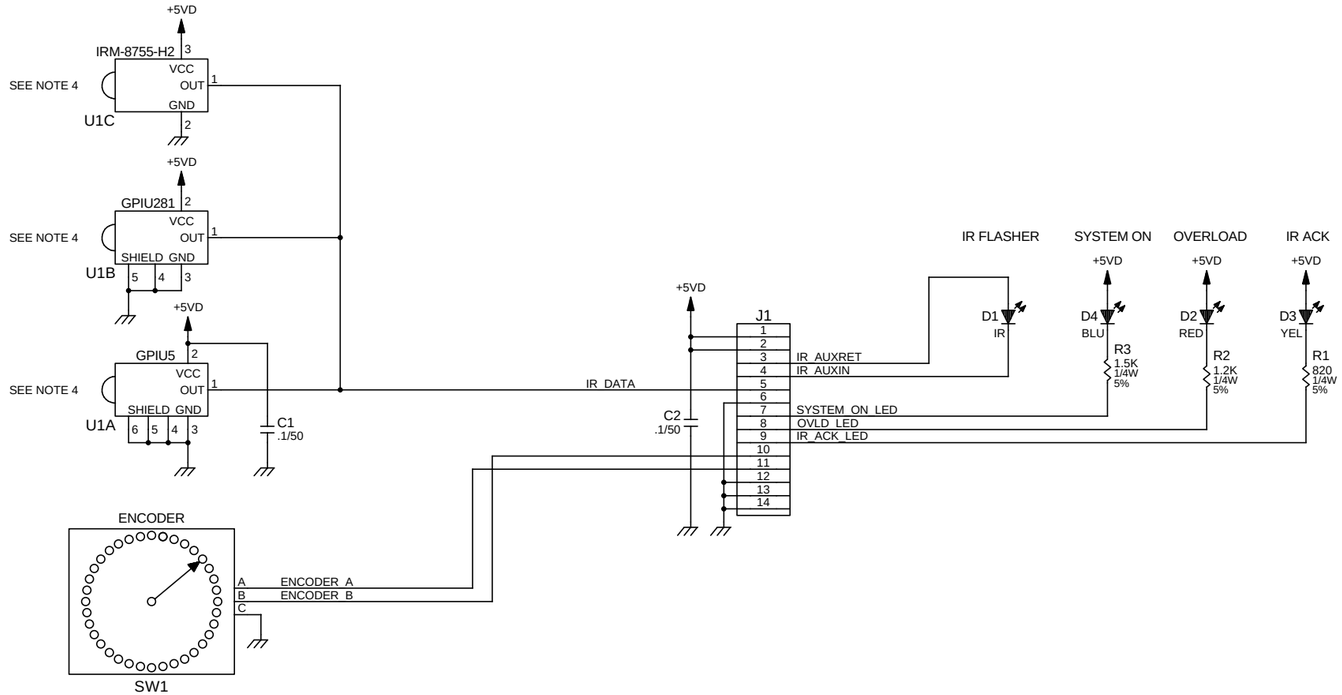
TITLE
ASSY DWG,
HS, DBL, RV–8

SIZE	FSCM NO.	DWG. NO.	REV.
B		080–16439	0

SCALE 1/1 SHEET 1 OF 1

RELEASED COPY
DEC 05 2003

DEC 05 2003



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 000327-00	RWH 3/27/00 KB 4/10/00	CW 4/28/00 KB 4/10/00
2	CHANGED PER DCR 000925-01	RWH 10/13/00 KB 10/20/00	CW 10/23/00 KB 10/20/00
3	CHANGED R3 FROM 2.4K TO 1.5K PER ECO 010130-00	CW 1/30/01 KB 1/30/01	ECM 1/30/01 KB 1/30/01

NOTES

1 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V

2 DIGITAL GROUND ANALOG GROUND CHASSIS GROUND POWER GROUND

3 LAST REFERENCE DESIGNATORS USED: C2, D4, J1, R3, SW1, U1

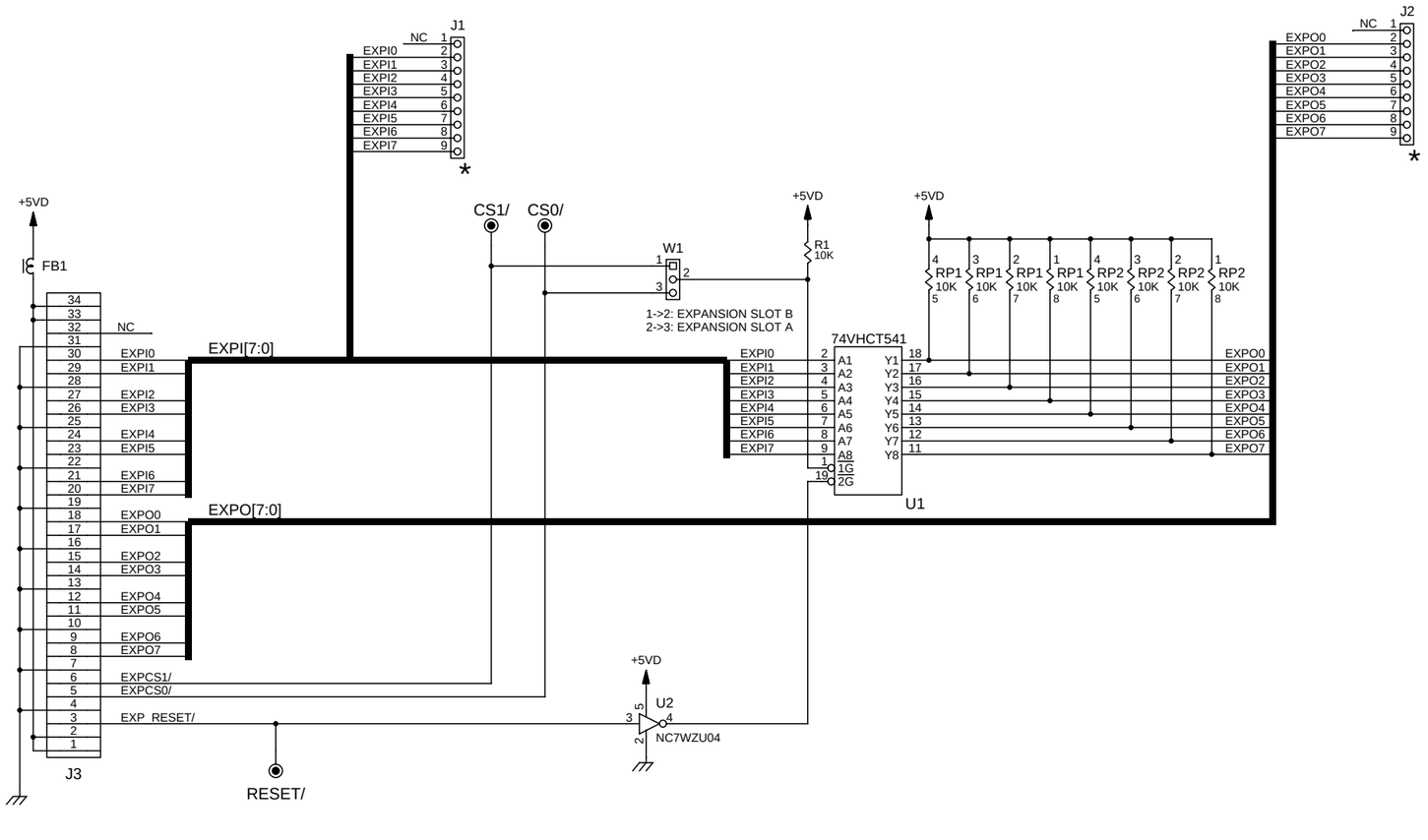
4 INSTALL ONE ONLY OF U1A, B, C.

REFERENCE COPY

CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS	DATE	TITLE	
DRAWN CW	10/27/99	SCHEM,IR/ENC BD,MC12	
CHECKED KB	10/27/99	SIZE B / CODE / NUMBER 060-13699 / REV 3	
Q.C. RWH	10/27/99	FILE NAME 13699-3.1	SHEET 1 OF 1
ISSUED KB	10/27/99		

1-30-2001_15:17

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020913-00	RWH 11/05/02	CW 12/20/02
		CAM 11/06/02	MAG 12/20/02
2	CHANGED PER DCR 030307-00	RWH 4/29/03	CW 4/29/03
		CAM 4/29/03	KAB 5/2/03



NOTES

1 UNLESS OTHERWISE INDICATED, RESISTORS ARE 1/10W

2 UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%

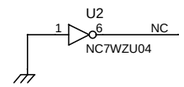
3 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V

4 DIGITAL GROUND ANALOG GROUND CHASSIS GROUND POWER GROUND

5 LAST REFERENCE DESIGNATORS USED: C2, FB1, J3, R1, RP2, U2, W1

6 COMPONENTS MARKED WITH * ARE NOT ON BOM.

SPARE



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CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	4/29/03
CHECKED	CAM	4/29/03
Q.C.	CW	4/29/03
ISSUED	KAB	5/2/03

TITLE: SCHEM, EXP TEST BD, RV8

SIZE	CODE	NUMBER	REV
B		060-15379	0

FILE NAME: 15379-0. 1 SHEET 1 OF 1

REFERENCE COPY

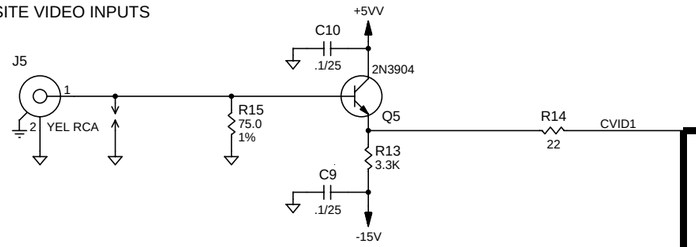
= 1.3mS

5-5-2003_15:43

COMPOSITE VIDEO INPUTS

CVID

1



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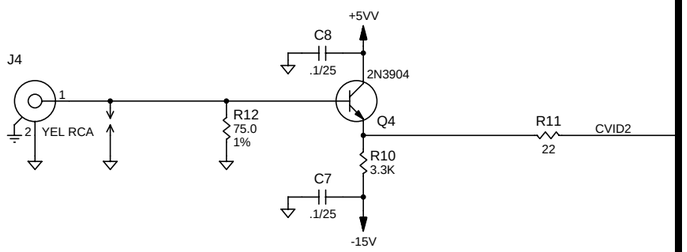

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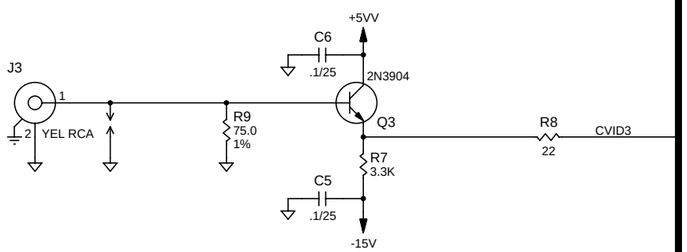

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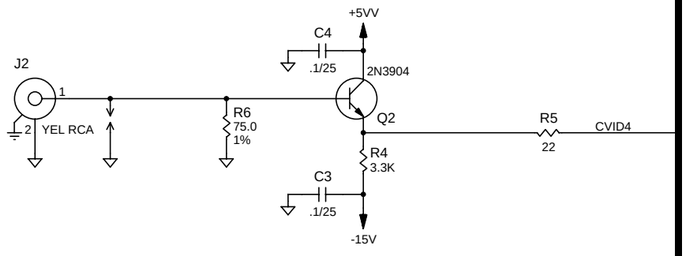

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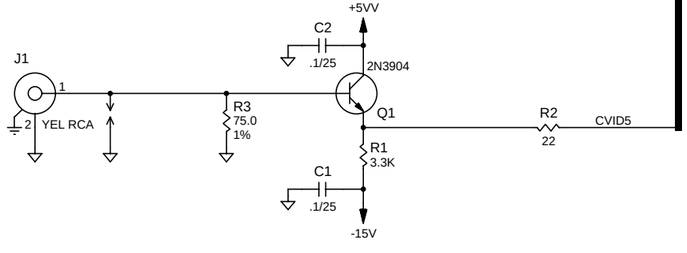
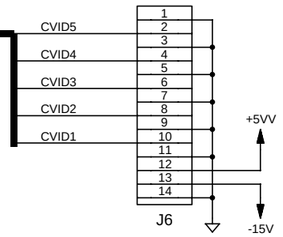
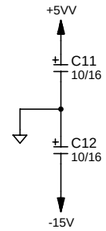


CVID[5:1]

VIDEO BOARD CONNECTOR





REVISIONS

REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.

NOTES

1 UNLESS OTHERWISE INDICATED, RESISTORS ARE 1/10W

2 UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%

3 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V

4 DIGITAL GROUND ANALOG GROUND CHASSIS GROUND POWER GROUND

5 LAST REFERENCE DESIGNATORS USED: C12, J6, Q5, R15

REFERENCE COPY

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CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730

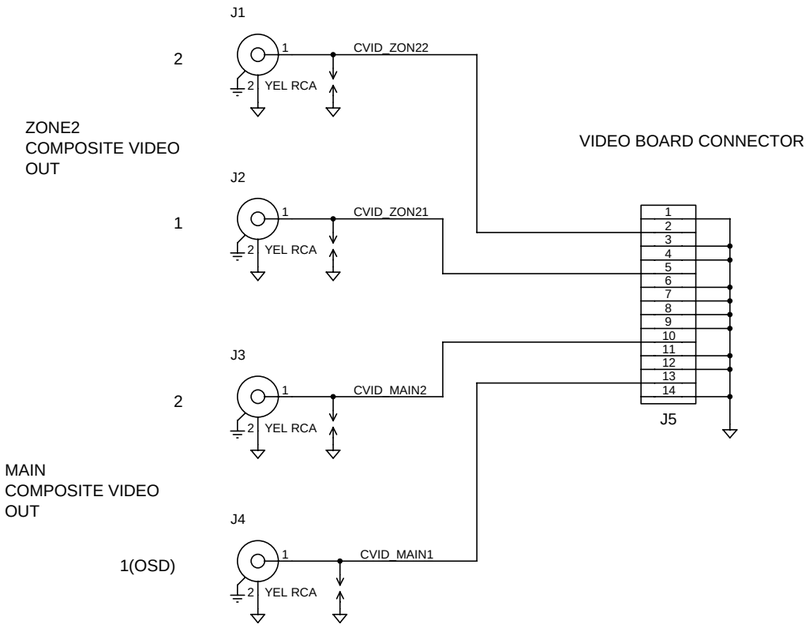
APPROVALS		DATE
DRAWN	CW	8/7/02
CHECKED	ECM	8/13/02
Q.C.	RWH	8/14/02
ISSUED	MAG	8/15/02

TITLE: SCHEM,VIDEO IN BD,RV8 RCA INPUTS

SIZE	CODE	NUMBER	REV
B		060-15509	0

FILE NAME: 15509-0 .1 SHEET 1 OF 1

9-3-2002_11:12



REVISIONS

REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.

NOTES

1 LAST REFERENCE DESIGNATORS USED: J5

REFERENCE COPY

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CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730

APPROVALS	DATE
DRAWN CW	8/7/02
CHECKED ECM	8/13/02
Q.C. RWH	8/14/02
ISSUED MAG	8/15/02

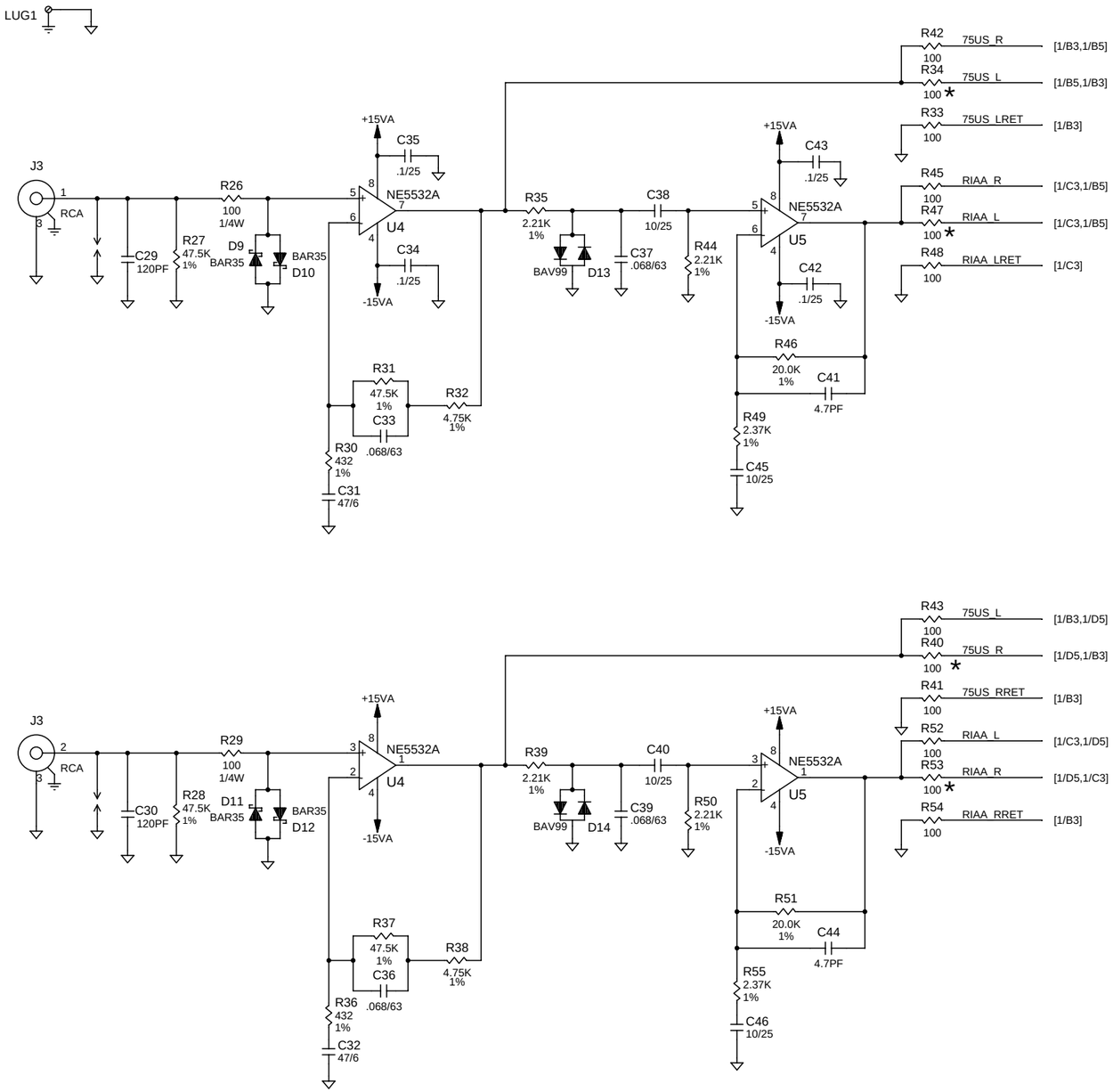
TITLE: SCHEM,VIDEO OUT BD,RV8 RCA OUTPUTS

SIZE	CODE	NUMBER	REV
B		060-15519	0

FILE NAME: 15519-0 . 1

SHEET 1 OF 1

9-3-2002_11:25



REVISIONS

REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 021030-00	CW 11/20/02	RWH 11/26/02
		CBV 11/20/02	MAG 11/26/02
2	CHANGED PER DCR 030317-00	RWH 5/21/03	CW 5/22/03
		CBV 5/22/03	MAG 5/22/03

NOTES

1 UNLESS OTHERWISE INDICATED, RESISTORS ARE 1/10W

2 UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%

3 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V

4 DIGITAL GROUND, ANALOG GROUND, CHASSIS GROUND, POWER GROUND

5 [XX/XX] DENOTES [SHEET NUMBER/SECTOR]

6 LAST REFERENCE DESIGNATORS USED: C46, D14, FB8, J4, LUG1, R55, U5.

7 COMPONENTS MARKED WITH * ARE NOT ON BOM. INSTALLED ONLY FOR WHITE OVER RED RCA CONNECTOR.

DOCUMENT CONTROL BLOCK: #060-15529

SHEET	REVISION	TITLE
1 OF 2	2	PHONO PREAMP
2 OF 2	2	MIC INPUTS

REFERENCE COPY

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CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	8/15/02
CHECKED	CBV	8/15/02
Q.C.	CW	8/26/02
ISSUED	MAG	8/16/02

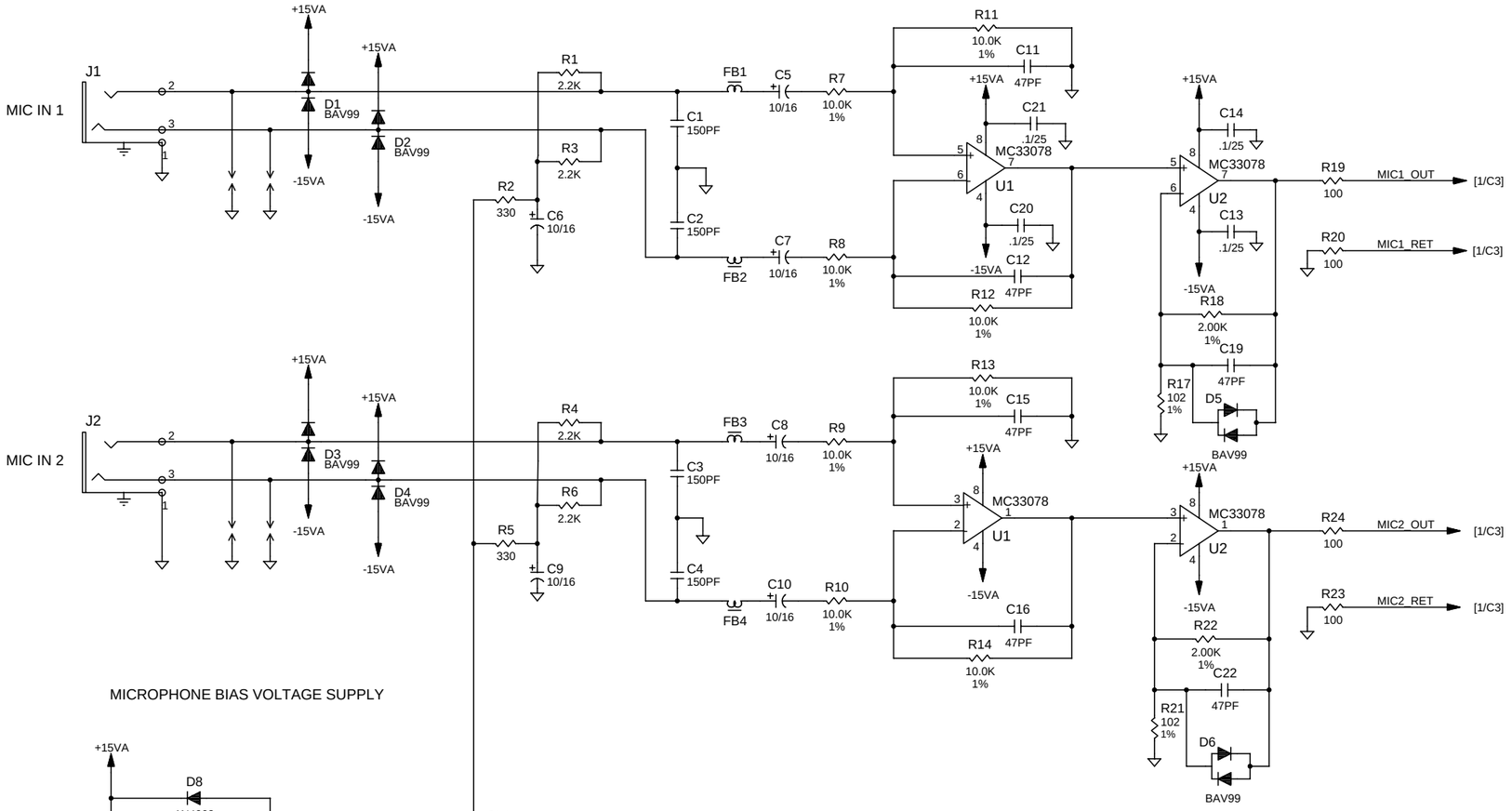
TITLE: SCHEM, MIC/PREAMP BD,RV8 PHONO PREAMP

SIZE	CODE	NUMBER	REV
B		060-15529	2

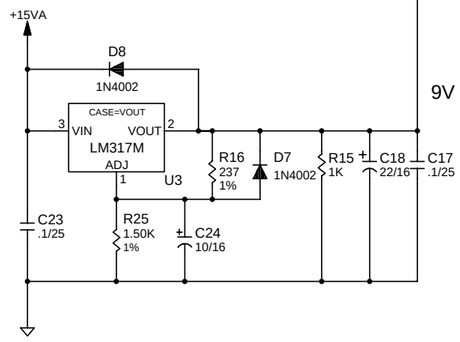
FILE NAME: 15529-2. 1 SHEET 1 OF 2

5-23-2003_9:15

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 021030-00	CW 11/27/02	RWH 11/26/02
		CBV 11/20/02	MAG 11/26/02
2	CHANGED PER DCR 030317-00	RWH 5/21/03	CW 5/22/03
		CBV 5/22/03	MAG 5/22/03



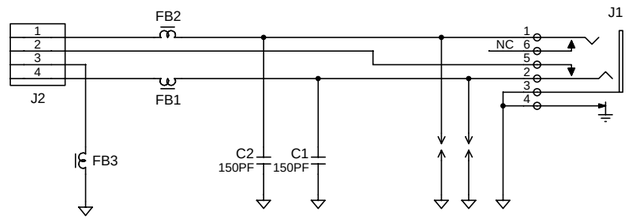
MICROPHONE BIAS VOLTAGE SUPPLY



CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS	DATE	TITLE: SCHEM, MIC/PREAMP BD,RV8 MIC INPUTS	
DRAWN RWH	8/15/02		
CHECKED CBV	8/15/02	SIZE B / CODE / NUMBER 060-15529 / REV 2	
Q.C. CW	8/26/02		
ISSUED MAG	8/16/02	FILE NAME 15529-2. 2 / SHEET 2 OF 2	

5-23-2003 9:16

HEADPHONE OUTPUT



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 021029-00	CW 11/4/02	RWH 11/14/02
		CBV 11/12/02	MAG 11/14/02
2	CHANGED PER DCR 030515-00	RWH 5/22/03	CW 5/23/03
		ECM 5/22/03	MAG 5/23/03

NOTES

1 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V

2 DIGITAL GROUND ANALOG GROUND CHASSIS GROUND POWER GROUND

3 LAST REFERENCE DESIGNATORS USED: C2, FB3, J2

4 COMPONENTS MARKED WITH * ARE NOT ON BOM.

REFERENCE COPY

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CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	CW	8/26/02
CHECKED	CBV	8/26/02
Q.C.	RWH	8/27/02
ISSUED	MAG	8/27/02

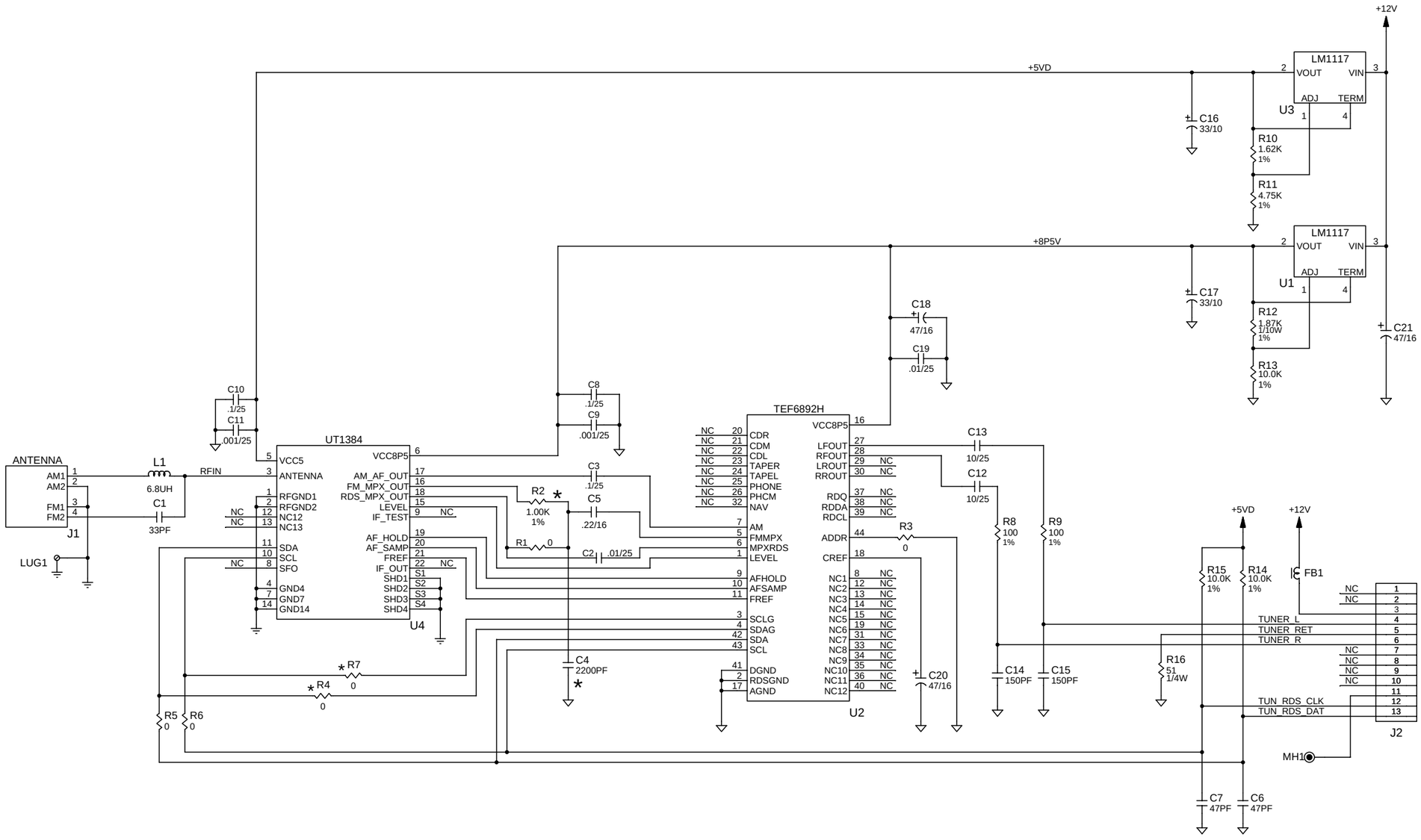
TITLE: SCHEM,HEADPHONE BD,RV8

SIZE	CODE	NUMBER	REV
B		060-15539	2

FILE NAME: 15539-2.1 SHEET 1 OF 1

6-3-2003_12:14

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCRS 030314-00 & 030410-00.	RWH 4/15/03	CW 4/15/03
		CAM 4/15/03	KAB 4/29/03



NOTES

1 UNLESS OTHERWISE INDICATED, RESISTORS ARE 1/10W

2 UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%

3 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V

4 DIGITAL GROUND, ANALOG GROUND, CHASSIS GROUND, POWER GROUND

5 LAST REFERENCE DESIGNATORS USED: C21, FB1, J2, L1, R16, U4.

6 COMPONENTS MARKED WITH * ARE NOT ON BOM.

REFERENCE COPY

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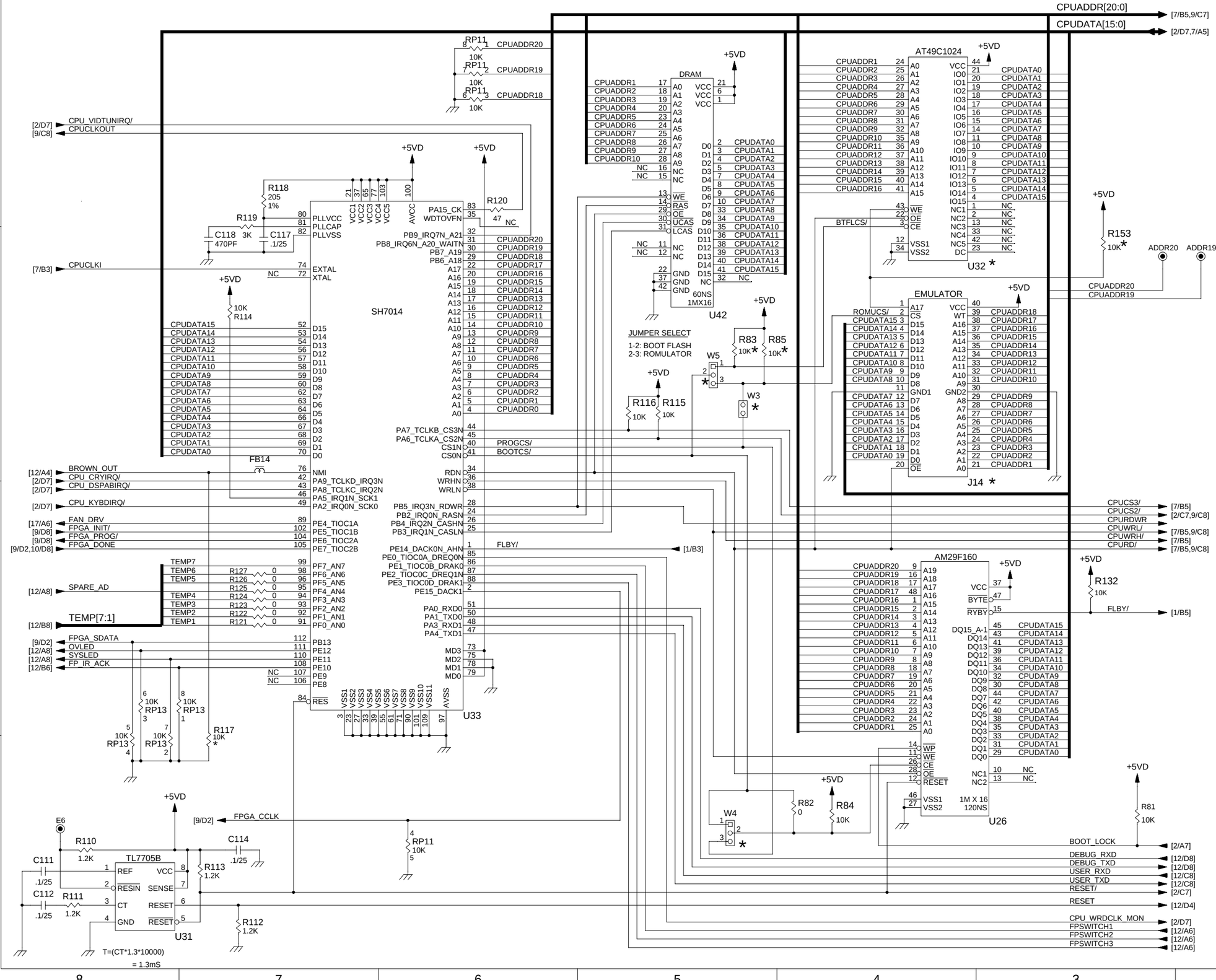
CONTRACT NO.	Lexicon 3 OAK PARK BEDFORD, MA 01730		
APPROVALS		DATE	TITLE: SCHEM, TUNER BD, RV8
DRAWN	RWH	12/3/02	
CHECKED	CAM	12/4/02	SIZE B / CODE / NUMBER 060-15549 / REV 1
Q.C.	CW	12/9/02	
ISSUED	MAG	12/9/02	FILE NAME 15549-1. 1 / SHEET 1 OF 1

5-12-2003_14:46



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020913-00	RWH 11/05/02	CW 12/20/02
		CAM 11/06/02	MAG 12/20/02
2	CHANGED PER DCR 030307-00	RWH 5/2/03	CW 5/20/03
		CAM 5/14/03	MAG 5/20/03
3	CHANGED SHT. 12 PER DCR 030307-00-A	RWH 5/22/03	CW 5/22/03
		CAM 5/22/03	MAG 5/22/03
4	CHANGED PER DCR 030626-00	RWH 9/29/03	ECM 10/9/03
		CAM 10/2/03	MAG 10/9/03
5	CHANGED SHTS 1,3,12 PER DCR 031124-00	RWH 12/2/03	CW 12/30/03
		CAM 12/8/03	MAG 12/30/03
6	CHANGED SHTS 7 & 19 PER ECO 040422-00	RWH 4/27/04	CW 4/29/04
		CAM 4/29/04	KAB 5/2/04

NOTES

1 UNLESS OTHERWISE INDICATED, RESISTORS ARE 1/10W

2 UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%

3 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V

4 DIGITAL GROUND, ANALOG GROUND, CHASSIS GROUND, POWER GROUND

5 [XX/XX] DENOTES [SHEET NUMBER/SECTOR]

6 LAST REFERENCE DESIGNATORS USED: C178, CP5, D49, FB18, J32, L3, Q2, R188, RP37, U48, W10, Y2.

7 COMPONENTS MARKED WITH * ARE NOT ON BOM.

DOCUMENT CONTROL BLOCK: #060-15559

SHEET	REVISION	TITLE
1 OF 19	6	HOST PROCESSOR
2 OF 19	3	BUFFERS, LEVEL SHIFTERS
3 OF 19	4	DSP HOST 1 AND 2
4 OF 19	3	DSP A SDRAM AND FLASH
5 OF 19	3	DSP B EXTERNAL MEMORY
6 OF 19	3	DSP SPI, SERIAL, AND LINK PORTS
7 OF 19	4	DSP/FPGA POWER CONN.
8 OF 19	3	CRYSTAL DSP
9 OF 19	3	MAIN FPGA
10 OF 19	3	FPGA FLASH
11 OF 19	3	EXPANSION PORT SERIES TERMINATIONS
12 OF 19	5	BOARD INTERCONN/DEBUG
13 OF 19	3	SPDIF I/O
14 OF 19	3	TRIGGER OUTPUTS
15 OF 19	3	VCO A
16 OF 19	3	VCO B
17 OF 19	3	POWER SUPPLY
18 OF 19	3	IR REMOTE CONNECTOR
19 OF 19	4	BYPASS CAPACITORS

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CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	4/26/02
CHECKED	CAM	4/30/02
Q.C.	CW	5/1/02
ISSUED	JV	4/30/02

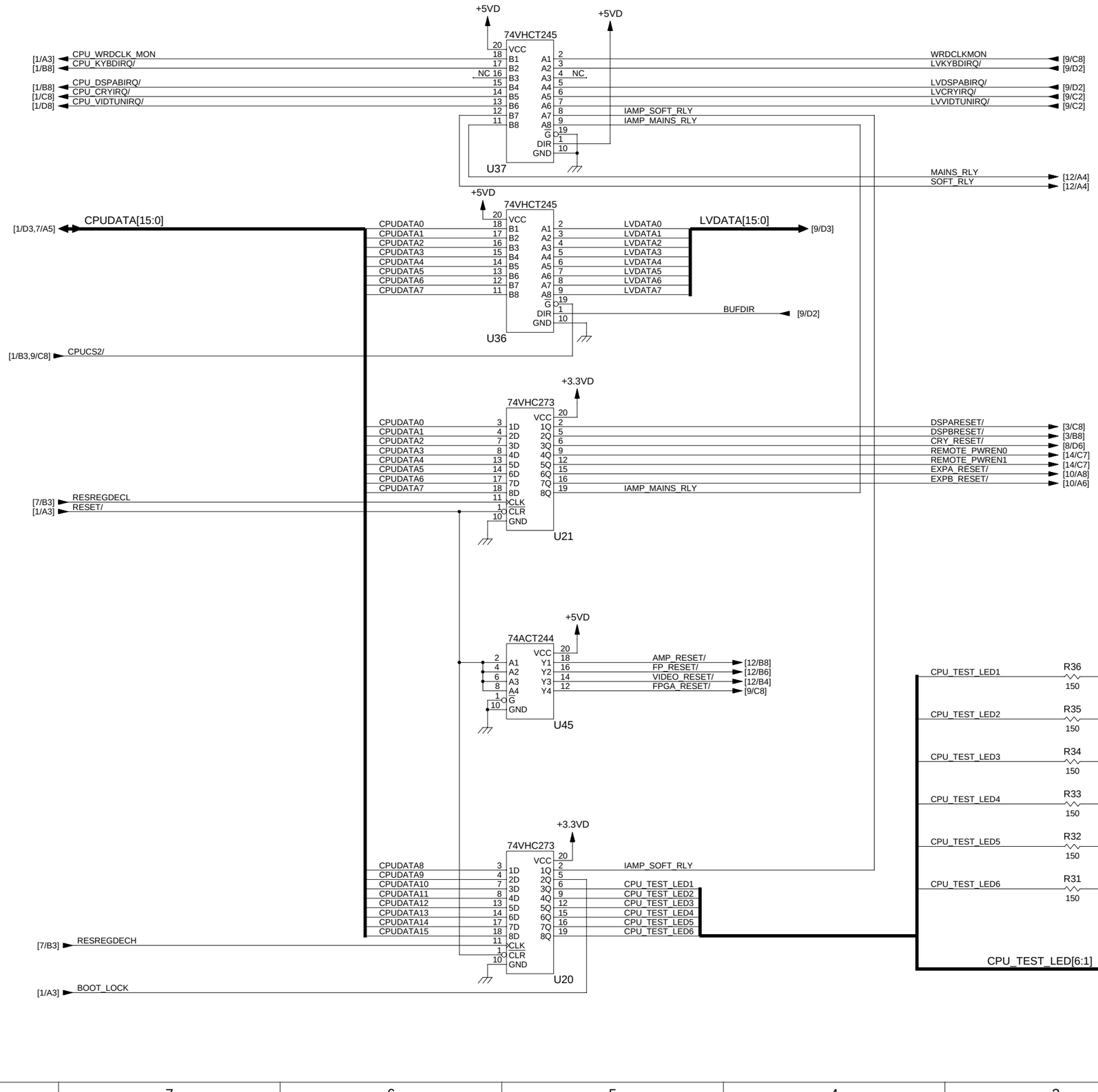
TITLE: SCHEM, MAIN BD,RV8
HOST PROCESSOR

SIZE	CODE	NUMBER	REV
B		060-15559	6

FILE NAME: 15559-6. 1 SHEET 1 OF 19

5-6-2004_9:30

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020913-00	RWH 11/05/02	CW 12/20/02
		CAM 11/06/02	MAG 12/20/02
2	CHANGED PER DCR 030307-00	RWH 5/2/03	CW 5/20/03
		CAM 5/14/03	MAG 5/20/03
3	CHANGED PER DCR 030626-00	RWH 9/29/03	ECM 10/9/03
		CAM 10/2/03	MAG 10/9/03



CONTRACT NO.	lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS	DATE	TITLE	
DRAWN RWH	4/26/02	SCHEM, MAIN BD,RV8 BUFFERS, LEVEL SHIFTERS	
CHECKED CAM	4/30/02	SIZE B / CODE / NUMBER 060-15559	REV 3
Q.C. CW	5/1/02	FILE NAME 15559-6.2	SHEET 2 OF 19
ISSUED JV	4/30/02		

5-6-2004_9:30

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020913-00	RWH 11/05/02	CW 12/20/02
		CAM 11/06/02	MAG 12/20/02
2	CHANGED PER DCR 030307-00	RWH 5/2/03	CW 5/20/03
		CAM 5/14/03	MAG 5/20/03
3	CHANGED PER DCR 030626-00	RWH 9/29/03	ECM 10/9/03
		CAM 10/2/03	MAG 10/9/03
4	CHANGED PER DCR 031124-00	RWH 12/2/03	CW 12/30/03
		CAM 12/8/03	MAG 12/30/03

SPARES

U47 74HCU04 NC

U47 74HCU04 NC

U46 74LCX14 NC

U46 74LCX14 NC

CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS	DATE	TITLE: SCHEM, MAIN BD,RV8 DSP HOST 1 AND 2	
DRAWN RWH	4/26/02		
CHECKED CAM	4/30/02	SIZE B / CODE / NUMBER 060-15559 / REV 4	
Q.C. CW	5/1/02	FILE NAME 15559-6. 3	SHEET 3 OF 19
ISSUED JV	4/30/02		

5-6-2004_9:30

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020913-00	RWH 11/05/02	CW 12/20/02
		CAM 11/06/02	MAG 12/20/02
2	CHANGED PER DCR 030307-00	RWH 5/2/03	CW 5/20/03
		CAM 5/14/03	MAG 5/20/03
3	CHANGED PER DCR 030626-00	RWH 9/29/03	ECM 10/9/03
		CAM 10/2/03	MAG 10/9/03

EBOOT	LBOOT	BMS	STATE
0	0	1	HOST BOOT (N/A)
0	1	0	SPI BOOT (DEFAULT)
0	1	1	LINK PORT BOOT
1	0	**	EEPROM BOOT (N/A)
1	1	X	RESERVED

** BMS BECOMES AN OUTPUT.
CHIP SELECT FOR EEPROM

+3.3VD

1 RP4 10K 8
2 RP4 10K 7
3 RP4 10K 6

R70
R69 *
R71

DSPA_A[19:0]

ADSP-21161N
MEMORY CTRL

NC	K4	ADDR23	DATA47	C15	DSPA_D31
NC	K2	ADDR22	DATA46	D14	DSPA_D30
NC	L3	ADDR21	DATA45	C14	DSPA_D29
NC	K3	ADDR20	DATA44	D15	DSPA_D28
NC	L1	ADDR19	DATA43	E14	DSPA_D27
NC	M3	ADDR18	DATA42	D13	DSPA_D26
NC	L2	ADDR17	DATA41	E15	DSPA_D25
NC	M1	ADDR16	DATA40	F13	DSPA_D24
NC	N2	ADDR15	DATA39	E13	DSPA_D23
DSPA_A14	N1	ADDR14	DATA38	F14	DSPA_D22
DSPA_A13	P1	ADDR13	DATA37	F12	DSPA_D21
NC	M2	ADDR12	DATA36	F15	DSPA_D20
NC	R2	ADDR11	DATA35	G13	DSPA_D19
NC	N3	ADDR10	DATA34	G12	DSPA_D18
DSPA_A9	P2	ADDR9	DATA33	G14	DSPA_D17
DSPA_A8	P3	ADDR8	DATA32	G15	DSPA_D16
DSPA_A7	R3	ADDR7	DATA31	H15	DSPA_D15
DSPA_A6	M4	ADDR6	DATA30	H14	DSPA_D14
DSPA_A5	N4	ADDR5	DATA29	H12	DSPA_D13
DSPA_A4	P4	ADDR4	DATA28	H13	DSPA_D12
DSPA_A3	R4	ADDR3	DATA27	J15	DSPA_D11
DSPA_A2	L4	ADDR2	DATA26	J12	DSPA_D10
DSPA_A1	N5	ADDR1	DATA25	J14	DSPA_D9
DSPA_A0	M5	ADDR0	DATA24	J13	DSPA_D8
			DATA23	K15	DSPA_D7
			DATA22	K12	DSPA_D6
			DATA21	K14	DSPA_D5
			DATA20	L13	DSPA_D4
			DATA19	K13	DSPA_D3
			DATA18	L15	DSPA_D2
			DATA17	M13	DSPA_D1
			DATA16	L14	DSPA_D0

NC	R5	MS3		
NC	P5	MS2		
NC	M6	MS1		
	N6	MS0		
	M9	WR		
	R8	RD		
	N9	BRST		
	M12	ACK		
	A5	EBOOT		
	A6	LBOOT		
	A3	BMS		

SDA10	M10		
DQM	P13		
RAS	M11		
CAS	L12		
SDWE	R14		
SDCKE	N10		
SDCLK0	P10		
SDCLK1	P9	NC	

U16

DSPASDRAMCS/

[5/B8] DSPABWR/
[5/B8] DSPABRD/
[5/B8] DSPABC_BRST
[5/B8] DSPABC_ACK

+3.3VD

VDDQ: 81 75 55 49 41 35 9 3
VDD: 43 29 15 1

2MX32
100MHZ

DQ31	56		BA1	23 DSPA_A14
DQ30	54		BA0	22 DSPA_A13
DQ29	53		A10	24 DSPA_AD10
DQ28	51		A9	66 DSPA_A9
DQ27	50		A8	65 DSPA_A8
DQ26	48		A7	64 DSPA_A7
DQ25	47		A6	63 DSPA_A6
DQ24	45		A5	62 DSPA_A5
DQ23	42		A4	61 DSPA_A4
DQ22	40		A3	60 DSPA_A3
DQ21	39		A2	27 DSPA_A2
DQ20	37		A1	26 DSPA_A1
DQ19	36		A0	25 DSPA_A0
DQ18	34			
DQ17	33		DQM3	59
DQ16	31		DQM2	28
DQ15	85		DQM1	71
DQ14	83		DQM0	16
DQ13	82			
DQ12	80		RAS	19
DQ11	79		CAS	18
DQ10	77		WE	17
DQ9	76		CS	20
DQ8	74			
DQ7	13		CKE	67
DQ6	11		CLK	68
DQ5	10			
DQ4	8		NC6	73 NC
DQ3	7		NC5	70 NC
DQ2	5		NC4	69 NC
DQ1	4		NC3	57 NC
DQ0	2		NC2	30 NC
			NC1	21 NC
			NC0	14 NC

VSSQ: 84 78 52 46 38 32 12 6
VSS: 86 72 58 44

U6

CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS	DATE	TITLE: SCHEM, MAIN BD,RV8 DSP A SDRAM AND FLASH	
DRAWN RWH	4/26/02	SIZE B	CODE	NUMBER 060-15559	REV 3
CHECKED CAM	4/30/02		
Q.C. CW	5/1/02	FILE NAME 15559-6. 4	SHEET 4 OF 19
ISSUED JV	4/30/02		

5-6-2004_9:30

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020913-00	RWH 11/05/02	CW 12/20/02
		CAM 11/06/02	MAG 12/20/02
2	CHANGED PER DCR 030307-00	RWH 5/2/03	CW 5/20/03
		CAM 5/14/03	MAG 5/20/03
3	CHANGED PER DCR 030626-00	RWH 9/29/03	ECM 10/9/03
		CAM 10/2/03	MAG 10/9/03

EBOOT	LBOOT	BMS	STATE
0	0	1	HOST BOOT (N/A)
0	1	0	SPI BOOT (DEFAULT)
0	1	1	LINK PORT BOOT
1	0	**	EEPROM BOOT (N/A)
1	1	X	RESERVED

** BMS BECOMES AN OUTPUT.
CHIP SELECT FOR EEPROM

+3.3VD
RP12 10K 8
RP12 10K 7
RP12 10K 6
R137
R136 *
R138

DSPB_A[14:0]

U34 ADSP-21161N MEMORY CTRL

NC	K4	ADDR23	DATA47	C15	DSPB_D31	56	DQ31
NC	K2	ADDR22	DATA46	D14	DSPB_D30	54	DQ30
NC	L3	ADDR21	DATA45	C14	DSPB_D29	53	DQ29
NC	K3	ADDR20	DATA44	D15	DSPB_D28	51	DQ28
NC	L1	ADDR19	DATA43	E14	DSPB_D27	50	DQ27
NC	M3	ADDR18	DATA42	D13	DSPB_D26	48	DQ26
NC	L2	ADDR17	DATA41	E15	DSPB_D25	47	DQ25
NC	M1	ADDR16	DATA40	F13	DSPB_D24	45	DQ24
NC	N2	ADDR15	DATA39	E13	DSPB_D23	42	DQ23
DSPB_A14	N1	ADDR14	DATA38	F14	DSPB_D22	40	DQ22
DSPB_A13	P1	ADDR13	DATA37	F12	DSPB_D21	39	DQ21
NC	M2	ADDR12	DATA36	F15	DSPB_D20	37	DQ20
NC	R2	ADDR11	DATA35	G13	DSPB_D19	36	DQ19
NC	N3	ADDR10	DATA34	G12	DSPB_D18	34	DQ18
DSPB_A9	P2	ADDR9	DATA33	G14	DSPB_D17	33	DQ17
DSPB_A8	P3	ADDR8	DATA32	G15	DSPB_D16	31	DQ16
DSPB_A7	R3	ADDR7	DATA31	H15	DSPB_D15	85	DQ15
DSPB_A6	M4	ADDR6	DATA30	H14	DSPB_D14	83	DQ14
DSPB_A5	N4	ADDR5	DATA29	H12	DSPB_D13	82	DQ13
DSPB_A4	P4	ADDR4	DATA28	H13	DSPB_D12	80	DQ12
DSPB_A3	R4	ADDR3	DATA27	J15	DSPB_D11	79	DQ11
DSPB_A2	L4	ADDR2	DATA26	J12	DSPB_D10	77	DQ10
DSPB_A1	N5	ADDR1	DATA25	J14	DSPB_D9	76	DQ9
DSPB_A0	M5	ADDR0	DATA24	J13	DSPB_D8	74	DQ8
			DATA23	K15	DSPB_D7	13	DQ7
NC	R5	MS3	DATA22	K12	DSPB_D6	11	DQ6
NC	P5	MS2	DATA21	K14	DSPB_D5	10	DQ5
NC	M6	MS1	DATA20	L13	DSPB_D4	8	DQ4
	N6	MS0	DATA19	K13	DSPB_D3	7	DQ3
			DATA18	L15	DSPB_D2	5	DQ2
	M9	WR	DATA17	M13	DSPB_D1	4	DQ1
	R8	RD	DATA16	L14	DSPB_D0	2	DQ0
	N9	BRST					
	M12	ACK					
	A5	EBOOT					
	A6	LBOOT					
	A3	BMS					

SDA10	M10	
DQM	P13	
RAS	M11	
CAS	L12	
SDWE	R14	
SDCKE	N10	
SDCLK0	P10	
SDCLK1	P9	NC

[4/B7] DSPABWR/
[4/B7] DSPABRD/
[4/B7] DSPABC_BRST
[4/B7] DSPABC_ACK

DSPBSDRAMCS/

+3.3VD
81 75 55 49 41 35 9 3 43 29 15 1
VDDQ VDD

2MX32
100MHZ

BA1	23	DSPB_A14	
BA0	22	DSPB_A13	
A10	24	DSPB_AD10	
A9	66	DSPB_A9	
A8	65	DSPB_A8	
A7	64	DSPB_A7	
A6	63	DSPB_A6	
A5	62	DSPB_A5	
A4	61	DSPB_A4	
A3	60	DSPB_A3	
A2	27	DSPB_A2	
A1	26	DSPB_A1	
A0	25	DSPB_A0	
DQM3	59		
DQM2	28		
DQM1	71		
DQM0	16		
RAS	19		
CAS	18		
WE	17		
CS	20		
CKE	67		
CLK	68		
NC6	73	NC	
NC5	70	NC	
NC4	69	NC	
NC3	57	NC	
NC2	30	NC	
NC1	21	NC	
NC0	14	NC	

VSSQ VSS
84 78 52 46 38 32 12 6 86 72 58 44

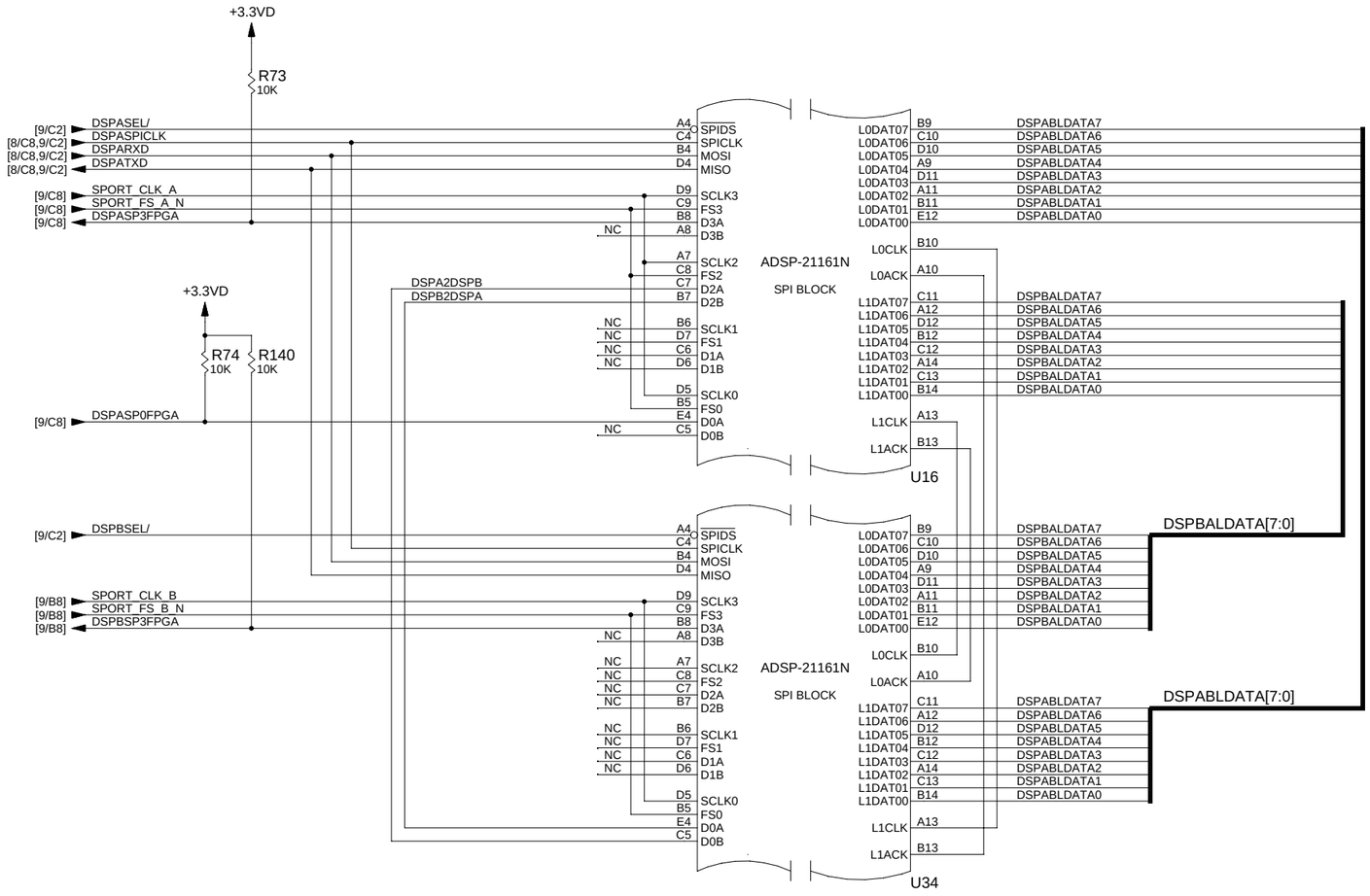
U27

SPARES
RP12
NC 5 4 NC
10K

CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS	DATE	TITLE	
DRAWN RWH	4/26/02	SCHEM, MAIN BD,RV8 DSP B EXTERNAL MEMORY	
CHECKED CAM	4/30/02	SIZE B / CODE / NUMBER 060-15559 / REV 3	
Q.C. CW	5/1/02	FILE NAME 15559-6. 5	SHEET 5 OF 19
ISSUED JV	4/30/02		

5-6-2004_9:30

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020913-00	RWH 11/05/02	CW 12/20/02
		CAM 11/06/02	MAG 12/20/02
2	CHANGED PER DCR 030307-00	RWH 5/2/03	CW 5/20/03
		CAM 5/14/03	MAG 5/20/03
3	CHANGED PER DCR 030626-00	RWH 9/29/03	ECM 10/9/03
		CAM 10/2/03	MAG 10/9/03



CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730

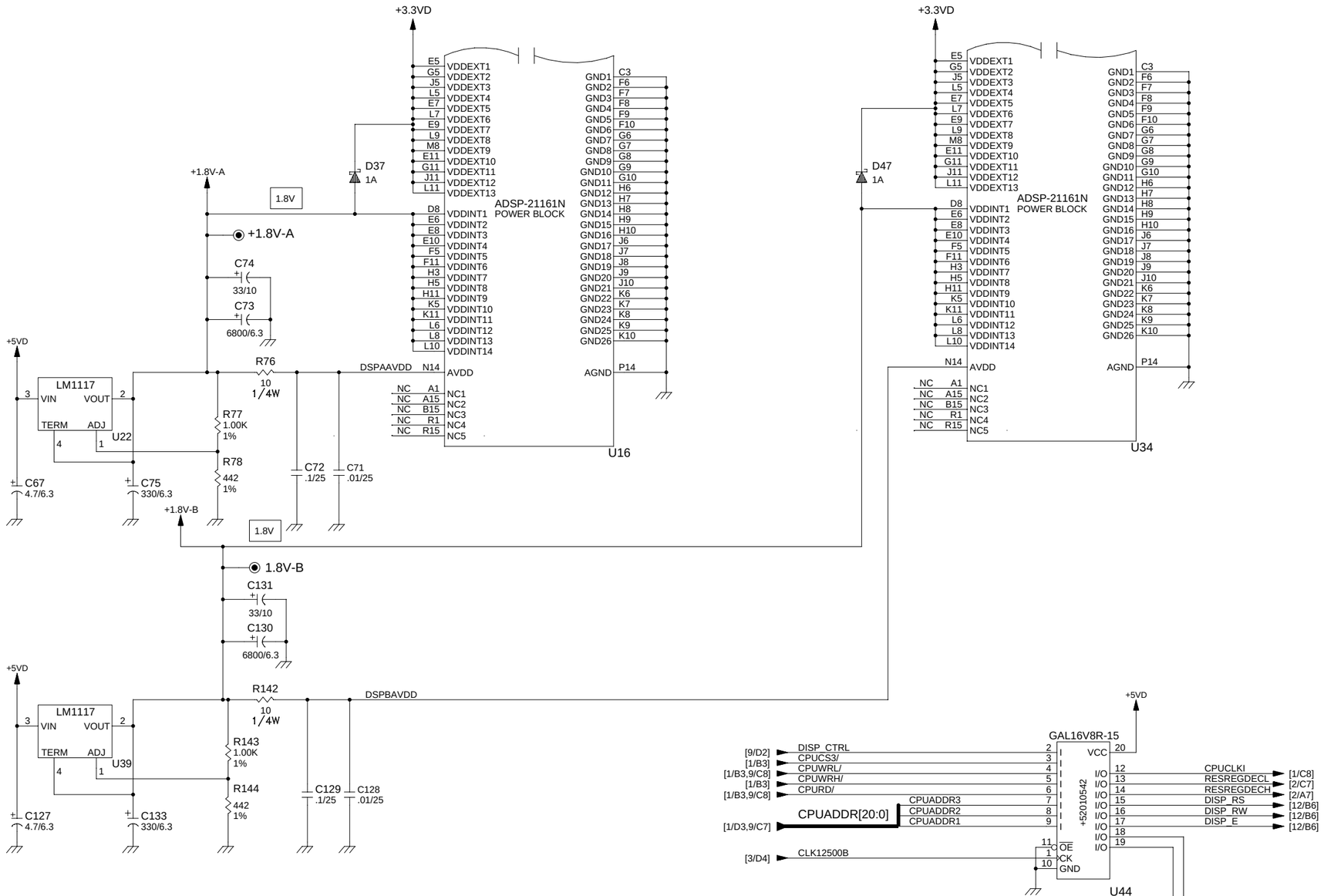
APPROVALS		DATE
DRAWN	RWH	4/26/02
CHECKED	CAM	4/30/02
Q.C.	CW	5/1/02
ISSUED	JV	4/30/02

TITLE: SCHEM, MAIN BD,RV8
DSP SPI, SERIAL AND LINK PORTS

SIZE	CODE	NUMBER	REV
B		060-15559	3

FILE NAME: 15559-6.6 SHEET 6 OF 19

5-6-2004_9:30



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020913-00	RWH 11/05/02	CW 12/20/02
		CAM 11/06/02	MAG 12/20/02
2	CHANGED PER DCR 030307-00	RWH 5/2/03	CW 5/20/03
		CAM 5/14/03	MAG 5/20/03
3	CHANGED PER DCR 030626-00	RWH 9/29/03	ECM 10/9/03
		CAM 10/2/03	MAG 10/9/03
4	CHANGED C73, 75, 130, 133 PER ECO 040422-00	RWH 4/27/04	CW 4/29/04
		CAM 4/29/04	KAB 5/2/04

CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	4/26/02
CHECKED	CAM	4/30/02
Q.C.	CW	5/1/02
ISSUED	JV	4/30/02

TITLE
SCHEM, MAIN BD,RV8
DSP/FPGA POWER CONN.

SIZE	CODE	NUMBER	REV
B		060-15559	4

FILE NAME 15559-6. 7

SHEET 7 OF 19

5-6-2004_9:30

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020913-00	RWH 11/05/02	CW 12/20/02
		CAM 11/06/02	MAG 12/20/02
2	CHANGED PER DCR 030307-00	RWH 5/2/03	CW 5/20/03
		CAM 5/14/03	MAG 5/20/03
3	CHANGED PER DCR 030626-00	RWH 9/29/03	ECM 10/9/03
		CAM 10/2/03	MAG 10/9/03

CS494001-CL

U25

U13

U7

U19

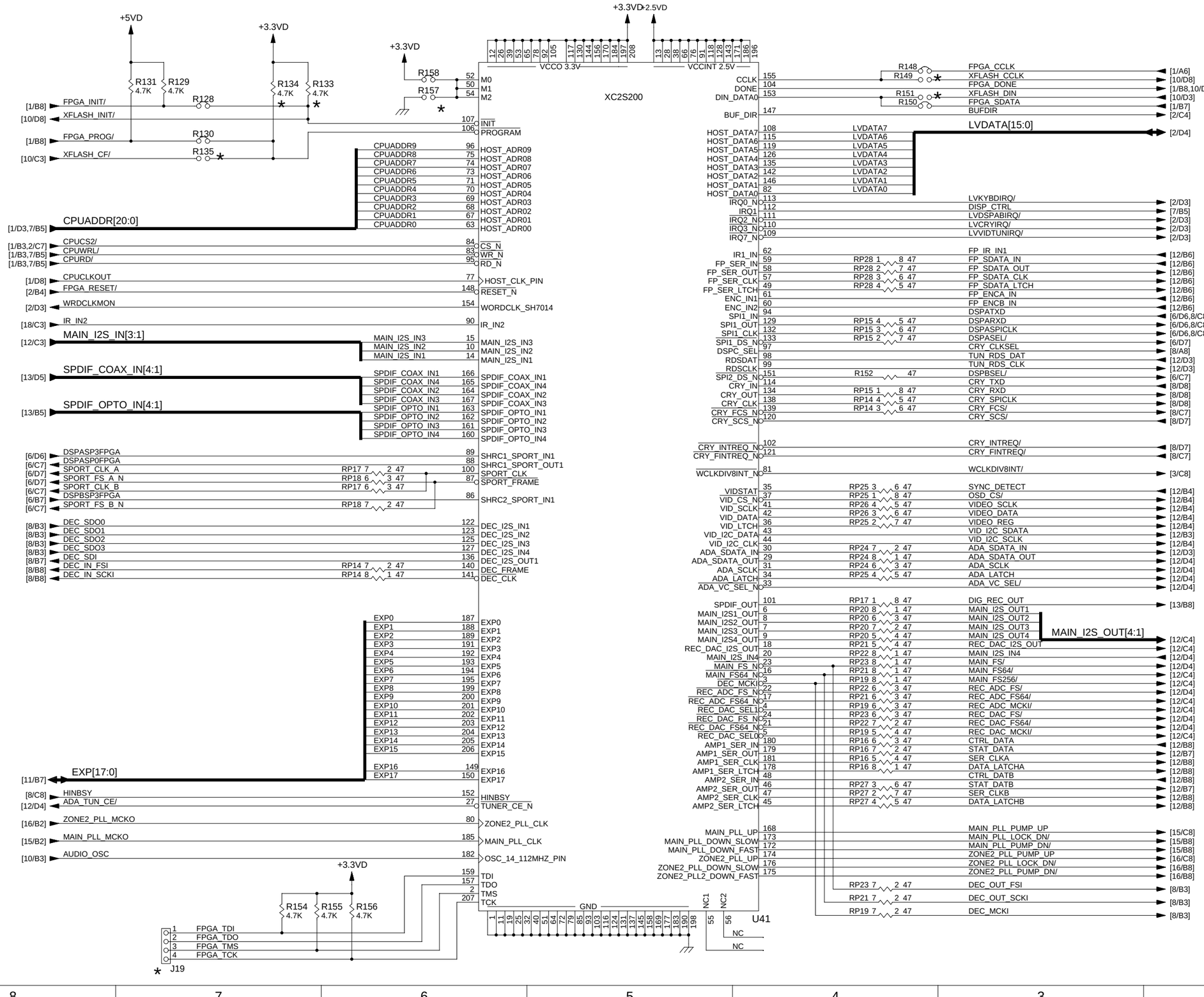
U30

SPARES

CONTRACT NO.	Lexicon 3 OAK PARK BEDFORD, MA 01730		
APPROVALS	DATE	TITLE	SCHEM, MAIN BD,RV8 CRYSTAL DSP
DRAWN RWH	4/26/02	SIZE B	CODE / NUMBER 060-15559 / REV 3
CHECKED CAM	4/30/02		
Q.C. CW	5/1/02	FILE NAME	15559-6. 8
ISSUED JV	4/30/02	SHEET	8 OF 19

10-10-2003_11:04

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020913-00	RWH 11/05/02	CW 12/20/02
		CAM 11/06/02	MAG 12/20/02
2	CHANGED PER DCR 030307-00	RWH 5/2/03	CW 5/20/03
		CAM 5/14/03	MAG 5/20/03
3	CHANGED PER DCR 030626-00	RWH 9/29/03	ECM 10/9/03
		CAM 10/2/03	MAG 10/9/03



CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	4/26/02
CHECKED	CAM	4/30/02
Q.C.	CW	5/1/02
ISSUED	JV	4/30/02

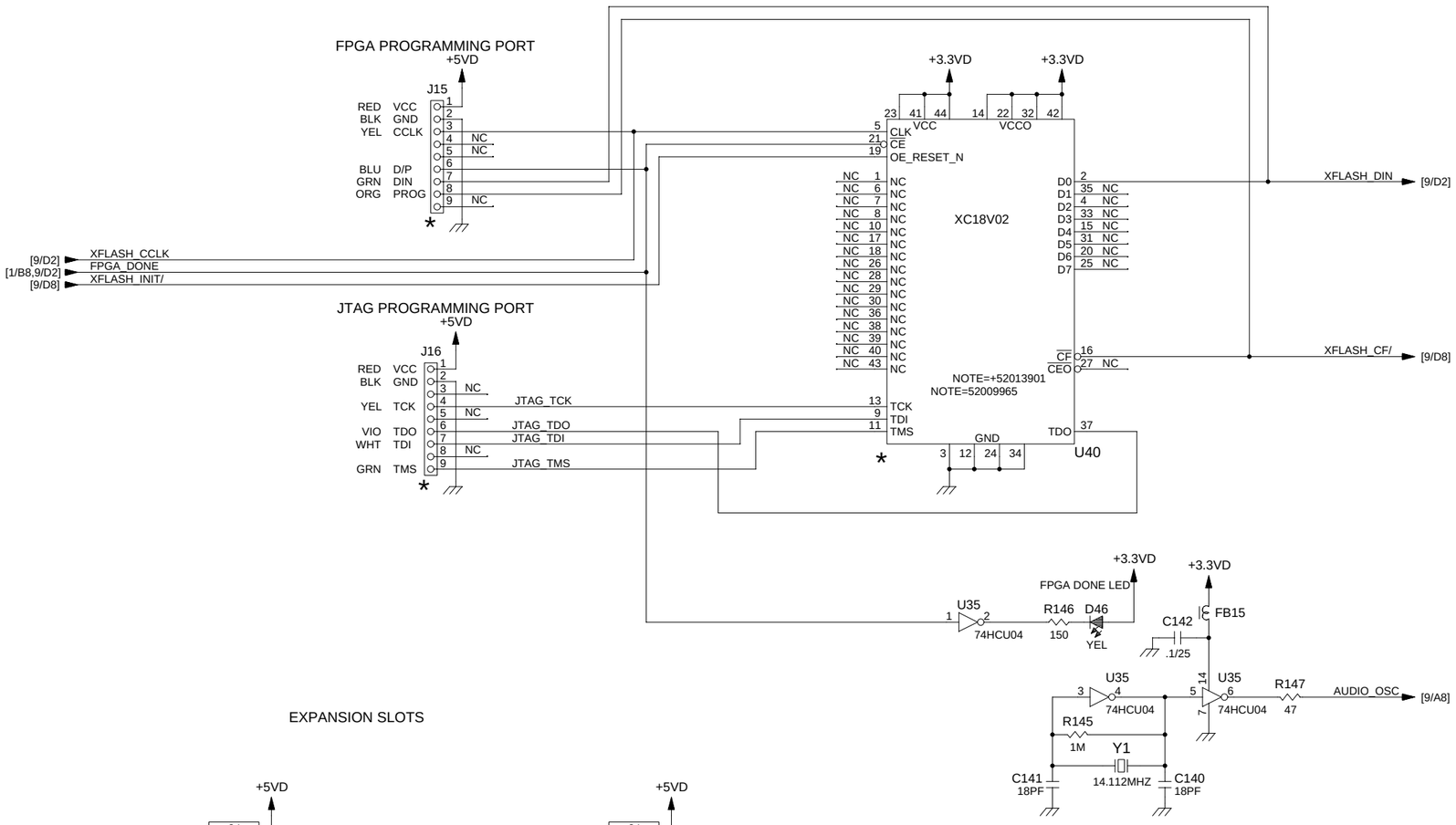
TITLE: SCHEM, MAIN BD,RV8 MAIN FPGA

SIZE	CODE	NUMBER	REV
B		060-15559	3

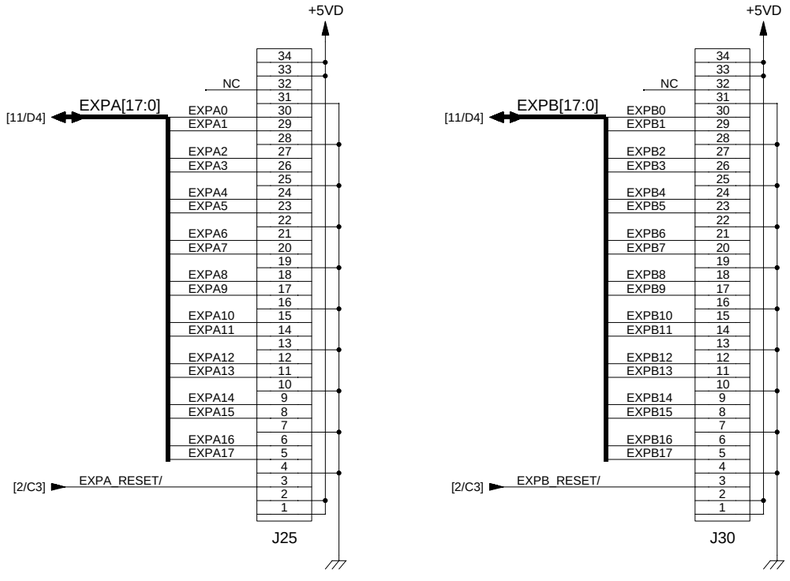
FILE NAME: 15559-6. 9 SHEET 9 OF 19

10-10-2003_11:04

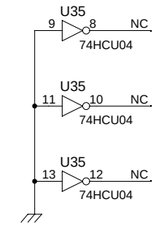
FPGA FLASH PROM (for development only)



EXPANSION SLOTS



SPARES



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020913-00	RWH 11/05/02	CW 12/20/02
		CAM 11/06/02	MAG 12/20/02
2	CHANGED PER DCR 030307-00	RWH 5/2/03	CW 5/20/03
		CAM 5/14/03	MAG 5/20/03
3	CHANGED PER DCR 030626-00	RWH 9/29/03	ECM 10/9/03
		CAM 10/2/03	MAG 10/9/03

CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

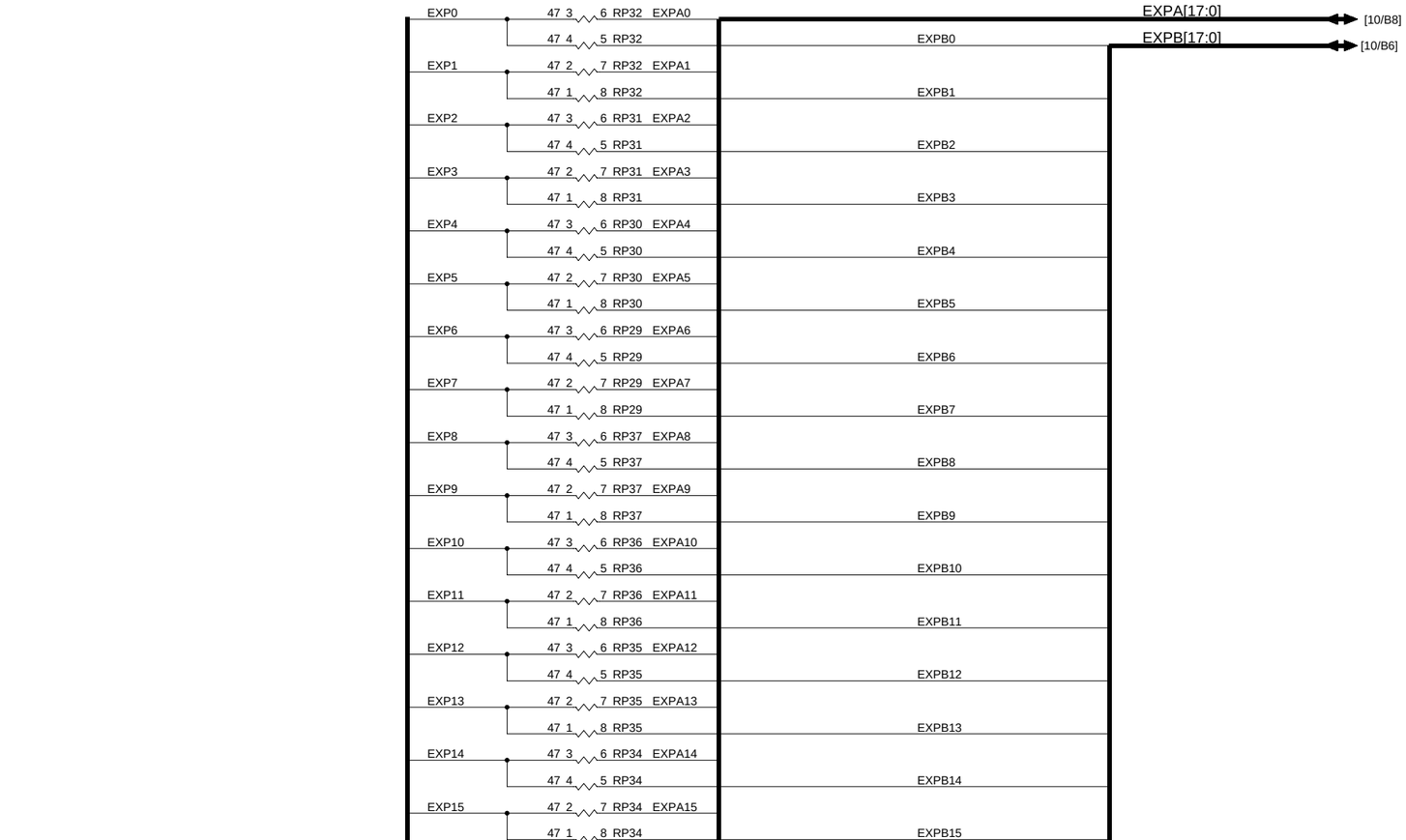
APPROVALS		DATE
DRAWN	RWH	4/26/02
CHECKED	CAM	4/30/02
Q.C.	CW	5/1/02
ISSUED	JV	4/30/02

TITLE
SCHEM, MAIN BD,RV8
FPGA FLASH

SIZE	CODE	NUMBER	REV
B		060-15559	3

FILE NAME 15559-6. 10
SHEET 10 OF 19

10-10-2003 11:04



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020913-00	RWH 11/05/02	CW 12/20/02
		CAM 11/06/02	MAG 12/20/02
2	CHANGED PER DCR 030307-00	RWH 5/2/03	CW 5/20/03
		CAM 5/14/03	MAG 5/20/03
3	CHANGED PER DCR 030626-00	RWH 9/29/03	ECM 10/9/03
		CAM 10/2/03	MAG 10/9/03

CONTRACT NO.

lexicon

3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	4/26/02
CHECKED	CAM	4/30/02
Q.C.	CW	5/1/02
ISSUED	JV	4/30/02

TITLE
SCHEM, MAIN BD,RV8
EXPANSION PORT SERIES TERMINATIONS

SIZE	CODE	NUMBER	REV
B		060-15559	3

FILE NAME 15559-6. 11

SHEET 11 OF 19

10-10-2003_11:04

RS-232 TRANSCEIVER

MAX202E

+5VD

C27 .1/25
C28 .1/25
C31 .1/25
C30 .1/25
C29 .1/25

2 V+ C1+ 1
16 VCC C1- 3
15 GND C2+ 4
6 V- C2- 5

W2 *
W1 *

[1/A3] DEBUG_TXD 11 14 TXDA FB5
[1/A3] DEBUG_RXD 12 13 RXDA FB6
[1/A3] USER_TXD 10 7 TXDB FB3
[1/A3] USER_RXD 9 8 RXDB FB4

U5

C13 150PF
C12 150PF
C15 150PF
C14 150PF

+5VD
R23 4.7K
R22 4.7K
R21 4.7K
R24 4.7K

RS-232
(FEMALE)
DE9F

NC A5
NC A9
A4
A8
RXD_A A3
NC A7
TXD_A A2
A6
NC A1
SHD1
SHD2

J4

DE9F

NC B5
B9
NC B4
B8
RXD_B B3
NC B7
TXD_B B2
B6
NC B1
SHD1
SHD2

J4

ANALOG BOARD CONNECTORS

J26

[1/A3] RESET 1
[9/B2] ADA_VC_SEL/ 2
[9/B2] ADA_LATCH 3
[9/B2] ADA_SCLK 4
5
[9/B2] ADA_SDATA_OUT 6
ADA_SDATA_IN 7 [9/B2]
[9/A8] ADA_TUN_CE/ 8
9
TUN_RDS_CLK 10
TUN_RDS_DAT 11 [9/C2]
12 [9/C2]
13
[9/B2] REC_DAC_FS/ 14
[9/B2] REC_ADC_FS/ 15
[9/B2] MAIN_FS/ 16
17
[9/B2] REC_DAC_FS64/ 18
[9/B2] MAIN_I2S_IN4 19
20
[9/B2] REC_ADC_FS64/ 21
[9/B2] REC_DAC_I2S_OUT 22
23
[9/B2] MAIN_FS64/ 24
25
MAIN_I2S_IN3 26
MAIN_I2S_IN2 27
MAIN_I2S_IN1 28
MAIN_I2S_IN[3:1] [9/C7]
29
[9/B3] MAIN_I2S_OUT[4:1]
MAIN_I2S_OUT4 30
MAIN_I2S_OUT3 31
MAIN_I2S_OUT2 32
MAIN_I2S_OUT1 33
34
[9/B2] REC_DAC_MCKI/ 35
36
[9/B2] REC_ADC_MCKI/ 37
38
[9/B2] MAIN_FS256/ 39
40

AMP BOARD CONNECTORS

+5VD +5VD +5VD +5VD

R187 10K
R171 10K
FB16
FB18

FLEX

[9/A2] SER_CLKA 1
[9/B2] CTRL_DATA 2
[9/A2] STAT_DATA 3
[9/A2] DATA_LATCHA 4
5
6
7
8
9
10
[1/B8] TEMP[7:1] TEMP1 11
TEMP2 12
TEMP3 13
TEMP4 14

J18

[9/A2] SER_CLKB 1
[9/A2] CTRL_DATB 2
[9/A2] STAT_DATB 3
[9/A2] DATA_LATCHB 4
[2/B4] AMP_RESET/ 5
[1/B8] SPARE_AD 6
7
8
9
10
TEMP5 11
TEMP6 12
TEMP7 13
14

J22

[1/B7] SYSLED 30 A1 Y1 19
[1/B7] OVLED 29 A2 Y2 20
27 A3 Y3 22 NC
26 A4 Y4 23 NC
24 OE

ABT16244

U15

FRONT PANEL CONNECTOR

+3.3VD +5VD +5VD

J20

[2/B4] FP_RESET/ 1
SYSTEM_ON_LED 2
[18/B3] FP_IR_BLINK 3
[18/B3] FP_IR_BLINK_RET 4
[9/C2] FP_IR_IN1 5
[1/B7] FP_IR_ACK 6
OVLD_LED 7
[9/C2] FP_ENCA_IN 8
[9/C2] FP_ENCB_IN 9
10
[9/C2] FP_SDATA_IN 11
[9/C2] FP_SDATA_OUT 12
[9/C2] FP_SDATA_CLK 13
[9/C2] FP_SDATA_LTCH 14
15
[7/B3] DISP_RS 16
NC 17
[7/B3] DISP_RW 18
[7/B3] DISP_E 19
20
[7/A3] FP_D[7:0] FP_D0 21
FP_D1 22
FP_D2 23
FP_D3 24
FP_D4 25
FP_D5 26
FP_D6 27
FP_D7 28
29
[1/A3] FPSWITCH1 30
[1/A3] FPSWITCH2 31
[1/A3] FPSWITCH3 32
NC 33
34
35
36
37
38
39
40

R173 10.0K 1%
R175 10.0K 1%
R172 100 1%
R174 100 1%
C165 .01/50
C170 .01/50

VIDEO BOARD CONNECTOR

+3.3VD

* R181 4.7K
* R180 4.7K

[2/B4] VIDEO_RESET/ 1
[9/B2] VIDEO_DATA 2
3
[9/B2] VIDEO_SCLK 4
5
[9/B2] OSD_CS/ 6
7
[9/B2] VIDEO_REG 8
9
[9/B2] VID_I2C_SCLK 10
11
[9/B2] VID_I2C_SDATA 12
13
[9/B2] SYNC_DETECT 14
15
[13/B3] CVID_ZON3 16

J29

AMP POWER SUPPLY CONNECTOR

FLEX

[2/D3] SOFT_RLY 1
[2/D3] MAINS_RLY 2
[1/C8] BROWN_OUT 3
4
5
6

* J28

J27

+5VD

1
2
3
4
5
6

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020913-00	RWH 11/05/02	CW 12/20/02
		CAM 11/06/02	MAG 12/20/02
2	CHANGED PER DCR 030307-00	RWH 5/2/03	CW 5/20/03
		CAM 5/14/03	MAG 5/20/03
3	CHANGED U52 PER DCR 030307-00-A	RWH 5/22/03	CW 5/22/03
		CAM 5/22/03	MAG 5/22/03
4	CHANGED PER DCR 030626-00	RWH 9/29/03	ECM 10/9/03
		CAM 10/2/03	MAG 10/9/03
5	CHANGED PER DCR 031124-00	RWH 12/2/03	CW 12/30/03
		CAM 12/8/03	MAG 12/30/03

CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	4/26/02
CHECKED	CAM	4/30/02
Q.C.	CW	5/1/02
ISSUED	JV	4/30/02

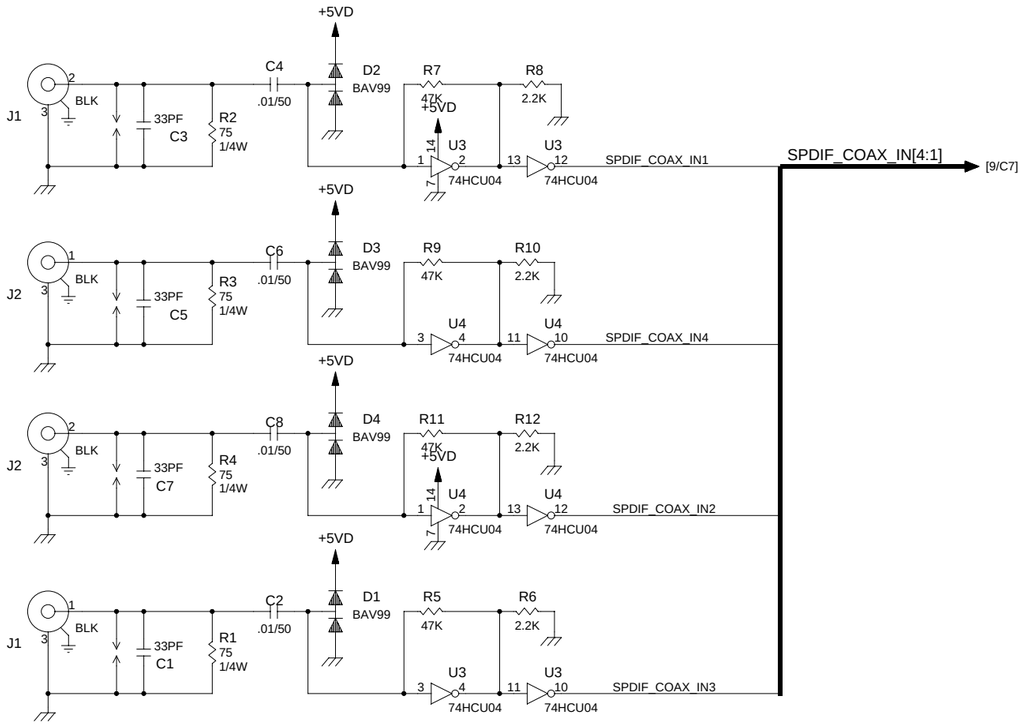
TITLE
SCHEM, MAIN BD,RV8
BOARD INTERCONN/DEBUG

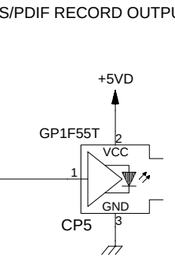
SIZE	CODE	NUMBER	REV
B		060-15559	5

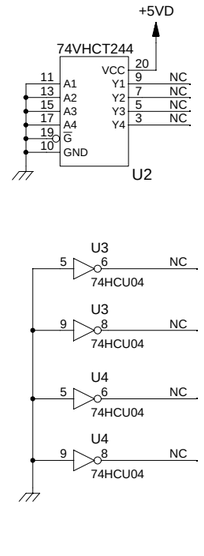
FILE NAME 15559-6. 12
SHEET 12 OF 19

12-30-2003 12:14

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020913-00	RWH 11/05/02	CW 12/20/02
		CAM 11/06/02	MAG 12/20/02
2	CHANGED PER DCR 030307-00	RWH 5/2/03	CW 5/20/03
		CAM 5/14/03	MAG 5/20/03
3	CHANGED PER DCR 030626-00	RWH 9/29/03	ECM 10/9/03
		CAM 10/2/03	MAG 10/9/03





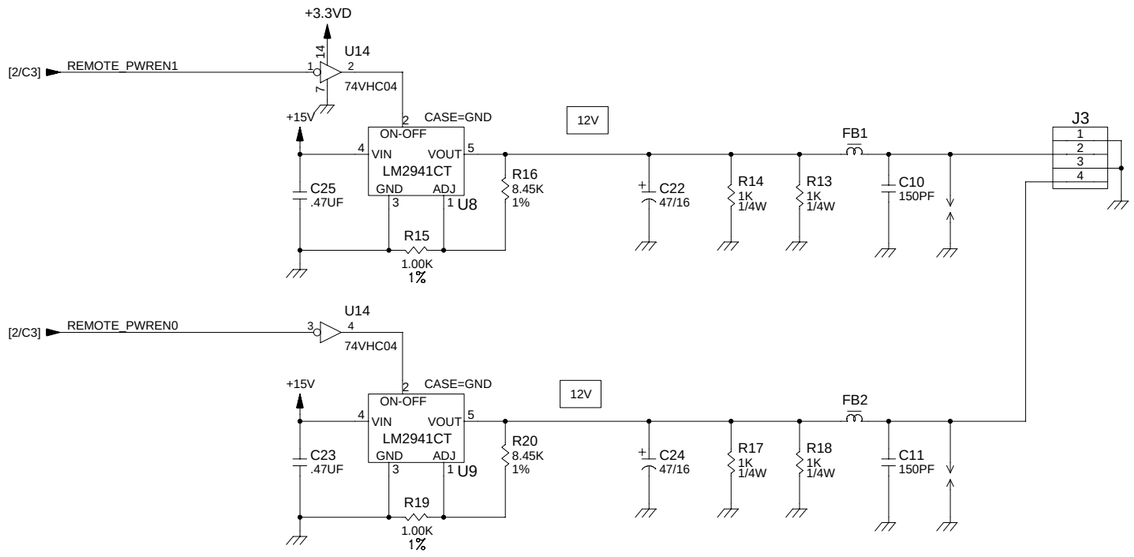


CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS	DATE	TITLE SCHEM, MAIN BD,RV8 SPDIF I/O	
DRAWN RWH	4/26/02		
CHECKED CAM	4/30/02	SIZE B / CODE / NUMBER 060-15559	REV 3
Q.C. CW	5/1/02	FILE NAME 15559-6. 13	SHEET 13 OF 19
ISSUED JV	4/30/02		

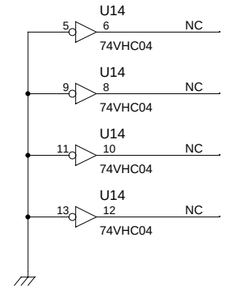
10-10-2003_11:04

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020913-00	RWH 11/05/02	CW 12/20/02
		CAM 11/06/02	MAG 12/20/02
2	CHANGED PER DCR 030307-00	RWH 5/2/03	CW 5/20/03
		CAM 5/14/03	MAG 5/20/03
3	CHANGED PER DCR 030626-00	RWH 9/29/03	ECM 10/9/03
		CAM 10/2/03	MAG 10/9/03

REMOTE POWER CONTROL DRIVERS



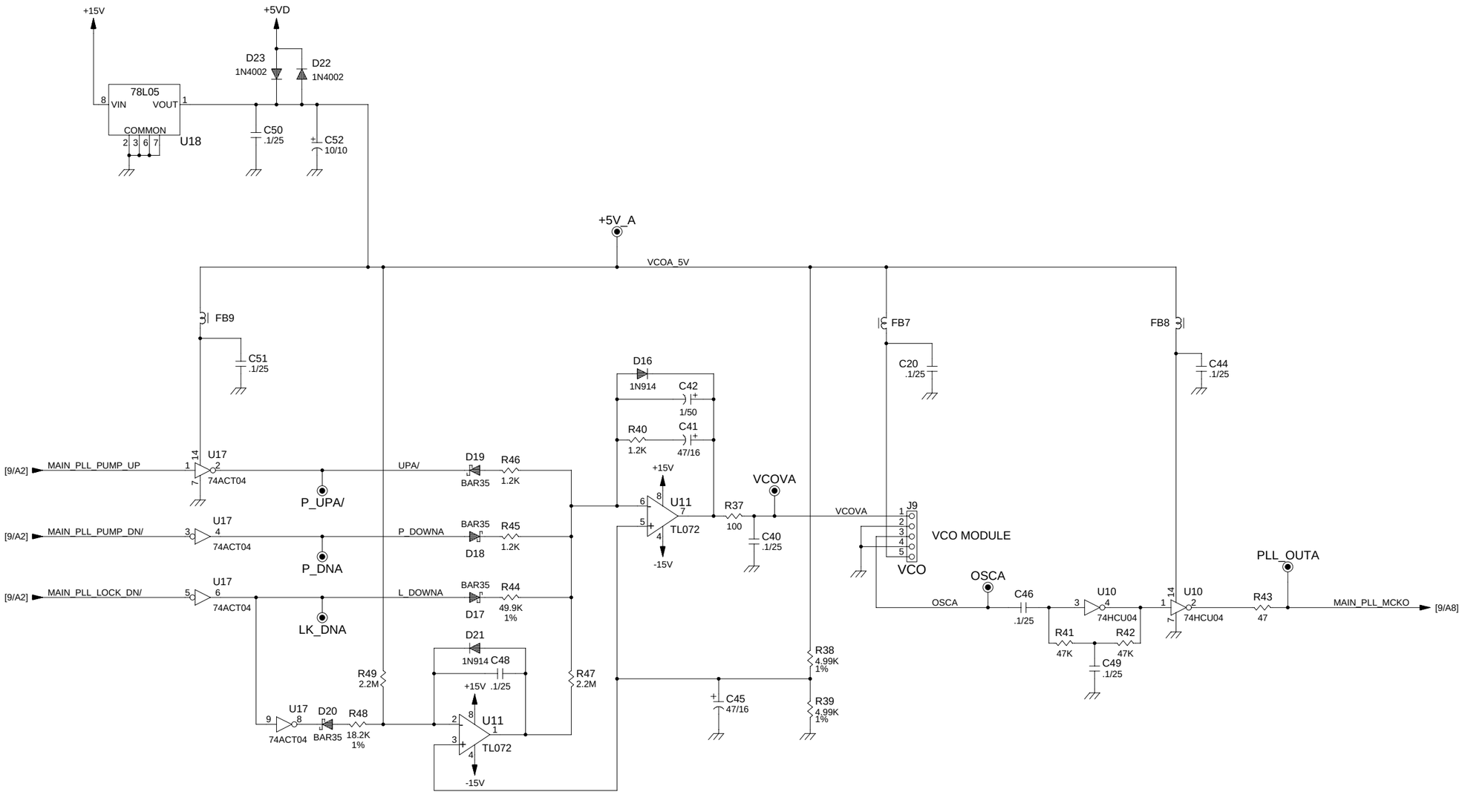
SPARES



CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS		DATE	TITLE: SCHEM, MAIN BD,RV8 TRIGGER OUTPUTS
DRAWN	RWH	4/26/02	SIZE: B; CODE: ; NUMBER: 060-15559; REV: 3
CHECKED	CAM	4/30/02	
Q.C.	CW	5/1/02	FILE NAME: 15559-6. 14; SHEET 14 OF 19
ISSUED	JV	4/30/02	

10-10-2003_11:04

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020913-00	RWH 11/05/02	CW 12/20/02
		CAM 11/06/02	MAG 12/20/02
2	CHANGED PER DCR 030307-00	RWH 5/2/03	CW 5/20/03
		CAM 5/14/03	MAG 5/20/03
3	CHANGED PER DCR 030626-00	RWH 9/29/03	ECM 10/9/03
		CAM 10/2/03	MAG 10/9/03



44.1K AND 48K @ 512FS

88.2K AND 96K @ 256 FS

CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	4/26/02
CHECKED	CAM	4/30/02
Q.C.	CW	5/1/02
ISSUED	JV	4/30/02

TITLE: SCHEM, MAIN BD,RV8
VCO A

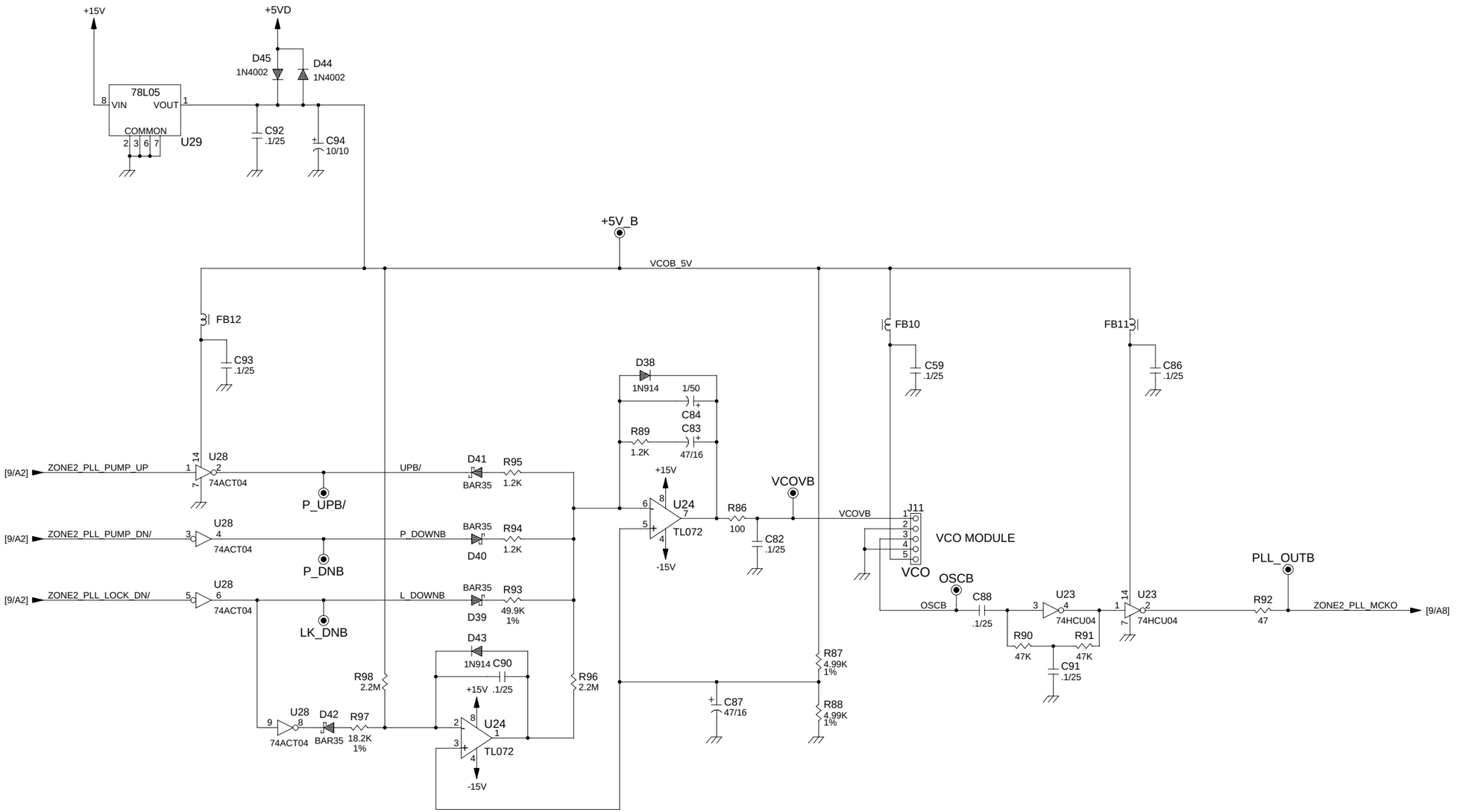
SIZE	CODE	NUMBER	REV
B		060-15559	3

FILE NAME: 15559-6. 15

SHEET 15 OF 19

4-27-2004 9:56

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020913-00	RWH 11/05/02	CW 12/20/02
		CAM 11/06/02	MAG 12/20/02
2	CHANGED PER DCR 030307-00	RWH 5/2/03	CW 5/20/03
		CAM 5/14/03	MAG 5/20/03
3	CHANGED PER DCR 030626-00	RWH 9/29/03	ECM 10/9/03
		CAM 10/2/03	MAG 10/9/03



CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS	DATE	TITLE SCHEM, MAIN BD,RV8 VCO B	
DRAWN RWH	4/26/02		
CHECKED CAM	4/30/02	SIZE B / CODE / NUMBER 060-15559 / REV 3	
Q.C. CW	5/1/02		
ISSUED JV	4/30/02	FILE NAME 15559-6. 16 / SHEET 16 OF 19	

4-27-2004 9:56

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020913-00	RWH 11/05/02	CW 12/20/02
		CAM 11/06/02	MAG 12/20/02
2	CHANGED PER DCR 030307-00	RWH 5/2/03	CW 5/20/03
		CAM 5/14/03	MAG 5/20/03
3	CHANGED PER DCR 030626-00	RWH 9/29/03	ECM 10/9/03
		CAM 10/2/03	MAG 10/9/03

POWER CONNECTOR

J31
1
2
3
4

+5VD
5VD
C169 100/25
C168 .22/50
C167 150PF
DGND1
DGND2
DGND3
DGND4
DGND5
DGND6
DGND7
DGND8
DGND9
LUG1

+15V
15VP
C173 100/25
C172 .22/50
C171 150PF

-15V
15VN
C176 100/25
C175 .22/50
C174 150PF

2.5V REGULATOR

+5VD
+2.5VD
LM2937
VIN VOUT TERM GND
1 3 4 2
U12
C54 4.7/6.3
C53 47/16

3.3V REGULATOR

+5VD
+3.3VD
D48 1N4002
W6
3.3V
LMS1585A
CASE=VOUT
VIN VOUT GND
TO-220
3 2 1
U38
L1 24UH *
C158 .1/25
C123 560/35 *
C122 10/10

+15V
L3 220UH *
R182 51 1/4W
R183 51 1/4W
R184 51 1/4W
R185 51 1/4W
R186 51 1/4W
R176 1K 1/4W
C177 470/16

FAN CONNECTORS

J24
J23
J32
J21

R188 0

D49 1N4002
C178 470/16
L2 220UH

3NF06
D1 D2 G S
2 4 1 3
Q2

R178 51 1/4W

[1/B8] FAN_DRV 9
U47 8 74HCU04
R179 10K
R177 4.7K
2N4401
Q1

CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	4/26/02
CHECKED	CAM	4/30/02
Q.C.	CW	5/1/02
ISSUED	JV	4/30/02

TITLE
SCHEM, MAIN BD,RV8
POWER SUPPLY

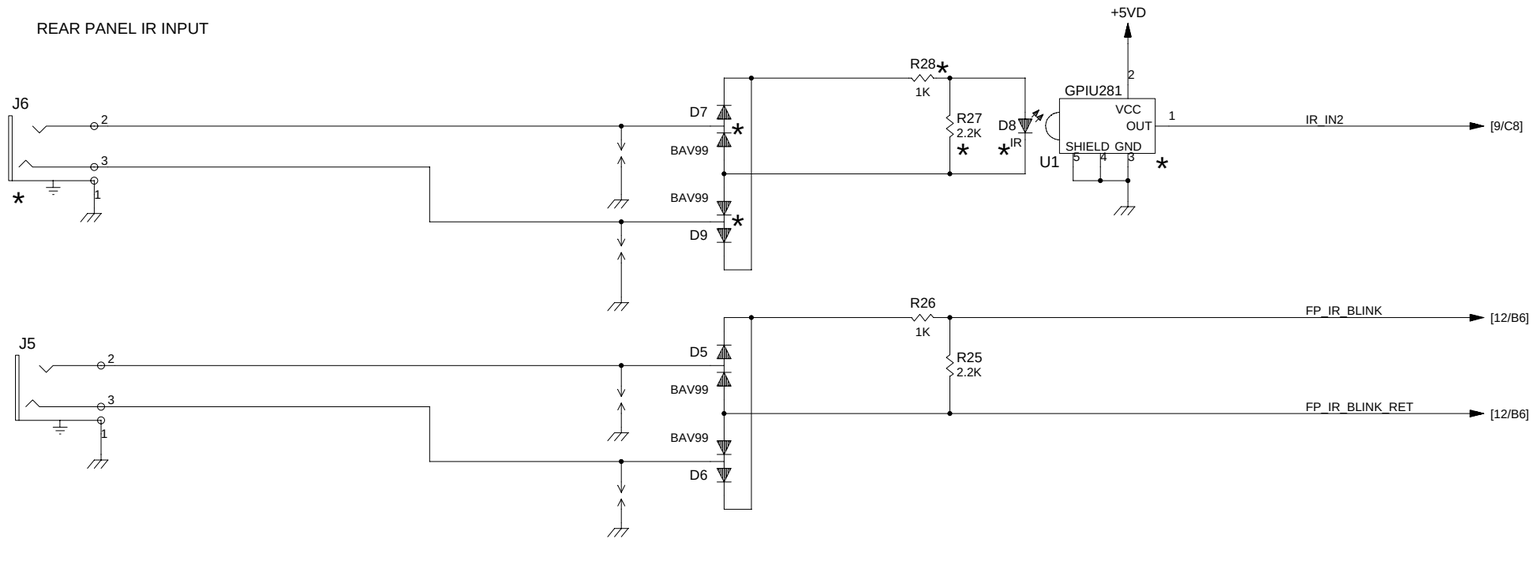
SIZE	CODE	NUMBER	REV
B		060-15559	3

FILE NAME 15559-6. 17
SHEET 17 OF 19

4-27-2004_9:56

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020913-00	RWH 11/05/02	CW 12/20/02
		CAM 11/06/02	MAG 12/20/02
2	CHANGED PER DCR 030307-00	RWH 5/2/03	CW 5/20/03
		CAM 5/14/03	MAG 5/20/03
3	CHANGED PER DCR 030626-00	RWH 9/29/03	ECM 10/9/03
		CAM 10/2/03	MAG 10/9/03

REAR PANEL IR INPUT



CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730

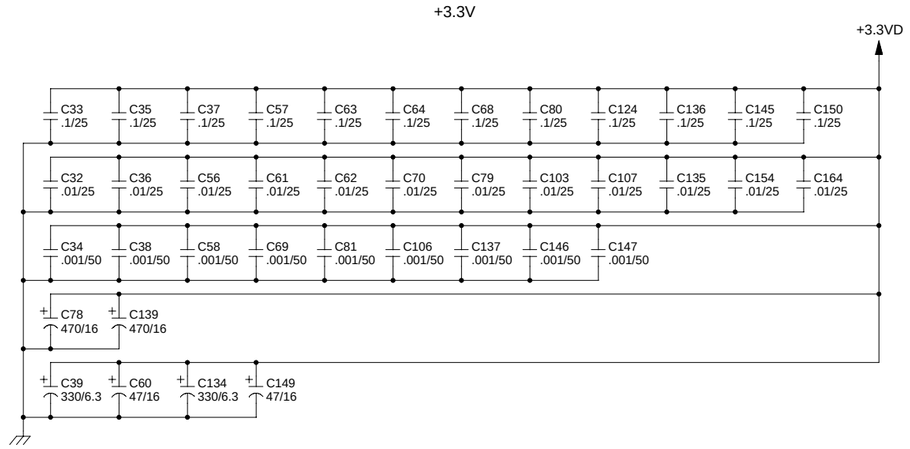
APPROVALS		DATE
DRAWN	RWH	4/26/02
CHECKED	CAM	4/30/02
Q.C.	CW	5/1/02
ISSUED	JV	4/30/02

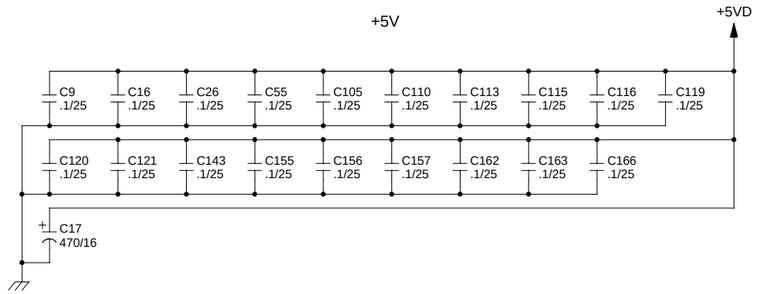
TITLE
SCHEM, MAIN BD,RV8
IR REMOTE CONNECTOR

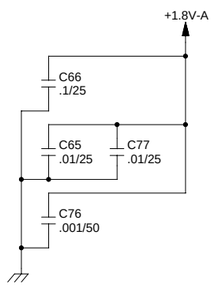
SIZE	CODE	NUMBER	REV
B		060-15559	3

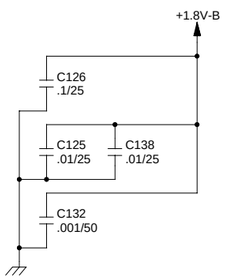
FILE NAME 15559-6. 18 SHEET 18 OF 19

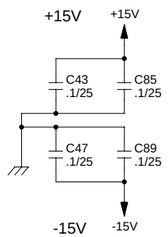
10-10-2003_11:04

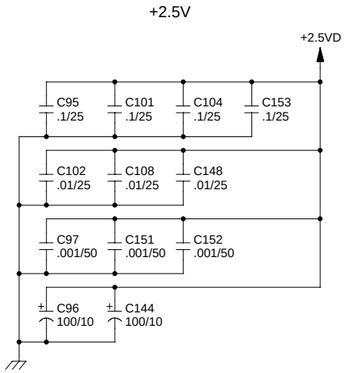












REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020913-00	RWH 11/05/02	CW 12/20/02
		CAM 11/06/02	MAG 12/20/02
2	CHANGED PER DCR 030307-00	RWH 5/2/03	CW 5/20/03
		CAM 5/14/03	MAG 5/20/03
3	CHANGED PER DCR 030626-00	RWH 9/29/03	ECM 10/9/03
		CAM 10/2/03	MAG 10/9/03
4	CHANGED C39, 134 PER ECO 040422-00	RWH 4/27/04	CW 4/29/04
		CAM 4/29/04	KAB 5/2/04

CONTRACT NO.

Lexicon

3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	4/26/02
CHECKED	CAM	4/30/02
Q.C.	CW	5/1/02
ISSUED	JV	4/30/02

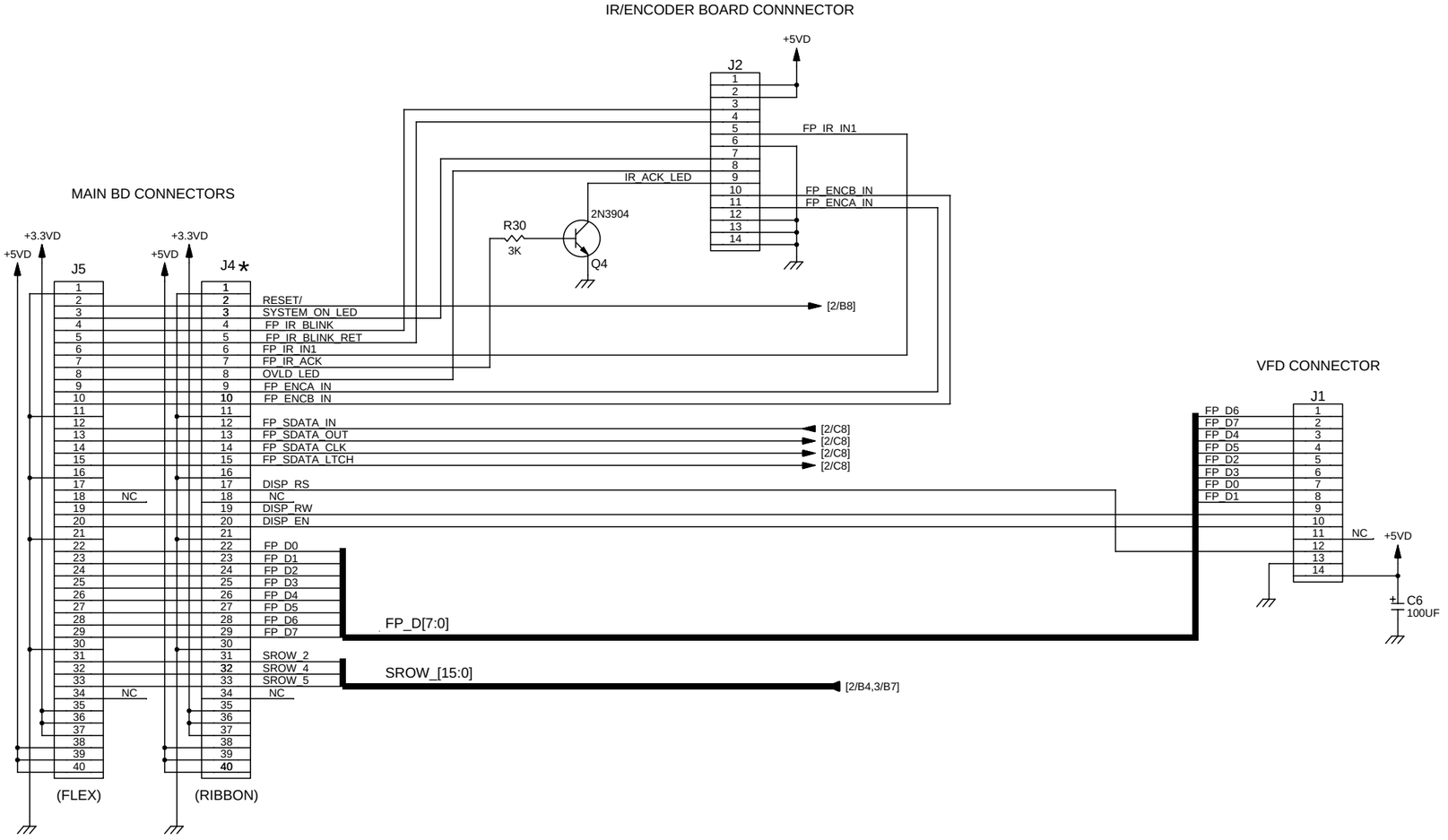
TITLE
SCHEM, MAIN BD,RV8
BYPASS CAPACITORS

SIZE	CODE	NUMBER	REV
B		060-15559	4

FILE NAME 15559-6. 19

SHEET 19 OF 19

5-4-2004_9:11



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 021028-00	CW 11/4/02	RWH 11/6/02
		CAM 11/5/02	MAG 11/6/02
2	CHANGED SHEET 4 PER DCR 030320-00	CW 3/24/03	RWH 3/26/03
		CAM 3/25/03	MAG 3/27/03
3	CHANGED SHEETS 2 & 4 PER DCR 030821-00.	RWH 9/19/03	CW 11/17/03
		CAM 9/23/03	KB 9/26/03

NOTES

1 UNLESS OTHERWISE INDICATED, RESISTORS ARE 1/10W

2 UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%

3 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V

4 DIGITAL GROUND, ANALOG GROUND, CHASSIS GROUND, POWER GROUND

5 [XX/XX] DENOTES [SHEET NUMBER/SECTOR]

6 LAST REFERENCE DESIGNATORS USED: C15, D40, J5, Q4, R51, RP4, SW45, U2.

7 COMPONENTS MARKED WITH * ARE NOT ON BOM.

DOCUMENT CONTROL BLOCK: #060-15569

SHEET	REVISION	TITLE
1 OF 4	3	FRONT PANEL CONNECTORS
2 OF 4	2	FRONT PANEL CPLD
3 OF 4	1	FRONT PANEL SWITCH MATRIX
4 OF 4	3	FRONT PANEL LED MATRIX

REFERENCE COPY

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CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	7/10/02
CHECKED	CAM	7/8/02
Q.C.	ECM	7/10/02
ISSUED	MAG	7/8/02

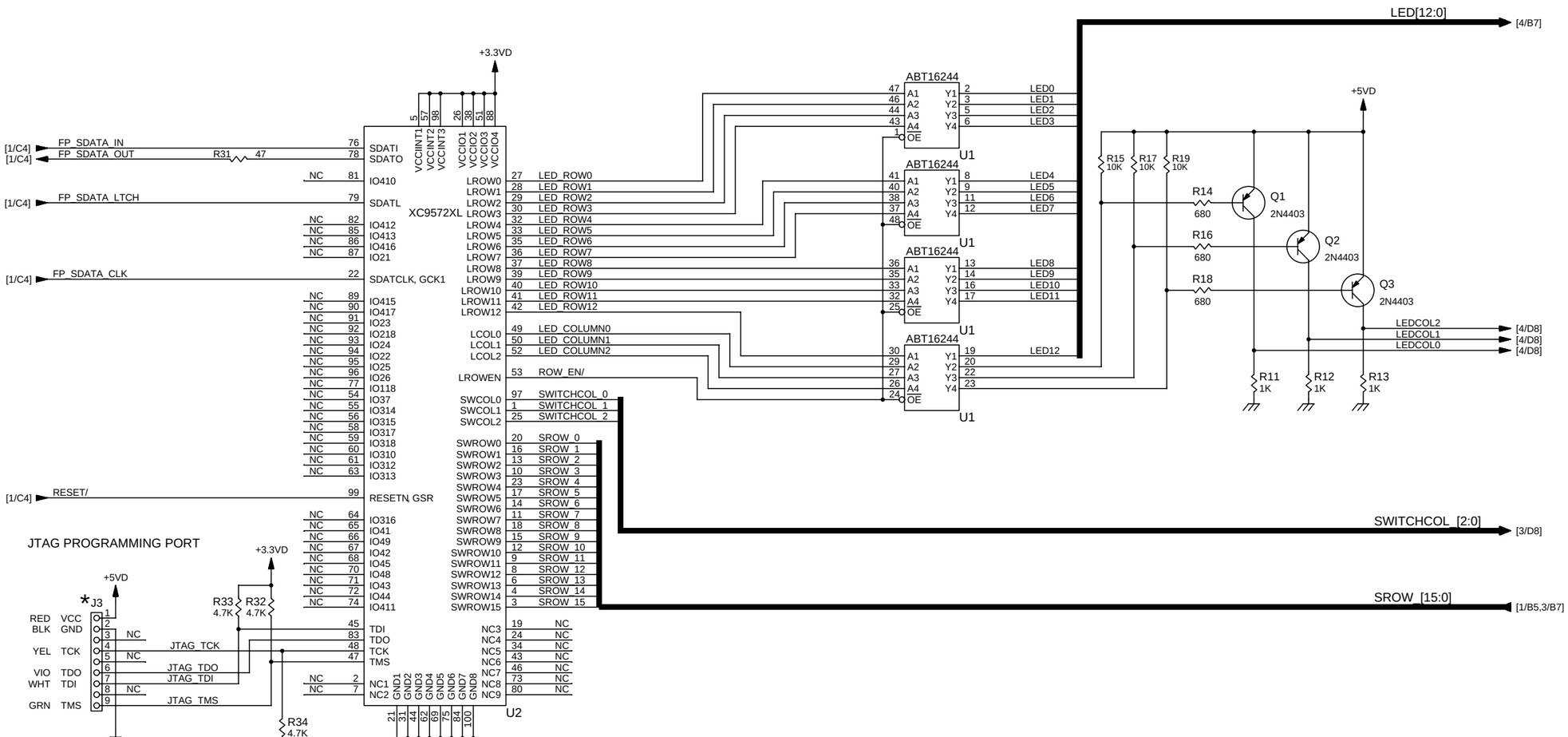
TITLE: SCHEM,SW/LED BD,RV8
FRONT PANEL CONNECTORS

SIZE	CODE	NUMBER	REV
B		060-15569	3

FILE NAME: 15569-3.1
SHEET 1 OF 4

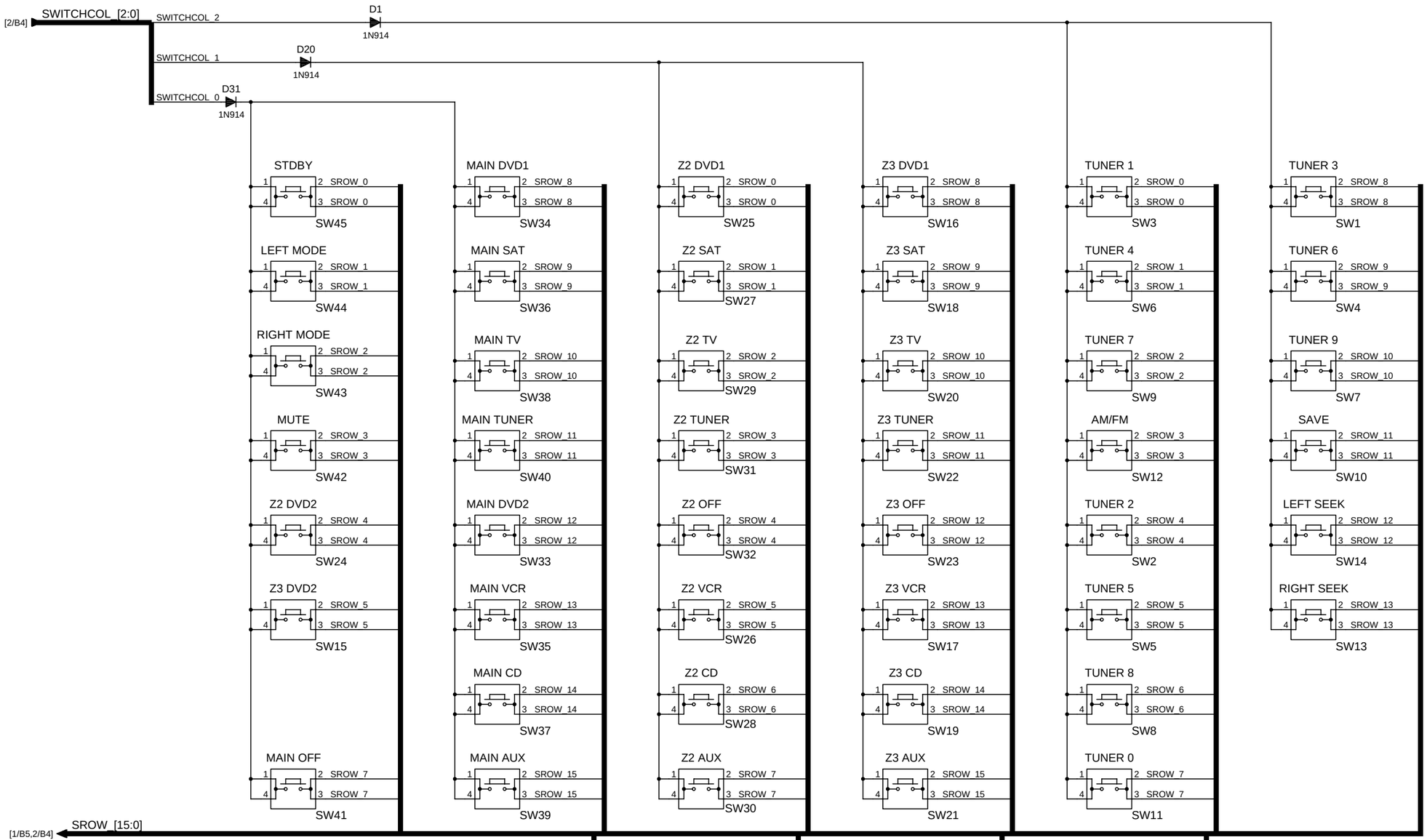
11-20-2003_17:06

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 021028-00	CW 11/4/02	RWH 11/6/02
		CAM 11/5/02	MAG 11/6/02
2	ADDED JTAG RES. PER DCR 030821-00.	RWH 9/19/03	CW 11/17/03
		CAM 9/23/03	KB 9/26/03



CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS		DATE	TITLE: SCHEM,SW/LED BD,RV8 FRONT PANEL CPLD
DRAWN	RWH	7/10/02	
CHECKED	CAM	7/8/02	SIZE B / CODE / NUMBER 060-15569 / REV 2
Q.C.	ECM	7/10/02	
ISSUED	MAG	7/8/02	FILE NAME 15569-3.2 / SHEET 2 OF 4

11-20-2003_17:07



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 021028-00	CW 11/4/02	RWH 11/6/02
		CAM 11/5/02	MAG 11/6/02

CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730

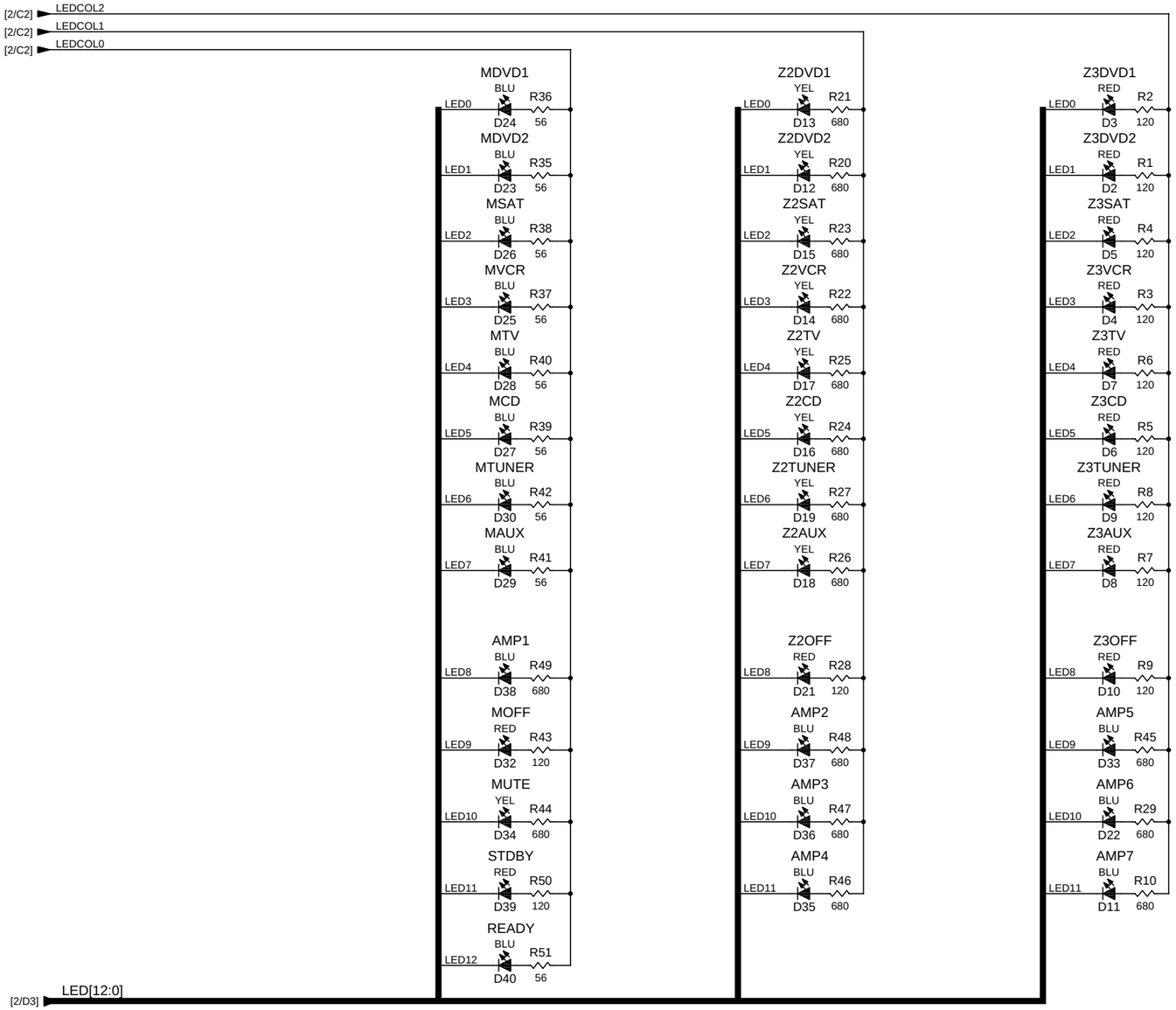
APPROVALS		DATE
DRAWN	RWH	7/10/02
CHECKED	CAM	7/8/02
Q.C.	ECM	7/10/02
ISSUED	MAG	7/8/02

TITLE: SCHEM,SW/LED BD,RV8
FRONT PANEL SWITCH MATRIX

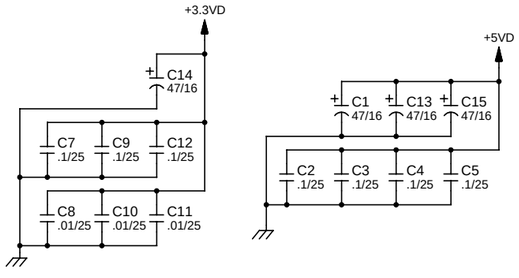
SIZE	CODE	NUMBER	REV
B		060-15569	1

FILE NAME: 15569-3.3
SHEET 3 OF 4

11-20-2003_17:07



BYPASS CAPACITORS



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 021028-00	CW 11/4/02	RWH 11/6/02
		CAM 11/5/02	MAG 11/6/02
2	CHANGED LED COLOR SCHEME PER DCR 030320-00	CW 3/24/03	RWH 3/26/03
		CAM 3/25/03	MAG 3/27/03
3	CHANGED RESISTORS PER DCR 030821-00.	RWH 9/19/03	CW 11/17/03
		CAM 9/23/03	KB 9/26/03

CONTRACT NO.

Lexicon

3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	7/10/02
CHECKED	CAM	7/8/02
Q.C.	ECM	7/10/02
ISSUED	MAG	7/8/02

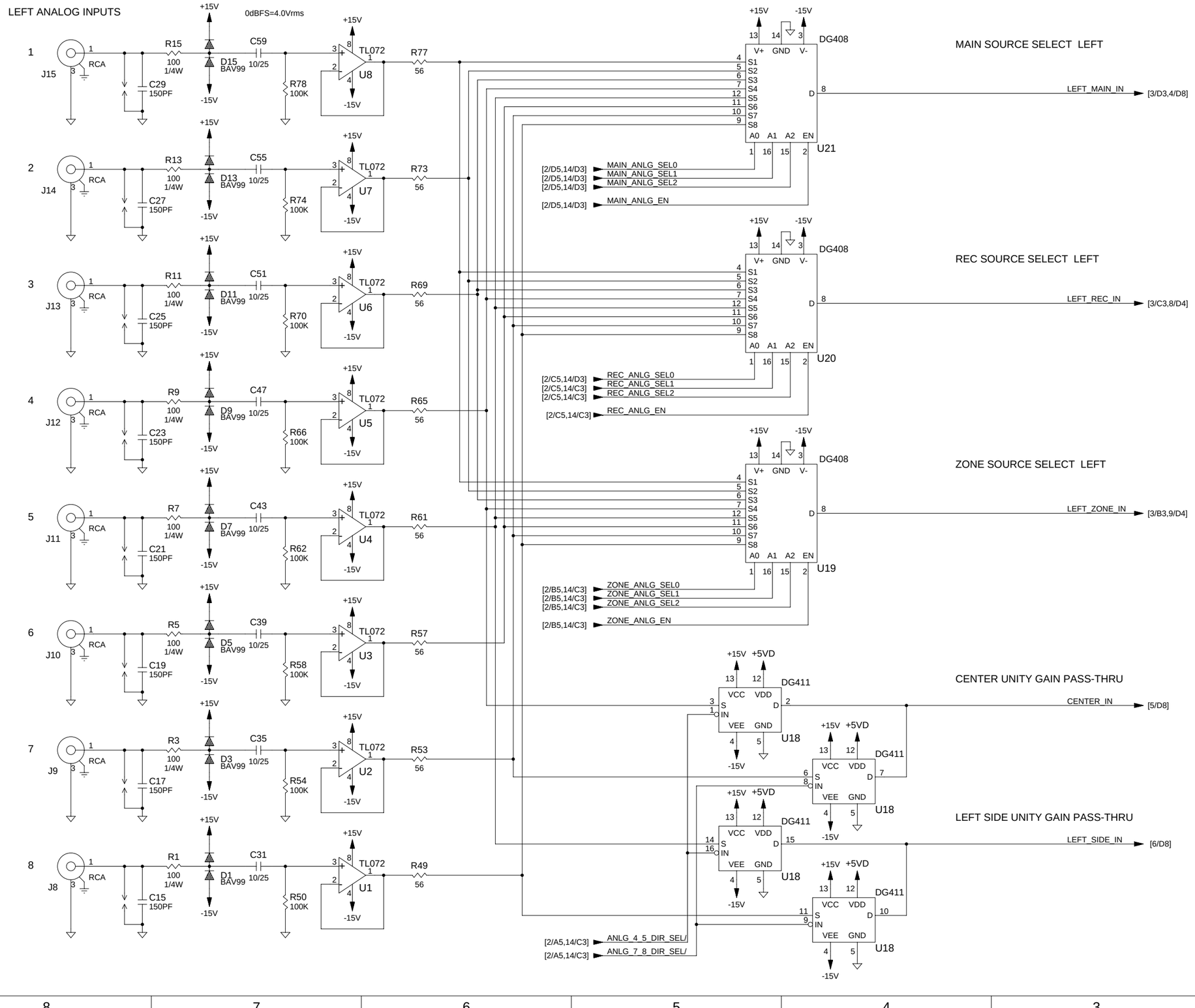
TITLE: SCHEM,SW/LED BD,RV8
FRONT PANEL LED MATRIX

SIZE	CODE	NUMBER	REV
B		060-15569	3

FILE NAME: 15569-3.4

SHEET 4 OF 4

11-20-2003_17:07



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 021107-00	RWH 11/14/02	CW 11/20/02
		CBV 11/20/02	MAG 11/21/02
2	CHANGED PER DCR 030407-00	RWH 5/21/03	CW 5/23/03
		CBV 5/23/03	MAG 5/23/03
3	CHANGED PER DCR 030729-00	RWH 9/29/03	CW 10/7/03
		CBV 10/6/03	MAG 10/7/03
4	CHANGED Sh. 6, 10-13, 15 PER DCR 031125-00	RWH 1/14/04	ECM 1/30/04
		CBV 1/30/04	MAG 2/2/04
5	CHANGED SH. 10-13 & 15 PER ECOS	RWH 4/14/04	CW 4/29/04
	040408-00 & 040421-00	CBV 4/28/04	KAB 5/2/04
6	CHANGED SHTS 10-13 PER ECO 040526-00	RWH 6/14/04	CW 6/16/04
		CBV 6/14/04	MAG 6/21/04

NOTES

1 UNLESS OTHERWISE INDICATED, RESISTORS ARE 1/10W

2 UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%

3 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V

4 DIGITAL GROUND, ANALOG GROUND, CHASSIS GROUND, POWER GROUND

5 [XX/XX] DENOTES [SHEET NUMBER/SECTOR]

6 LAST REFERENCE DESIGNATORS USED: C475, D36, E1, FB38, J27, Q3, R421, RY8, U96.

7 COMPONENTS MARKED WITH * ARE NOT ON BOM.

DOCUMENT CONTROL BLOCK: #060-15579

SHEET	REVISION	TITLE
1 OF 17	6	LEFT ANALOG INPUT MUXES
2 OF 17	3	RIGHT ANALOG INPUT MUXES
3 OF 17	3	MORE ANALOG INPUT MUXES
4 OF 17	3	INPUTS & MAIN A/D CONVERTER
5 OF 17	3	INPUTS & C/SUB A/D CONVERTER
6 OF 17	4	INPUTS & SIDE A/D CONVERTER
7 OF 17	3	REC A/D CONVERTER
8 OF 17	3	REC DAC & OUT LEVELS
9 OF 17	3	ZONE OUT LEVELS
10 OF 17	6	L/R FRONT DACS
11 OF 17	6	CENTER AND SUB DACS
12 OF 17	6	L/R SIDE DACS
13 OF 17	6	L/R REAR DACS
14 OF 17	3	CONTROL REGISTERS
15 OF 17	5	MAIN - AUX - AMP CONNS
16 OF 17	3	POWER SUPPLY & HEADPHONE
17 OF 17	3	BYPASS CAPACITORS

RELEASED COPY

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CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	8/27/02
CHECKED	CBV	8/28/02
Q.C.	CW	8/29/02
ISSUED	MAG	8/29/02

TITLE: SCHEM,ANALOG I/O BD,RV8
LEFT ANALOG INPUT MUXES

SIZE	CODE	NUMBER	REV
B		060-15579	6

FILE NAME: 15579-6.1
SHEET 1 OF 17

6-21-2004 14:22

RIGHT ANALOG INPUTS

0dBFS=4.0Vrms

1 J15 RCA — R16 100 1/4W — D16 BAV99 — C60 10/25 — R79 100K — TL072 U8 — R80 56

2 J14 RCA — R14 100 1/4W — D14 BAV99 — C56 10/25 — R75 100K — TL072 U7 — R76 56

3 J13 RCA — R12 100 1/4W — D12 BAV99 — C52 10/25 — R71 100K — TL072 U6 — R72 56

4 J12 RCA — R10 100 1/4W — D10 BAV99 — C48 10/25 — R67 100K — TL072 U5 — R68 56

5 J11 RCA — R8 100 1/4W — D8 BAV99 — C44 10/25 — R63 100K — TL072 U4 — R64 56

6 J10 RCA — R6 100 1/4W — D6 BAV99 — C40 10/25 — R59 100K — TL072 U3 — R60 56

7 J9 RCA — R4 100 1/4W — D4 BAV99 — C36 10/25 — R55 100K — TL072 U2 — R56 56

8 J8 RCA — R2 100 1/4W — D2 BAV99 — C32 10/25 — R51 100K — TL072 U1 — R52 56

MAIN SOURCE SELECT RIGHT

DG408 U12: S1–S8 ← MAIN_ANLG_SEL0 [1/D5,14/D3], MAIN_ANLG_SEL1 [1/D5,14/D3], MAIN_ANLG_SEL2 [1/D5,14/D3], MAIN_ANLG_EN [1/D5,14/D3]; D → RIGHT_MAIN_IN [3/D3,4/D8]

REC SOURCE SELECT RIGHT

DG408 U11: S1–S8 ← REC_ANLG_SEL0 [1/C5,14/D3], REC_ANLG_SEL1 [1/C5,14/C3], REC_ANLG_SEL2 [1/C5,14/C3], REC_ANLG_EN [1/C5,14/C3]; D → RIGHT_REC_IN [3/B3,8/C4]

ZONE SOURCE SELECT RIGHT

DG408 U10: S1–S8 ← ZONE_ANLG_SEL0 [1/B5,14/C3], ZONE_ANLG_SEL1 [1/B5,14/C3], ZONE_ANLG_SEL2 [1/B5,14/C3], ZONE_ANLG_EN [1/B5,14/C3]; D → RIGHT_ZONE_IN [3/A3,9/C4]

SUB UNITY GAIN PASS-THRU

DG411 U9: SUB_IN → [5/C8]

RIGHT SIDE UNITY GAIN PASS-THRU

DG411 U9: RIGHT_SIDE_IN → [6/D8]

DG411 U9: ANLG_4_5_DIR_SEL/ [1/A5,14/C3], ANLG_7_8_DIR_SEL/ [1/A5,14/C3]

REVISIONS

REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 021107-00	RWH 11/14/02	CW 11/20/02
		CBV 11/20/02	MAG 11/21/02
2	CHANGED PER DCR 030407-00	RWH 5/21/03	CW 5/23/03
		CBV 5/23/03	MAG 5/23/03
3	CHANGED PER DCR 030729-00	RWH 9/29/03	CW 10/7/03
		CBV 10/6/03	MAG 10/7/03

CONTRACT NO.

Lexicon 3 OAK PARK BEDFORD, MA 01730

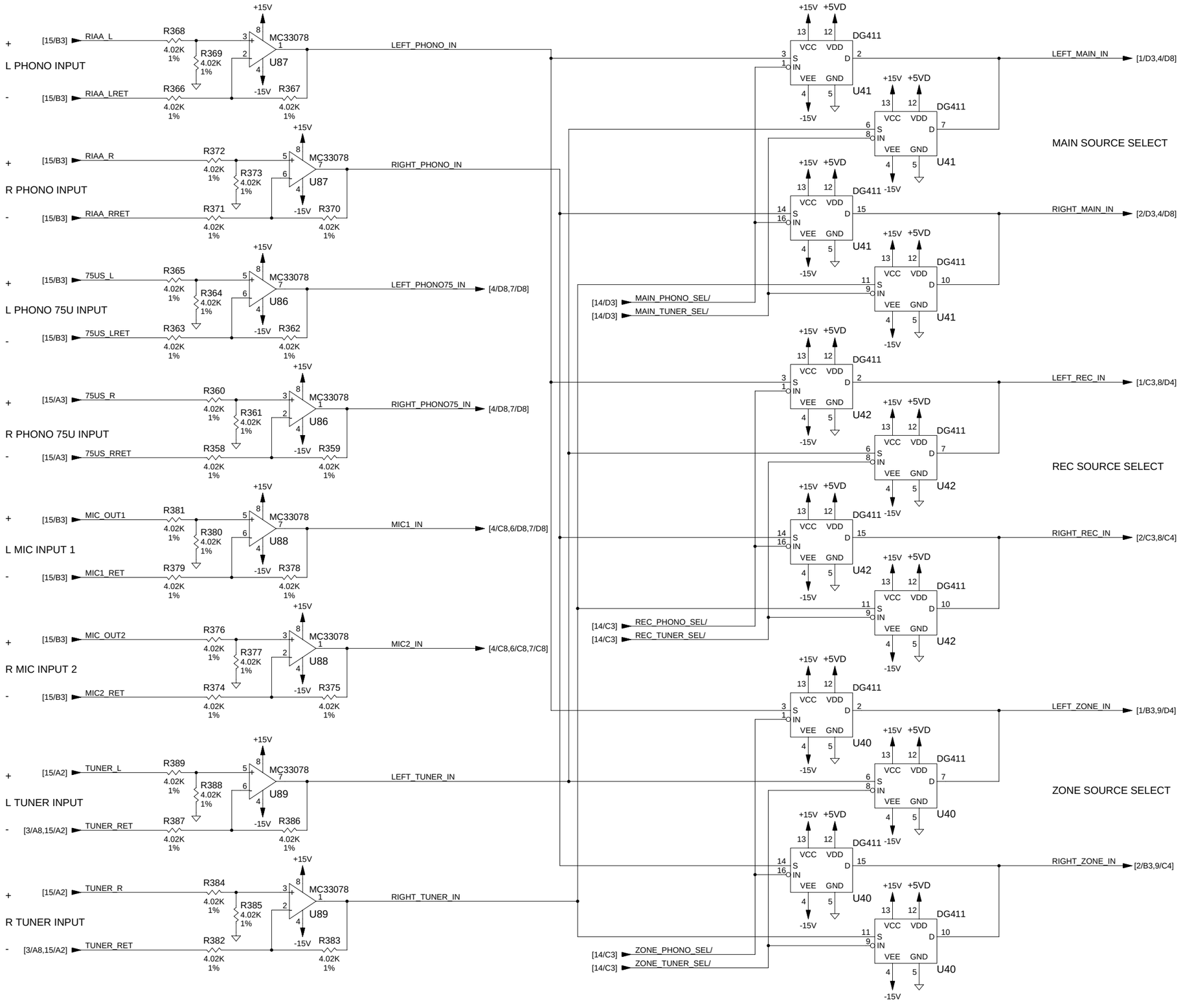
APPROVALS		DATE
DRAWN	RWH	8/27/02
CHECKED	CBV	8/28/02
Q.C.	CW	8/29/02
ISSUED	MAG	8/29/02

TITLE: SCHEM,ANALOG I/O BD,RV8
RIGHT ANALOG INPUT MUXES

SIZE	CODE	NUMBER	REV
B		060-15579	3

FILE NAME: 15579-6.2 SHEET 2 OF 17

10-7-2003 11:05



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 021107-00	RWH 11/14/02	CW 11/20/02
		CBV 11/20/02	MAG 11/21/02
2	CHANGED PER DCR 030407-00	RWH 5/21/03	CW 5/23/03
		CBV 5/23/03	MAG 5/23/03
3	CHANGED PER DCR 030729-00	RWH 9/29/03	CW 10/7/03
		CBV 10/6/03	MAG 10/7/03

CONTRACT NO.	lexicon	3 OAK PARK BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	8/27/02
CHECKED	CBV	8/28/02
Q.C.	CW	8/29/02
ISSUED	MAG	8/29/02

TITLE: SCHEM,ANALOG I/O BD,RV8
MORE ANALOG INPUT MUXES

SIZE	CODE	NUMBER	REV
B		060-15579	3

FILE NAME: 15579-6.3
SHEET 3 OF 17

10-7-2003 11:05

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 021107-00	RWH 11/14/02	CW 11/20/02
		CBV 11/20/02	MAG 11/21/02
2	CHANGED PER DCR 030407-00	RWH 5/21/03	CW 5/23/03
		CBV 5/23/03	MAG 5/23/03
3	CHANGED PER DCR 030729-00	RWH 9/29/03	CW 10/7/03
		CBV 10/6/03	MAG 10/7/03

MAIN INPUT LEVEL CONTROL

0dBFS=2.0Vrms

[1/D3,3/D3] LEFT_MAIN_IN
[2/D3,3/D3] RIGHT_MAIN_IN
[3/C6,7/D8] LEFT_PHONO75_IN
[3/C6,7/D8] RIGHT_PHONO75_IN
[3/B6,6/D8,7/D8] MIC1_IN
[3/B6,6/C8,7/C8] MIC2_IN
[14/D3] MAIN_PHONO75_SEL/
[14/D3] MAIN_MIC_SEL/

PHONO 75U INPUT
MIC INPUT

DG411 U50

MC33078 U57

R254 1.00K 1%
R255 1.00K 1%
R256 100K
R257 1.00K 1%
R258 100K
R259 1.00K 1%

PGA2311 U67

C342 .1/25
C343 4.7
C345 .1/25
C346 4.7
C340 4.7
C341 .1/25
R275 10
R276 100K

[5/D5,6/D4,7/B7,8/B6,9/B6,10/C7,11/C7,12/C7,13/C7,14/B5,15/C5] ADA_SCLK
[8/C7,10/C7,11/C7,12/C7,13/C7,14/B5,15/A5,15/C5] ADA_SDATA_OUT
[5/D5,6/C4,7/A7,8/B7,9/C7,9/B7,14/B5,15/C5] ADA_VC_SEL/
[5/C5,6/C4,7/A7,9/C7,14/B3] MAIN_VC_ZCEN
[5/C5,6/C4,7/A7,8/B7,9/C7,9/B7,14/B3] VC_MUTE/

MAL
LEFT_MAIN_IN_LVL [4/B8,10/D5]
MAR
RIGHT_MAIN_IN_LVL [4/A8,10/B5]
VC_0 [5/D5]

MAIN A/D CONVERTER

-7dB
0dBFS=2.0Vrms
0dBFS=0.884Vrms

C363 100PF
R291 2.49K 1%
R336 2.00K 1%
C390 100PF
R337 2.00K 1%
R338 51 1/4W
C436 2200PF
C344 47/16
R274 5.62K 1%
[4/D2,10/D5] LEFT_MAIN_IN_LVL
U71 MC33078
R290 51 1/4W
R334 10.0K 1%
C367 10/16
C389 .1/25
R335 10.0K 1%
C391 100PF
R340 2.00K 1%
C365 100PF
R292 2.49K 1%
R339 2.00K 1%
R341 51 1/4W
C437 2200PF
C347 47/16
R277 5.62K 1%
[4/C2,10/B5] RIGHT_MAIN_IN_LVL
R293 51 1/4W
U80 MC33078

+5VA +3.3VD
C446 4.7
C447 .1/25
C441 4.7
C442 .1/25
R356 0
R355 * NC
R354 NC

PCM1804 U84

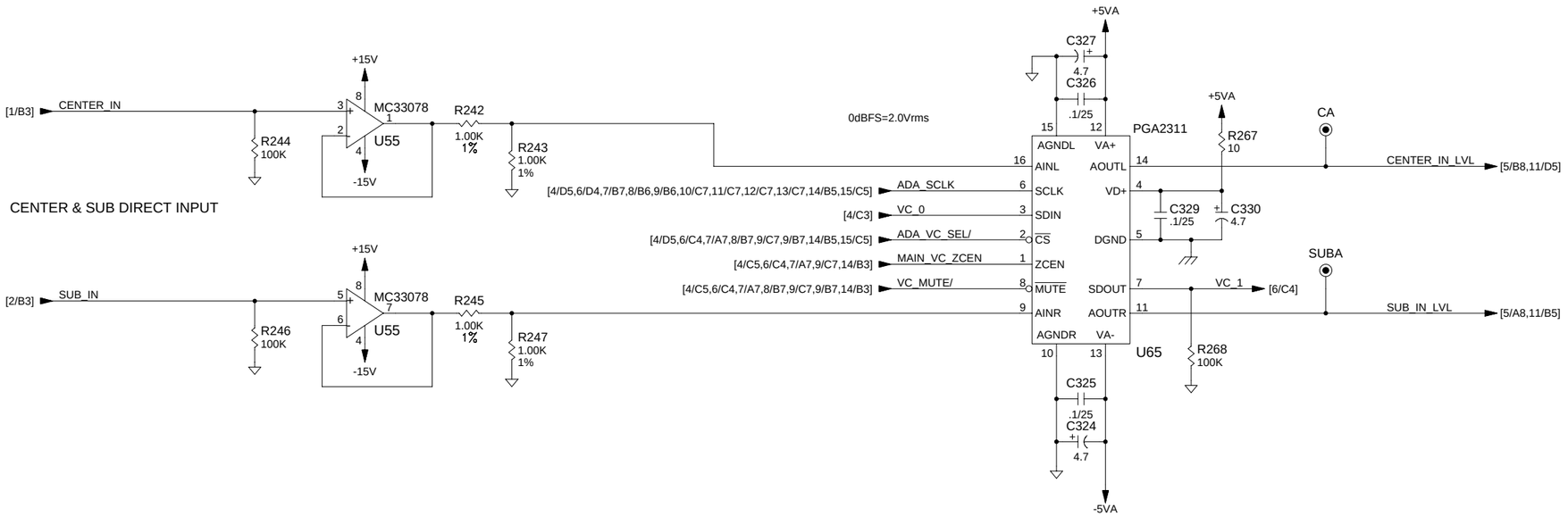
C439 4.7
C438 .1/25
C440 .1/25
C445 .1/25
C443 4.7
C444 .1/25

MAIN_ADC_192K_EN [5/B4,6/A4,14/B3]
MAIN_ADC_96K_EN [5/B4,6/A4,14/B3]
R357 47
MAIN_I2S_IN1 [15/B5,15/D6]
MAIN_FS/ [5/A4,6/A4,10/C7,11/C7,12/C7,13/C7,15/C3,15/C5]
MAIN_FS64/ [5/A4,6/A4,10/C7,11/D7,12/D7,13/D7,15/B3,15/D5]
MAIN_ADC_MCKI [15/D3]
MAIN_ADC_RST/ [5/A4,6/A4,14/B3]

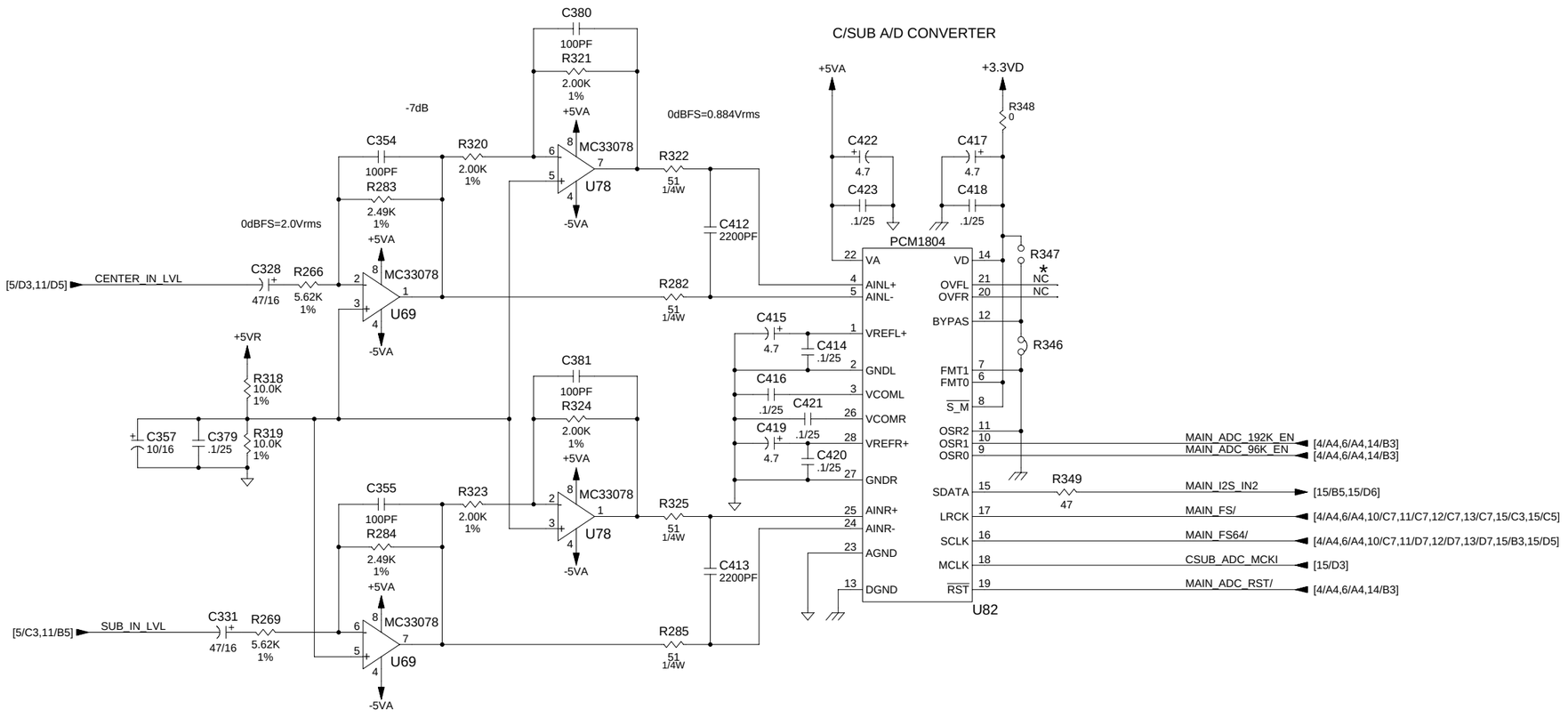
CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS	DATE	TITLE: SCHEM,ANALOG I/O BD,RV8 INPUTS & MAIN A/D CONVERTER	
DRAWN RWH	8/27/02		
CHECKED CBV	8/28/02	SIZE B / CODE / NUMBER 060-15579 / REV 3	
Q.C. CW	8/29/02		
ISSUED MAG	8/29/02	FILE NAME 15579-6.4	SHEET 4 OF 17

10-7-2003_11:05

C/SUB INPUT LEVEL CONTROL



C/SUB A/D CONVERTER



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 021107-00	RWH 11/14/02	CW 11/20/02
		CBV 11/20/02	MAG 11/21/02
2	CHANGED PER DCR 030407-00	RWH 5/21/03	CW 5/23/03
		CBV 5/23/03	MAG 5/23/03
3	CHANGED PER DCR 030729-00	RWH 9/29/03	CW 10/7/03
		CBV 10/6/03	MAG 10/7/03

CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	8/27/02
CHECKED	CBV	8/28/02
Q.C.	CW	8/29/02
ISSUED	MAG	8/29/02

TITLE
SCHEM,ANALOG I/O BD,RV8
INPUTS & C/SUB A/D CONVERTER

SIZE	CODE	NUMBER	REV
B		060-15579	3

FILE NAME 15579-6.5
SHEET 5 OF 17

10-7-2003_11:05

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 021107-00	RWH 11/14/02	CW 11/20/02
		CBV 11/20/02	MAG 11/21/02
2	CHANGED PER DCR 030407-00	RWH 5/21/03	CW 5/23/03
		CBV 5/23/03	MAG 5/23/03
3	CHANGED PER DCR 030729-00	RWH 9/29/03	CW 10/7/03
		CBV 10/6/03	MAG 10/7/03
4	CHANGED PER DCR 031125-00	RWH 1/14/04	ECM 1/30/04
		CBV 1/30/04	MAG 2/2/04

MIC INPUT

SIDE INPUT LEVEL CONTROL

SIDE A/D CONVERTER

CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS		DATE	TITLE: SCHEM,ANALOG I/O BD,RV8 INPUTS & SIDE A/D CONVERTER
DRAWN	RWH	8/27/02	
CHECKED	CBV	8/28/02	SIZE: B; CODE: ; NUMBER: 060-15579; REV: 4
Q.C.	CW	8/29/02	
ISSUED	MAG	8/29/02	FILE NAME: 15579-6.6; SHEET 6 OF 17

2-2-2004_11:13

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 021107-00	RWH 11/14/02	CW 11/20/02
		CBV 11/20/02	MAG 11/21/02
2	CHANGED PER DCR 030407-00	RWH 5/21/03	CW 5/23/03
		CBV 5/23/03	MAG 5/23/03
3	CHANGED PER DCR 030729-00	RWH 9/29/03	CW 10/7/03
		CBV 10/6/03	MAG 10/7/03

PHONO 75U INPUT

MIC INPUT

REC_DAC_OUT

REC INPUT LEVEL CONTROL

REC A/D CONVERTER

CONTRACT NO.	Lexicon 3 OAK PARK BEDFORD, MA 01730
TITLE	SCHEM,ANALOG I/O BD,RV8 REC A/D CONVERTER
SIZE	B
CODE	
NUMBER	060-15579
REV	3
FILE NAME	15579-6.7
SHEET	7 OF 17

APPROVALS		DATE
DRAWN	RWH	8/27/02
CHECKED	CBV	8/28/02
Q.C.	CW	8/29/02
ISSUED	MAG	8/29/02

10-7-2003_11:05

REC D/A CONVERSION

REC OUTPUT LEVEL CONTROL

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 021107-00	RWH 11/14/02	CW 11/20/02
		CBV 11/20/02	MAG 11/21/02
2	CHANGED PER DCR 030407-00	RWH 5/21/03	CW 5/23/03
		CBV 5/23/03	MAG 5/23/03
3	CHANGED PER DCR 030729-00	RWH 9/29/03	CW 10/7/03
		CBV 10/6/03	MAG 10/7/03

CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	8/27/02
CHECKED	CBV	8/28/02
Q.C.	CW	8/29/02
ISSUED	MAG	8/29/02

TITLE: SCHEM,ANALOG I/O BD,RV8
REC DAC & OUT LEVELS

SIZE	CODE	NUMBER	REV
B		060-15579	3

FILE NAME: 15579-6.8 SHEET 8 OF 17

10-7-2003_11:05

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 021107-00	RWH 11/14/02	CW 11/20/02
		CBV 11/20/02	MAG 11/21/02
2	CHANGED PER DCR 030407-00	RWH 5/21/03	CW 5/23/03
		CBV 5/23/03	MAG 5/23/03
3	CHANGED PER DCR 030729-00	RWH 9/29/03	CW 10/7/03
		CBV 10/6/03	MAG 10/7/03

REAR OUTPUT
LEVEL CONTROL

0dBFS=4.3Vrms

[6/D2] LEFT_SIDE_IN_HALF
[8/B5] VC_4
[4/D5,5/D5,6/C4,7/A7,8/B7,9/B7,14/B5,15/C5] ADA_VC_SEL/
[4/C5,5/C5,6/C4,7/A7,8/B7,9/B7,14/B3] MAIN_VC_ZCEN
[4/C5,5/C5,6/C4,7/A7,8/B7,9/B7,14/B3] VC_MUTE/
[6/D2] RIGHT_SIDE_IN_HALF

PGA2311 U63
AGNDL VA+ AINL AOUTL SCLK VD+ SDIN CS DGND ZCEN MUTE SDOUT AINR AOUTR AGNDR VA-

C312 4.7, C313 .1/25, C310 .1/25, C311 4.7, C314 .1/25, C315 4.7
R260 10, R261 100K
+5VA, -5VA

LEFT_REAR_IN_LVL [13/D5]
VC_5 [9/B7]
RIGHT_REAR_IN_LVL [13/B5]

[8/D4] L_REC_DAC
[1/B3,3/B3] LEFT_ZONE_IN
[14/C7,14/C3] ZONE_DACOUT_SEL/
[14/C6] ZONE_DIRECT_SEL/
[8/C4] R_REC_DAC
[2/B3,3/A3] RIGHT_ZONE_IN

DG411 U44
VCC VDD S D IN VEE GND
+15V +5VD -15V

L_ZONE_DACOUT [9/B7]
R_ZONE_DACOUT [9/A7]

ZONE OUTPUT
LEVEL CONTROL

[9/D3] L_ZONE_DACOUT
[4/D5,5/D5,6/D4,7/B7,8/B6,10/C7,11/C7,12/C7,13/C7,14/B5,15/C5] ADA_SCLK
[9/C5] VC_5
[4/D5,5/D5,6/C4,7/A7,8/B7,9/C7,14/B5,15/C5] ADA_VC_SEL/
[14/B3] ZONE_VC_ZCEN
[4/C5,5/C5,6/C4,7/A7,8/B7,9/C7,14/B3] VC_MUTE/
[9/C3] R_ZONE_DACOUT

MC33078 U33
R131 1.00K 1%, R132 100K, R130 1.00K 1%, C125 10/25
R134 1.00K 1%, R135 100K, R133 1.00K 1%, C126 10/25

PGA2311 U23
C121 4.7, C122 .1/25, C124 .1/25, C123 4.7, C119 .1/25, C120 4.7
R114 10

MC33078 U15
C67 47/25, C93 18PF, R89 4.02K 1%, R88 4.02K 1%, R29 10K
C68 47/25, C96 18PF, R91 4.02K 1%, R90 4.02K 1%, R30 10K

RELAY RY3
[8/A4] ZONE_RLY_CNTL

R28 120 L_ZONE_AMP [15/A8,16/C8]
R32 120 R_ZONE_AMP [15/A8,16/B8]

0dBFS=4Vrms

R27 330 1/4W FB5 C5 150PF J3 RCA ZONE3 LEFT OUT
R31 330 1/4W FB6 C6 150PF J3 RCA ZONE3 RIGHT OUT

CONTRACT NO.	Lexicon 3 OAK PARK BEDFORD, MA 01730	
APPROVALS	DATE	TITLE: SCHEM,ANALOG I/O BD,RV8 ZONE OUT LEVELS
DRAWN RWH	8/27/02	SIZE B | CODE | NUMBER 060-15579 | REV 3
CHECKED CBV	8/28/02	
Q.C. CW	8/29/02	
ISSUED MAG	8/29/02	FILE NAME 15579-6.9 SHEET 9 OF 17

10-7-2003 11:05

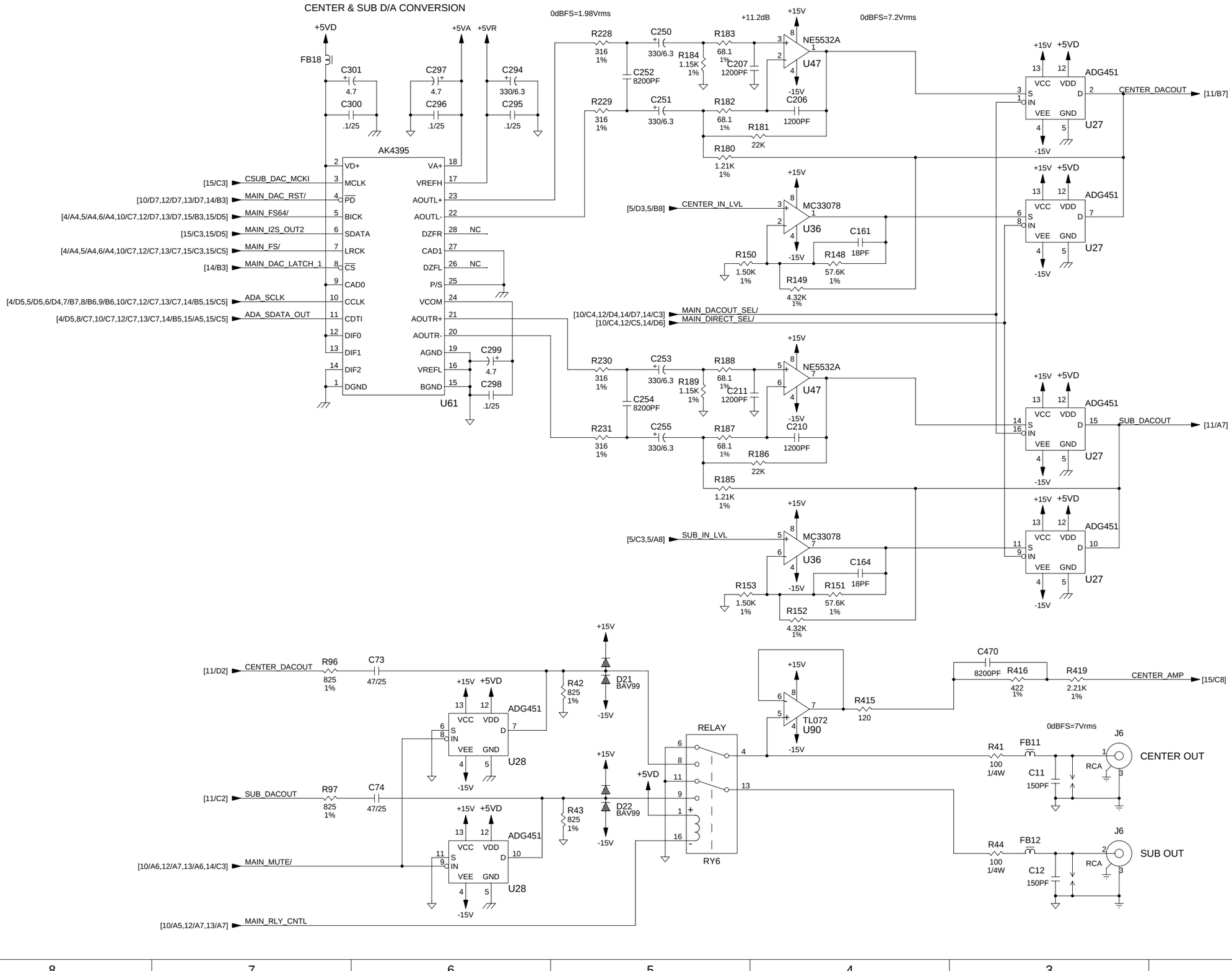
LEFT & RIGHT FRONT D/A CONVERSION

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 021107-00	RWH 11/14/02	CW 11/20/02
		CBV 11/20/02	MAG 11/21/02
2	CHANGED PER DCR 030407-00	RWH 5/21/03	CW 5/23/03
		CBV 5/23/03	MAG 5/23/03
3	CHANGED PER DCR 030729-00	RWH 9/29/03	CW 10/7/03
		CBV 10/6/03	MAG 10/7/03
4	CHANGED PER DCR 031125-00	RWH 1/14/04	ECM 1/30/04
		CBV 1/30/04	MAG 2/2/04
5	CHANGED R45-48, R99-100 PER ECO 040408-00	RWH 4/27/04	CW 4/29/04
		CBV 4/28/04	KAB 5/2/04
6	CHANGED U29 PER ECO 040526-00	RWH 6/14/04	CW 6/16/04
		CBV 6/14/04	MAG 6/21/04

CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS		DATE	TITLE: SCHEM,ANALOG I/O BD,RV8 L/R FRONT DACS
DRAWN	RWH	8/27/02	
CHECKED	CBV	8/28/02	SIZE: B; CODE: ; NUMBER: 060-15579; REV: 6
Q.C.	CW	8/29/02	
ISSUED	MAG	8/29/02	FILE NAME: 15579-6.10; SHEET 10 OF 17

6-21-2004_14:22

CENTER & SUB D/A CONVERSION



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 021107-00	RWH 11/14/02	CW 11/20/02
		CBV 11/20/02	MAG 11/21/02
2	CHANGED PER DCR 030407-00	RWH 5/21/03	CW 5/23/03
		CBV 5/23/03	MAG 5/23/03
3	CHANGED PER DCR 030729-00	RWH 9/29/03	CW 10/7/03
		CBV 10/6/03	MAG 10/7/03
4	CHANGED PER DCR 031125-00	RWH 1/14/04	ECM 1/30/04
		CBV 1/30/04	MAG 2/2/04
5	CHANGED R41-44, R96-97 PER ECO 040408-00	RWH 4/27/04	CW 4/29/04
		CBV 4/28/04	KAB 5/2/04
6	CHANGED U27 PER ECO 040526-00	RWH 6/14/04	CW 6/16/04
		CBV 6/14/04	MAG 6/21/04

CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	8/27/02
CHECKED	CBV	8/28/02
Q.C.	CW	8/29/02
ISSUED	MAG	8/29/02

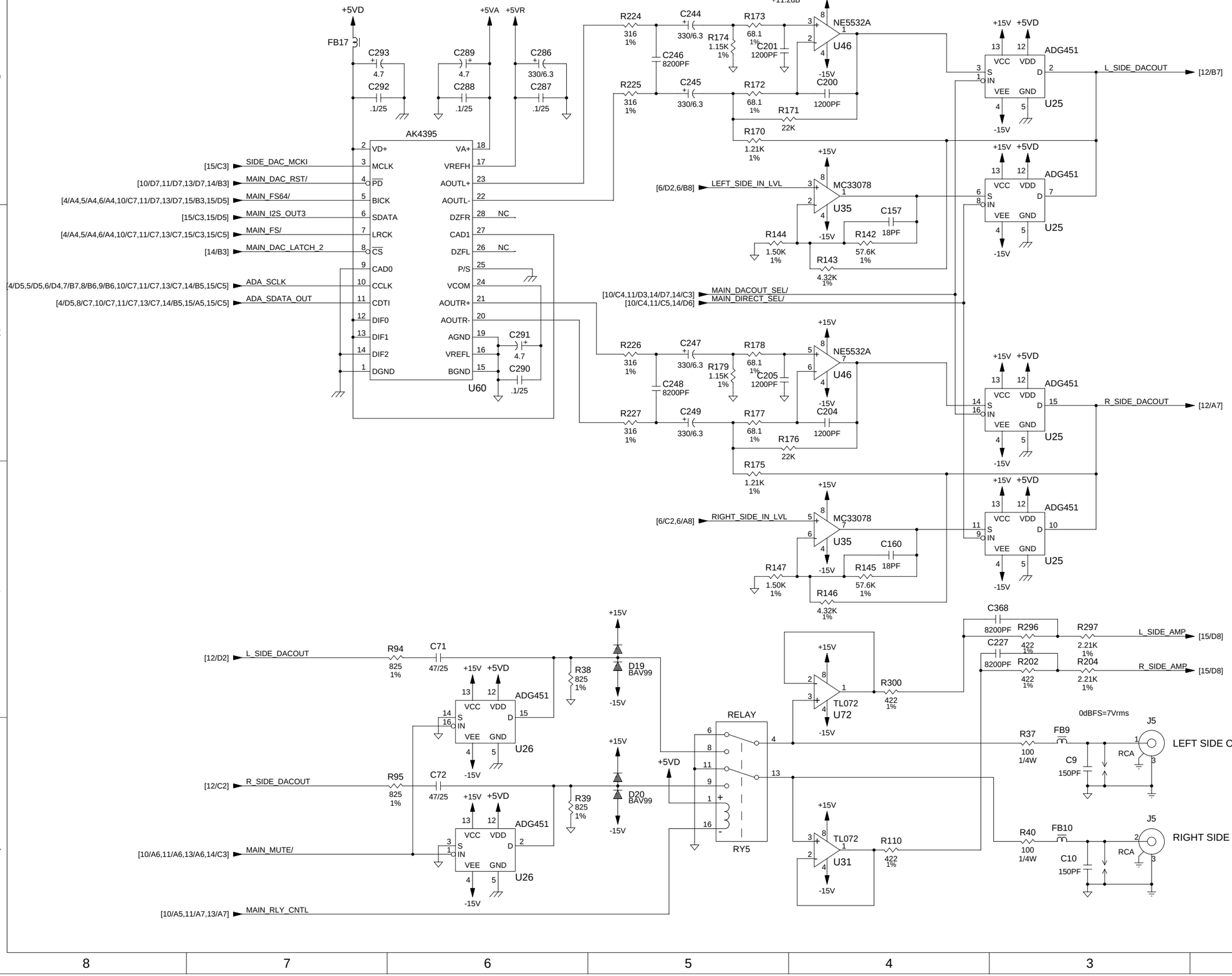
TITLE
SCHEM,ANALOG I/O BD,RV8
CENTER AND SUB DACS

SIZE	CODE	NUMBER	REV
B		060-15579	6

FILE NAME 15579-6.11 SHEET 11 OF 17

6-21-2004_14:23

LEFT & RIGHT SIDE D/A CONVERSION



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 021107-00	RWH 11/14/02	CW 11/20/02
		CBV 11/20/02	MAG 11/21/02
2	CHANGED PER DCR 030407-00	RWH 5/21/03	CW 5/23/03
		CBV 5/23/03	MAG 5/23/03
3	CHANGED PER DCR 030729-00	RWH 9/29/03	CW 10/7/03
		CBV 10/6/03	MAG 10/7/03
4	CHANGED PER DCR 031125-00	RWH 1/14/04	ECM 1/30/04
		CBV 1/30/04	MAG 2/2/04
5	CHANGED R37-40, R94-95 PER ECO 040408-00	RWH 4/27/04	CW 4/29/04
		CBV 4/28/04	KAB 5/2/04
6	CHANGED U25 PER ECO 040526-00	RWH 6/14/04	CW 6/16/04
		CBV 6/14/04	MAG 6/21/04

CONTRACT NO.

lexicon
3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	8/27/02
CHECKED	CBV	8/28/02
Q.C.	CW	8/29/02
ISSUED	MAG	8/29/02

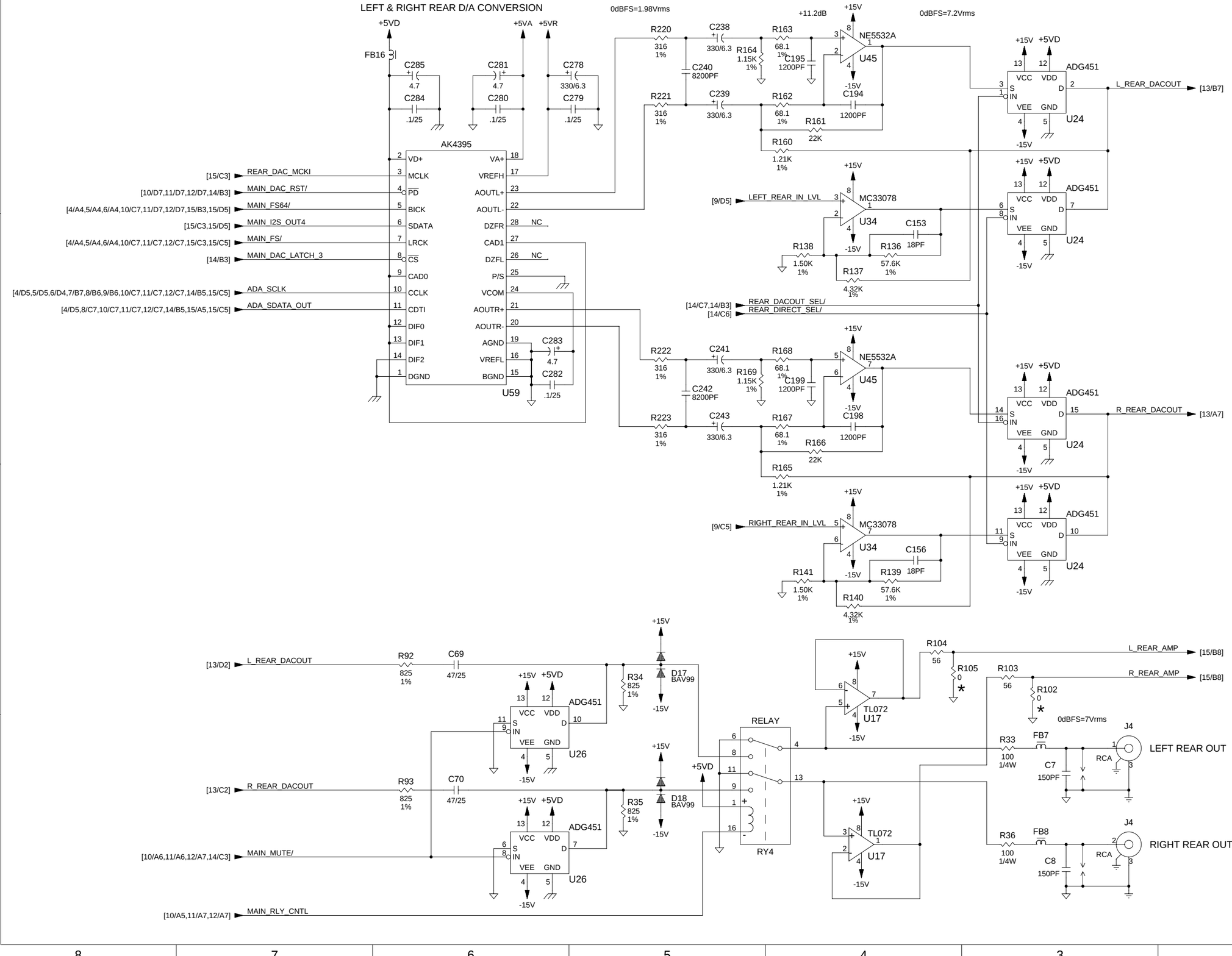
TITLE: SCHEM,ANALOG I/O BD,RV8
L/R SIDE DACS

SIZE	CODE	NUMBER	REV
B		060-15579	6

FILE NAME: 15579-6.12
SHEET 12 OF 17

6-21-2004_14:23

LEFT & RIGHT REAR D/A CONVERSION



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 021107-00	RWH 11/14/02	CW 11/20/02
		CBV 11/20/02	MAG 11/21/02
2	CHANGED PER DCR 030407-00	RWH 5/21/03	CW 5/23/03
		CBV 5/23/03	MAG 5/23/03
3	CHANGED PER DCR 030729-00	RWH 9/29/03	CW 10/7/03
		CBV 10/6/03	MAG 10/7/03
4	CHANGED PER DCR 031125-00	RWH 1/14/04	ECM 1/30/04
		CBV 1/30/04	MAG 2/2/04
5	CHANGED R33-36, R92-93 PER ECO 040408-00	RWH 4/27/04	CW 4/29/04
	CHANGED R102-105 PER ECO 040421-00	CBV 4/28/04	KAB 5/2/04
6	CHANGED U24 PER ECO 040526-00	RWH 6/14/04	CW 6/16/04
		CBV 6/14/04	MAG 6/21/04

CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	8/27/02
CHECKED	CBV	8/28/02
Q.C.	CW	8/29/02
ISSUED	MAG	8/29/02

TITLE
SCHEM,ANALOG I/O BD,RV8
L/R REAR DACS

SIZE	CODE	NUMBER	REV
B		060-15579	6

FILE NAME 15579-6.13
SHEET 13 OF 17

6-21-2004_14:23

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 021107-00	RWH 11/14/02	CW 11/20/02
		CBV 11/20/02	MAG 11/21/02
2	CHANGED PER DCR 030407-00	RWH 5/21/03	CW 5/23/03
		CBV 5/23/03	MAG 5/23/03
3	CHANGED PER DCR 030729-00	RWH 9/29/03	CW 10/7/03
		CBV 10/6/03	MAG 10/7/03

+3.3VD

U53 74VHC04

[10/C4,11/D3,12/D4,14/C3] MAIN_DACOUT_SEL/ 1 → 2 MAIN_DIRECT_SEL/ → [10/C4,11/C5,12/C5]

[8/D4,14/C3] REC_DACOUT_SEL/ 3 → 4 REC_DIRECT_SEL/ → [8/D4]

[9/C4,14/C3] ZONE_DACOUT_SEL/ 5 → 6 ZONE_DIRECT_SEL/ → [9/C4]

[13/C5,14/B3] REAR_DACOUT_SEL/ 11 → 10 REAR_DIRECT_SEL/ → [13/C5]

XC9572XL

+3.3VD → VCCIO1 (26), VCCIO2 (38), VCCIO3 (51), VCCIO4 (88)

+3.3VD → VCCINT1 (5), VCCINT2 (57), VCCINT3 (98)

NC (2, 7, 19, 24, 34, 43, 46, 73, 80)

O__0_0	1	MAIN_ANLG_SEL0	[1/D5,2/D5]
O__0_1	6	MAIN_ANLG_SEL1	[1/D5,2/D5]
O__0_2	8	MAIN_ANLG_SEL2	[1/D5,2/D5]
O__0_3	9	MAIN_ANLG_EN	[1/D5,2/D5]
O__0_4	10	MAIN_PHONO_SEL/	[3/C5]
O__0_5	11	MAIN_TUNER_SEL/	[3/C5]
O__0_6	12	MAIN_PHONO75_SEL/	[4/C8]
O__0_7	13	MAIN_MIC_SEL/	[4/C8]
O__1_0	14	REC_ANLG_SEL0	[1/C5,2/C5]
O__1_1	15	REC_ANLG_SEL1	[1/C5,2/C5]
O__1_2	16	REC_ANLG_SEL2	[1/C5,2/C5]
O__1_3	17	REC_ANLG_EN	[1/C5,2/C5]
O__1_4	18	REC_PHONO_SEL/	[3/B5]
O__1_5	20	REC_TUNER_SEL/	[3/B5]
O__1_6	25	REC_AD_DAC_SEL/	[7/C8]
O__1_7	28	REC_AMP_SEL/	[15/A8]
O__2_0	29	ZONE_ANLG_SEL0	[1/B5,2/B5]
O__2_1	30	ZONE_ANLG_SEL1	[1/B5,2/B5]
O__2_2	32	ZONE_ANLG_SEL2	[1/B5,2/B5]
O__2_3	33	ZONE_ANLG_EN	[1/B5,2/B5]
O__2_4	35	ZONE_PHONO_SEL/	[3/A5]
O__2_5	36	ZONE_TUNER_SEL/	[3/A5]
O__2_6	37	ZONE_AMP_SEL/	[15/A8]
O__2_7	39	REAR_AMP_SEL/	[15/A8]
O__3_0	40	HEADP_FRONT_SEL/	[16/A8]
O__3_1	41	HEADP_REC_SEL/	[16/A8]
O__3_2	42	HEADP_ZONE_SEL/	[16/A8]
O__3_3	49	ANLG_4_5_DIR_SEL/	[1/A5,2/A5]
O__3_4	50	ANLG_7_8_DIR_SEL/	[1/A5,2/A5]
O__3_5	52	REC_AD_PHO75_SEL/	[7/C8]
O__3_6	53	SIDE_MIC_SEL/	[6/C8]
O__3_7	54	MAIN_MUTE/	[10/A6,11/A6,12/A7,13/A6]
O__4_0	55	MAIN_DACOUT_SEL/	[10/C4,11/D3,12/D4,14/D7]
O__4_1	56	REC_DACOUT_SEL/	[8/D4,14/C7]
O__4_2	58	ZONE_DACOUT_SEL/	[9/C4,14/C7]
O__4_3	59	MAIN_MUTE_RLY/	[10/A7]
O__4_4	60	HEADP_MUTE_RLY/	[16/A8]
O__4_5	61	REAR_DACOUT_SEL/	[13/C5,14/C7]
O__4_6	63	REC_AD_MIC_SEL/	[7/C8]
O__4_7	64	MAIN_DAC_RST/	[10/D7,11/D7,12/D7,13/D7]
O__5_0	65	REC_DAC_RST/	[8/D7]
O__5_1	66	ZONE_MUTE_RLY/	[8/A7]
O__5_2	67	MAIN_DAC_LATCH_0	[10/C7]
O__5_3	68	MAIN_DAC_LATCH_1	[11/C7]
O__5_4	70	MAIN_DAC_LATCH_2	[12/C7]
O__5_5	71	MAIN_DAC_LATCH_3	[13/C7]
O__5_6	72	REC_DAC_LATCH	[8/C7]
O__5_7	74		S2
O__6_0	76	VC_MUTE/	[4/C5,5/C5,6/C4,7/A7,8/B7,9/C7,9/B7]
O__6_1	77	MAIN_VC_ZCEN	[4/C5,5/C5,6/C4,7/A7,9/C7]
O__6_2	78	NC	
O__6_3	79	REC_VC_ZCEN	[8/B7]
O__6_4	81	NC	
O__6_5	82	ZONE_VC_ZCEN	[9/B7]
O__6_6	85	MAIN_ADC_RST/	[4/A4,5/A4,6/A4]
O__6_7	86	MAIN_ADC_96K_EN	[4/A4,5/B4,6/A4]
O__7_0	87	MAIN_ADC_192K_EN	[4/A4,5/B4,6/A4]
O__7_1	89	REC_ADC_RST/	[7/A2]
O__7_2	90	REC_ADC_96K_EN	[7/A2]
O__7_3	91	REC_ADC_192K_EN	[7/A2]
O__7_4	92	R200 56 ADA_SDATA_IN	[15/C6]
O__7_5	93	R201 56 TUN_SCLK	[15/A5]
TDO	83		U39 TDO

[4/D5,5/D5,6/D4,7/B7,8/B6,9/B6,10/C7,11/C7,12/C7,13/C7,15/C5]	ADA_SCLK	22 I/O_GCK1
[4/D5,8/C7,10/C7,11/C7,12/C7,13/C7,15/A5,15/C5]	ADA_SDATA_OUT	23 I/O_GCK2
[15/C5]	ADA_LATCH	27 I/O_GCK3
[4/D5,5/D5,6/C4,7/A7,8/B7,9/C7,9/B7,15/C5]	ADA_VC_SEL/	3 I/O_GTS1
		4 I/O_GTS2
S1 [15/C5]	RESET	99 I/O_GSR
[15/A2]	TUN_TUNED	94 I_0
[15/A2]	TUN_STEREO	95 I_1
[15/A2]	TUN_SDATA_OUT	96 I_2
		97 I_3
TDI		45 TDI
TCK		48 TCK
TMS		47 TMS

+3.3VD → R122 4.7K, R121 4.7K

R123 4.7K

GND (100, 84, 75, 69, 62, 44, 31, 21)

[16/A3] HEADP_PRES 11 → 10 U76 74LCX14; 13 → 12 U76 74LCX14

JTAG PROGRAMMING PORT

+5VD

J16

RED	VCC	1	
BLK	GND	2	
		3	NC
YEL	TCK	4	TCK
		5	NC
VIO	TDO	6	TDO
WHT	TDI	7	TDI
		8	NC
GRN	TMS	9	TMS

*

SPARES

U53 74VHC04: 9 → 8 NC

U53 74VHC04: 13 → 12 NC

CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS	DATE	TITLE	
DRAWN RWH	8/27/02	SCHEM,ANALOG I/O BD,RV8 CONTROL REGISTERS	
CHECKED CBV	8/28/02	SIZE B / CODE / NUMBER 060-15579	REV 3
Q.C. CW	8/29/02	FILE NAME 15579-6.14	SHEET 14 OF 17
ISSUED MAG	8/29/02		

10-7-2003 14:56

CONNECTORS TO AMPS

[10/B2] L_FRONT_AMP — FB24 — R295 2.74K 1% — FB21 — J18
[12/B2] L_SIDE_AMP — FB22 — R294 2.74K 1% — FB20 — J18 — FB23
[10/B2] R_FRONT_AMP — R206 2.74K 1% — J17
[12/B2] R_SIDE_AMP — R207 2.74K 1% — J17
[11/B2] CENTER_AMP — FB34 — R421 2.74K 1% — FB37 — J27
[15/B4] AMP_3_OUT — FB36 — R422 2.74K 1% — FB38 — J27 — FB35
[15/B4] AMP_7_OUT — R399 2.74K 1% — J21
E1 — R398 2.74K 1% — R397 2.74K 1% — J21

DIGITAL CONNECTOR FROM MAIN BOARD

J26
MAIN_FS256/ [10/C7,15/C3]
MAIN_I2S_OUT1 [11/C7,15/C3]
MAIN_I2S_OUT2 [12/C7,15/C3]
MAIN_I2S_OUT3 [13/C7,15/C3]
MAIN_I2S_OUT4
[4/A4,15/B5] MAIN_I2S_IN1
[5/A4,15/B5] MAIN_I2S_IN2
[6/A4,15/A5] MAIN_I2S_IN3
MAIN_FS64/ [4/A4,5/A4,6/A4,10/C7,11/D7,12/D7,13/D7,15/B3]
REC_DAC_I2S_OUT [8/D7,15/C3]
REC_ADC_FS64/ [7/A2,15/B3]
[7/A2,15/A5] MAIN_I2S_IN4
REC_DAC_FS64/ [8/D7,15/B3]
MAIN_FS/ [4/A4,5/A4,6/A4,10/C7,11/C7,12/C7,13/C7,15/C3]
REC_ADC_FS/ [7/A2,15/C3]
REC_DAC_FS/ [8/C7,15/C3]
[15/A2] TUN_RDS_DAT
[15/A2] TUN_RDS_CLK
[14/B3] ADA_SDATA_IN
ADA_TUN_CE/ [15/A5]
ADA_SDATA_OUT [4/D5,8/C7,10/C7,11/C7,12/C7,13/C7,14/B5,15/A5]
ADA_SCLK [4/D5,5/D5,6/D4,7/B7,8/B6,9/B6,10/C7,11/C7,12/C7,13/C7,14/B5]
ADA_LATCH [14/B5]
ADA_VC_SEL/ [4/D5,5/D5,6/C4,7/A7,8/B7,9/C7,9/B7,14/B5]
RESET [14/B5]

MAIN_FS256/ — U91 74LCX14 — R396 68.1 1%

+3.3VD — U95 74LVC1G04 — R409 68.1 1% — REC_ADC_MCKI/ [7/A2,15/B3]
+3.3VD — U94 74LVC1G04 — R408 68.1 1% — REC_DAC_MCKI/ [8/D7,15/B3]

CLOCK BUFFERS

+3.3VD — U91 74LCX14 — R395 68.1 1% — MAIN_ADC_MCKI [4/A4]
U91 74LCX14 — R393 68.1 1% — CSUB_ADC_MCKI [5/A4]
U91 74LCX14 — R394 68.1 1% — SIDE_ADC_MCKI [6/A4]
+3.3VD — U76 74LCX14 — R309 68.1 1% — FRONT_DAC_MCKI [10/D7]
U76 74LCX14 — R308 68.1 1% — CSUB_DAC_MCKI [11/D7]
U76 74LCX14 — R307 68.1 1% — SIDE_DAC_MCKI [12/D7]
U76 74LCX14 — R306 68.1 1% — REAR_DAC_MCKI [13/D7]

J20 *
1 MAIN_I2S_OUT1 [10/C7,15/D5]
2 MAIN_I2S_OUT2 [11/C7,15/D5]
3 MAIN_I2S_OUT3 [12/C7,15/D5]
4 MAIN_I2S_OUT4 [13/C7,15/D5]
5 REC_DAC_I2S_OUT [8/D7,15/D5]
6 MAIN_FS/ [4/A4,5/A4,6/A4,10/C7,11/C7,12/C7,13/C7,15/C5]
7 REC_DAC_FS/ [8/C7,15/C5]
8 REC_ADC_FS/ [7/A2,15/C5]
9 MAIN_FS64/ [4/A4,5/A4,6/A4,10/C7,11/D7,12/D7,13/D7,15/D5]
10 REC_DAC_FS64/ [8/D7,15/C5]
11 REC_ADC_FS64/ [7/A2,15/D5]
12 MAIN_FS256_BUF
13 REC_DAC_MCKI/ [8/D7,15/D4]
14 REC_ADC_MCKI/ [7/A2,15/D4]

INPUT SEL AMP 7 AND 3

DG411 U16: [13/B2] L_REAR_AMP; [13/B2] R_REAR_AMP
DG411 U14: [8/B3,16/B8] L_REC_AMP; [8/B3,16/B8] R_REC_AMP; [9/B3,16/C8] L_ZONE_AMP; [9/B3,16/B8] R_ZONE_AMP
[14/C3] REAR_AMP_SEL/
[14/C3] REC_AMP_SEL/
[14/C3] ZONE_AMP_SEL/

LEFT & RIGHT REAR
LEFT & RIGHT REC
LEFT & RIGHT ZONE

R406 100K — R390 100K

TL072 U93: R404 120 — C475 8200PF — R403 422 1% — R402 2.21K 1% — AMP_7_OUT [15/C8]; R407 2.21K 1%; R405 0 *
TL072 U90: R417 120 — C471 8200PF — R418 422 1% — R420 2.21K 1% — AMP_3_OUT [15/C8]; R392 2.21K 1%; R391 0 *

[4/A4,15/D6] MAIN_I2S_IN1
[5/A4,15/D6] MAIN_I2S_IN2
[6/A4,15/D6] MAIN_I2S_IN3
[7/A2,15/C6] MAIN_I2S_IN4
J22 *

[15/C5] ADA_TUN_CE/ — U96 74VHCT14 — R412 1.2K
[4/D5,8/C7,10/C7,11/C7,12/C7,13/C7,14/B5,15/C5] ADA_SDATA_OUT — U96 74VHCT14 — R411 1.2K
[14/A3] TUN_SCLK — U96 74VHCT14 — R410 1.2K

CONNECTOR FROM AUX PHONO BOARD

J23
MIC_OUT1 [3/B8]
MIC1_RET [3/B8]
MIC_OUT2 [3/B8]
MIC2_RET [3/B8]
RIAA_L [3/D8]
RIAA_LRET [3/D8]
RIAA_R [3/D8]
RIAA_RRET [3/D8]
75US_L [3/C8]
75US_LRET [3/C8]
75US_R [3/C8]
75US_RRET [3/C8]

CONNECTOR FROM TUNER MODULE

J24
FB28 TUN_TUNED [14/B5]
FB29 TUN_STEREO [14/B5]
TUNER_L [3/A8]
TUNER_RET [3/A8,3/A8]
TUNER_R [3/A8]
FB30 TUN_SDATA_OUT [14/B5]
FB31 TUN_RDS_CLK [15/C6]
FB32 TUN_RDS_DAT [15/C6]
FB33

SPARES

TL072 U93 — NC — U91 74LCX14 — U91 74LCX14

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 021107-00	RWH 11/14/02	CW 11/20/02
		CBV 11/20/02	MAG 11/21/02
2	CHANGED PER DCR 030407-00	RWH 5/21/03	CW 5/23/03
		CBV 5/23/03	MAG 5/23/03
3	CHANGED PER DCR 030729-00	RWH 9/29/03	CW 10/7/03
		CBV 10/6/03	MAG 10/7/03
4	CHANGED PER DCR 031125-00	RWH 1/14/04	ECM 1/30/04
		CBV 1/30/04	MAG 2/2/04
5	CHANGED R391, 405 PER ECO 040421-00	RWH 4/27/04	CW 4/29/04
		CBV 4/28/04	KAB 5/2/04

CONTRACT NO.

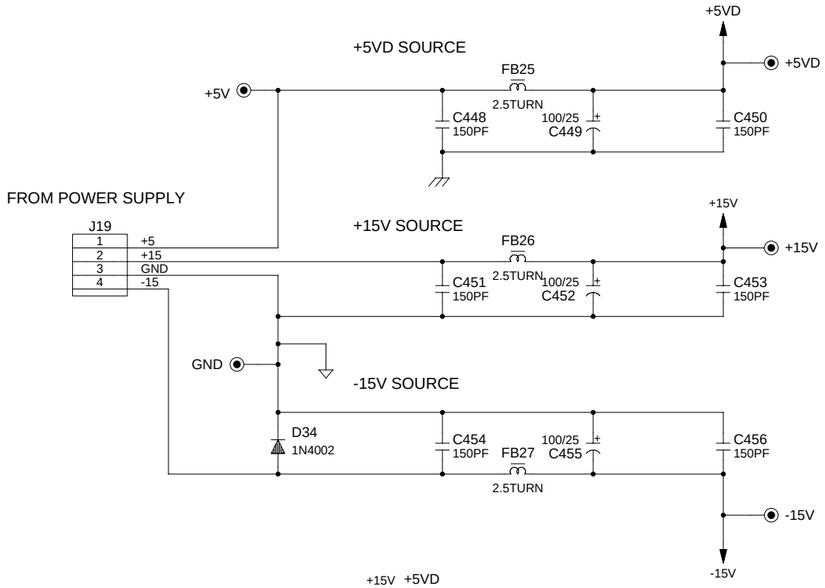
Lexicon
3 OAK PARK
BEDFORD, MA 01730

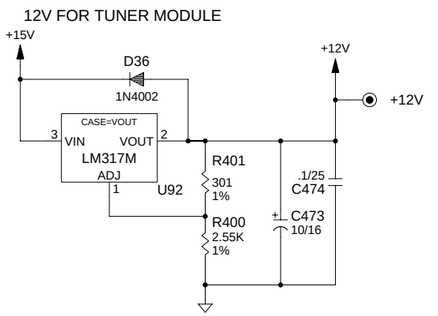
APPROVALS		DATE
DRAWN	RWH	8/27/02
CHECKED	CBV	8/28/02
Q.C.	CW	8/29/02
ISSUED	MAG	8/29/02

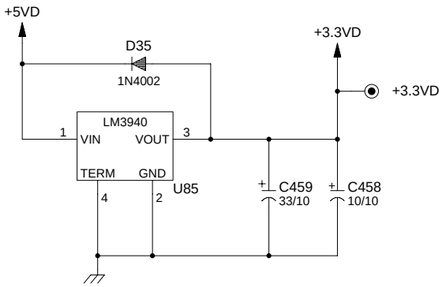
TITLE: SCHEM,ANALOG I/O BD,RV8
MAIN - AUX - AMP CONNS
SIZE B | CODE | NUMBER 060-15579 | REV 5
FILE NAME 15579-6.15 | SHEET 15 OF 17

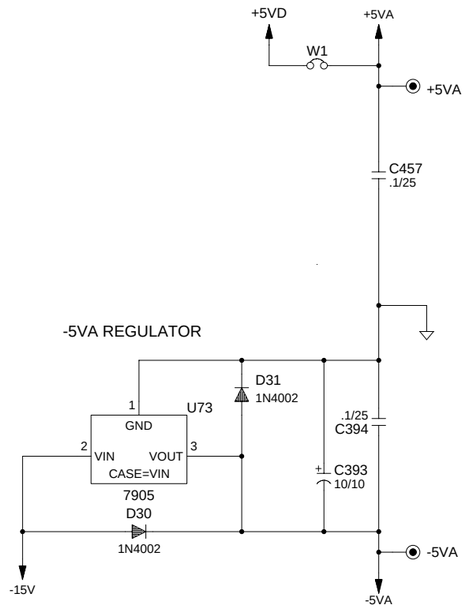
5-4-2004 8:43

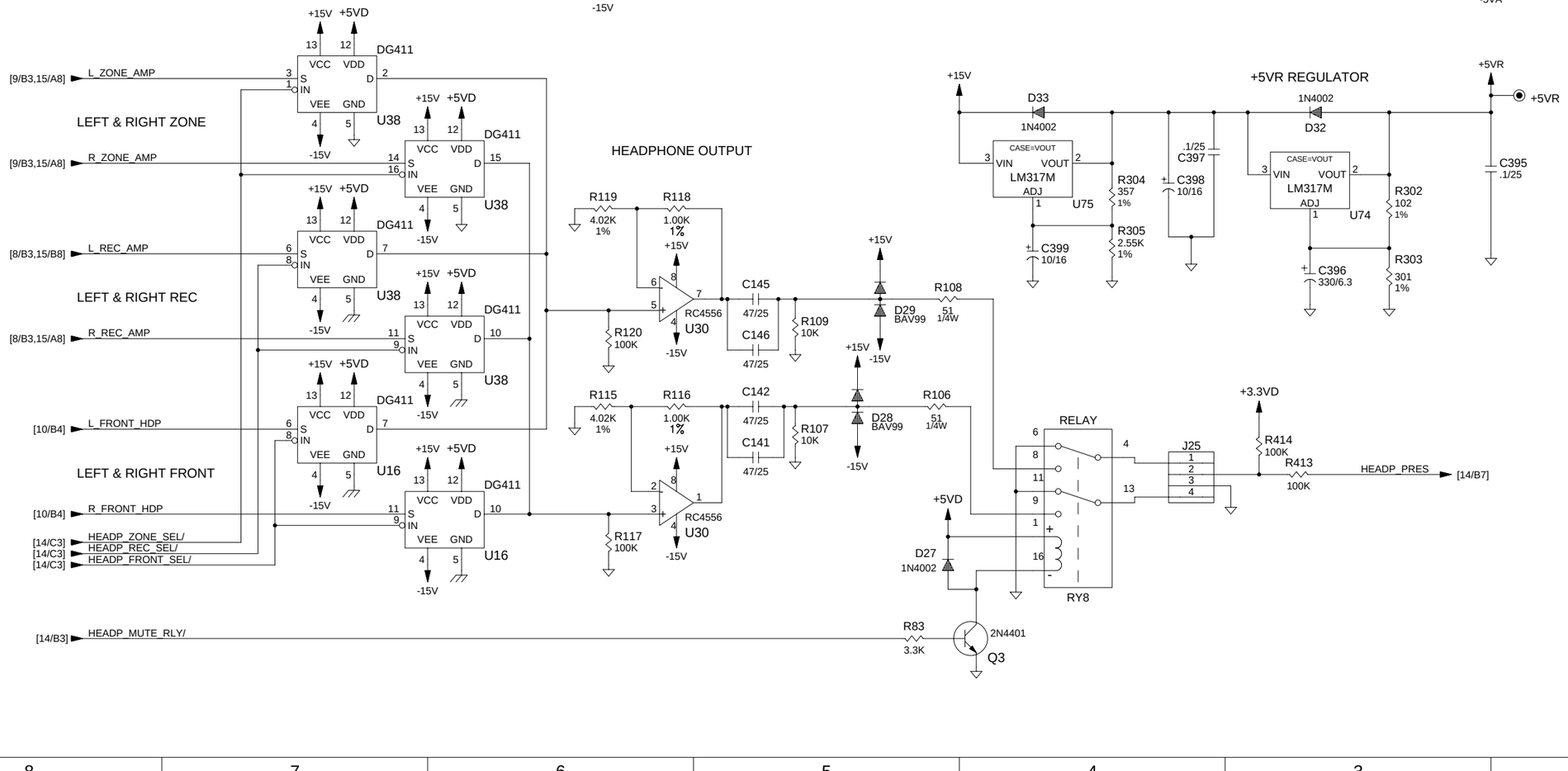
REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 021107-00	RWH 11/14/02	CW 11/20/02
		CBV 11/20/02	MAG 11/21/02
2	CHANGED PER DCR 030407-00	RWH 5/21/03	CW 5/23/03
		CBV 5/23/03	MAG 5/23/03
3	CHANGED PER DCR 030729-00	RWH 9/29/03	CW 10/7/03
		CBV 10/6/03	MAG 10/7/03

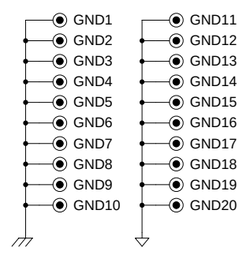








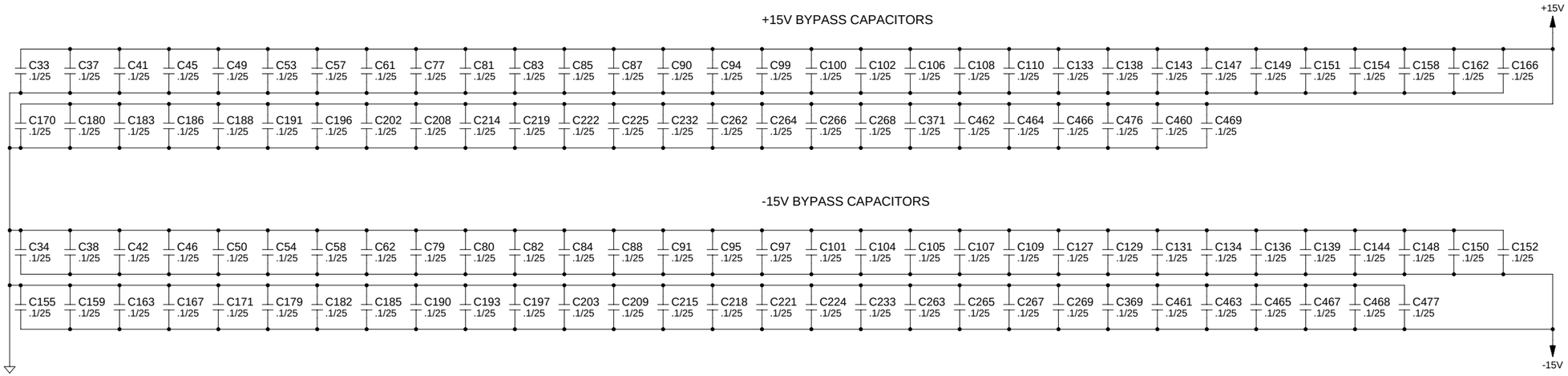




CONTRACT NO.	lexicon 3 OAK PARK BEDFORD, MA 01730		
APPROVALS		DATE	TITLE: SCHEM,ANALOG I/O BD,RV8 POWER SUPPLY & HEADPHONE
DRAWN	RWH	8/27/02	
CHECKED	CBV	8/28/02	SIZE B / CODE / NUMBER 060-15579 / REV 3
Q.C.	CW	8/29/02	
ISSUED	MAG	8/29/02	FILE NAME 15579-6.16 / SHEET 16 OF 17

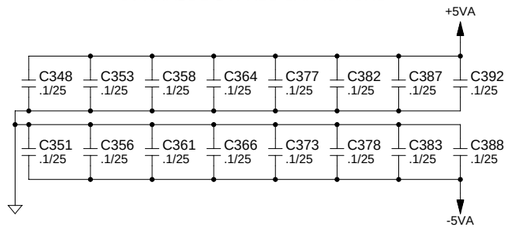
10-7-2003 11:05

+15V BYPASS CAPACITORS

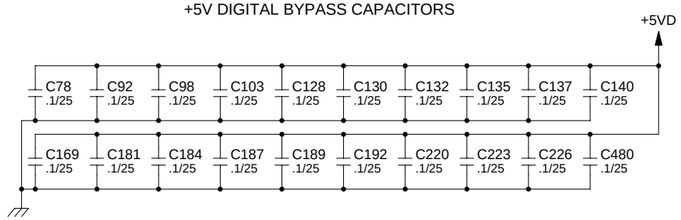


-15V BYPASS CAPACITORS

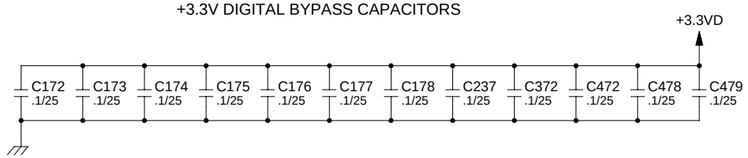
+/-5V ANALOG BYPASS CAPACITORS



+5V DIGITAL BYPASS CAPACITORS



+3.3V DIGITAL BYPASS CAPACITORS



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 021107-00	RWH 11/14/02	CW 11/20/02
		CBV 11/20/02	MAG 11/21/02
2	CHANGED PER DCR 030407-00	RWH 5/21/03	CW 5/23/03
		CBV 5/23/03	MAG 5/23/03
3	CHANGED PER DCR 030729-00	RWH 9/29/03	CW 10/7/03
		CBV 10/6/03	MAG 10/7/03

CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	8/27/02
CHECKED	CBV	8/28/02
Q.C.	CW	8/29/02
ISSUED	MAG	8/29/02

TITLE
SCHEM,ANALOG I/O BD,RV8
BYPASS CAPACITORS

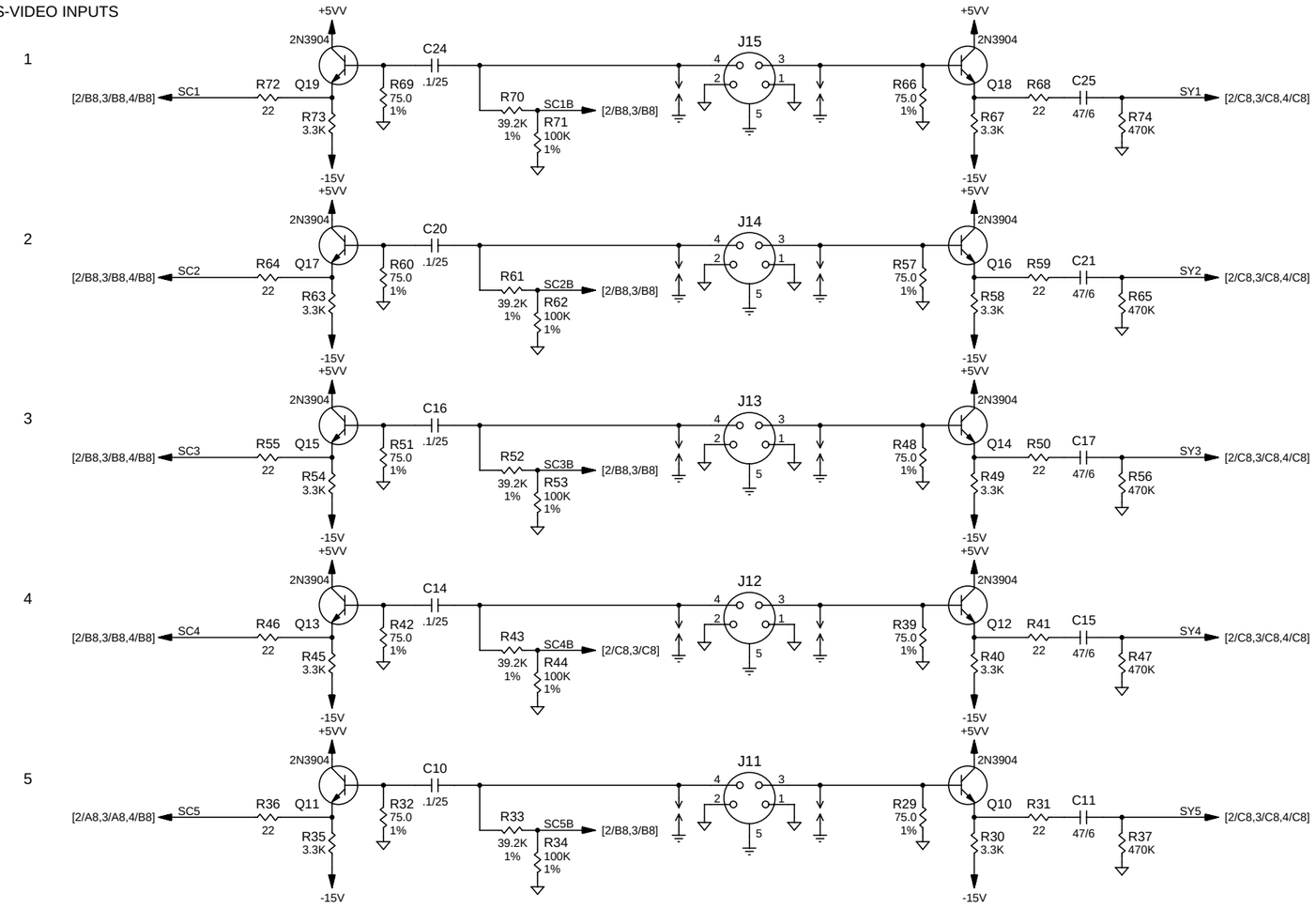
SIZE	CODE	NUMBER	REV
B		060-15579	3

FILE NAME 15579-6.17

SHEET 17 OF 17

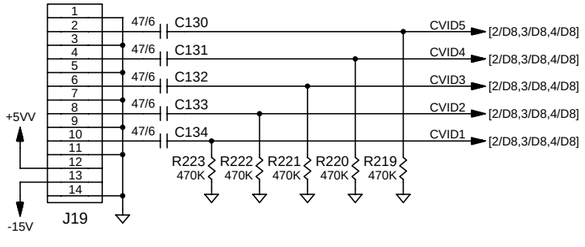
10-7-2003_11:05

S-VIDEO INPUTS



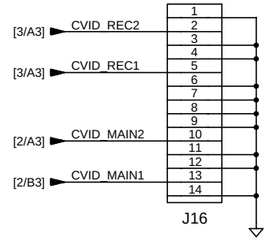
COMPOSITE VIDEO INPUTS

VIDEO INPUT BOARD CONNECTOR



COMPOSITE VIDEO OUTPUTS

VIDEO OUTPUT BOARD CONNECTOR



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 030106-00	RWH 1/13/03	CW 1/23/03
		ECM 1/21/03	MAG 1/23/03
2	CHANGED PER DCR 030421-00	RWH 5/20/03	CW 5/22/03
		ECM 5/20/03	MAG 5/22/03
3	CHANGED PER DCR 030623-00	RWH 10/8/03	CW 10/16/03
		ECM 10/9/03	MAG 10/16/03

REFERENCE COPY

NOTES

1 UNLESS OTHERWISE INDICATED, RESISTORS ARE 1/10W

2 UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%

3 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V.

4 DIGITAL GROUND, ANALOG GROUND, CHASSIS GROUND, POWER GROUND

5 [XX/XX] DENOTES [SHEET NUMBER/SECTOR]

6 LAST REFERENCE DESIGNATORS USED: C183, D11, E3, FB11, J20, L7, Q26, R255, RP1, RY6, U42, Y1.

7 COMPONENTS MARKED WITH * ARE NOT INSTALLED.

Notation:
CVID: composite video
SVID: s-video
PVID: component video

DOCUMENT CONTROL BLOCK: #060-15589		
SHEET	REVISION	TITLE
1 OF 10	3	S-VIDEO IN, COMPOSITE IN/OUT
2 OF 10	3	MAIN
3 OF 10	3	ZONE 2
4 OF 10	3	ZONE 3
5 OF 10	3	VIDEO CONVERSION
6 OF 10	3	COMPONENT VIDEO
7 OF 10	3	ON-SCREEN DISPLAY
8 OF 10	3	SYNC STRIPPER
9 OF 10	3	CPLD CONTROL REGISTERS, PLL
10 OF 10	3	POWER, INTERFACE CONNS

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CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	8/9/02
CHECKED	ECM	8/28/02
Q.C.	CW	8/28/02
ISSUED	MAG	8/28/02

TITLE
SCHEM,VIDEO BD, RV8
S-VIDEO IN, COMPOSITE IN/OUT

SIZE	CODE	NUMBER	REV
B		060-15589	3

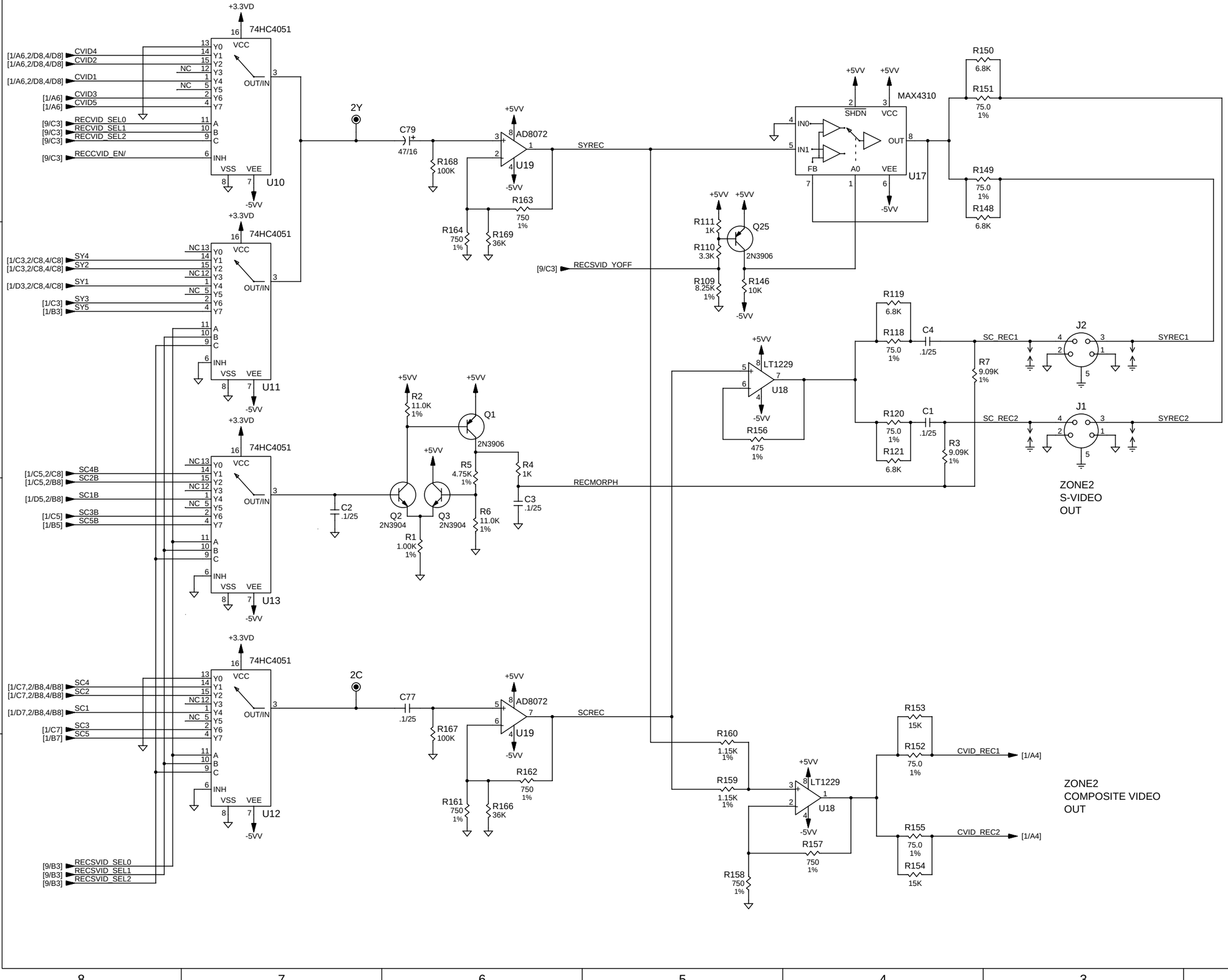
FILE NAME 15589-3 .1 SHEET 1 OF 10

10-16-2003 16:26

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 030106-00	RWH 1/13/03	CW 1/23/03
		ECM 1/21/03	MAG 1/23/03
2	CHANGED PER DCR 030421-00	RWH 5/20/03	CW 5/22/03
		ECM 5/20/03	MAG 5/22/03
3	CHANGED PER DCR 030623-00	RWH 10/8/03	CW 10/16/03
		ECM 10/9/03	MAG 10/16/03

CONTRACT NO.	Lexicon 3 OAK PARK BEDFORD, MA 01730		
APPROVALS	DATE	TITLE SCHEM,VIDEO BD, RV8 MAIN	
DRAWN RWH	8/9/02		
CHECKED ECM	8/28/02	SIZE B / CODE / NUMBER 060-15589 / REV 3	
Q.C. CW	8/28/02		
ISSUED MAG	8/28/02	FILE NAME 15589-3 . 2 / SHEET 2 OF 10	

10-16-2003_16:28



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 030106-00	RWH 1/13/03	CW 1/23/03
		ECM 1/21/03	MAG 1/23/03
2	CHANGED PER DCR 030421-00	RWH 5/20/03	CW 5/22/03
		ECM 5/20/03	MAG 5/22/03
3	CHANGED PER DCR 030623-00	RWH 10/8/03	CW 10/16/03
		ECM 10/9/03	MAG 10/16/03

CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

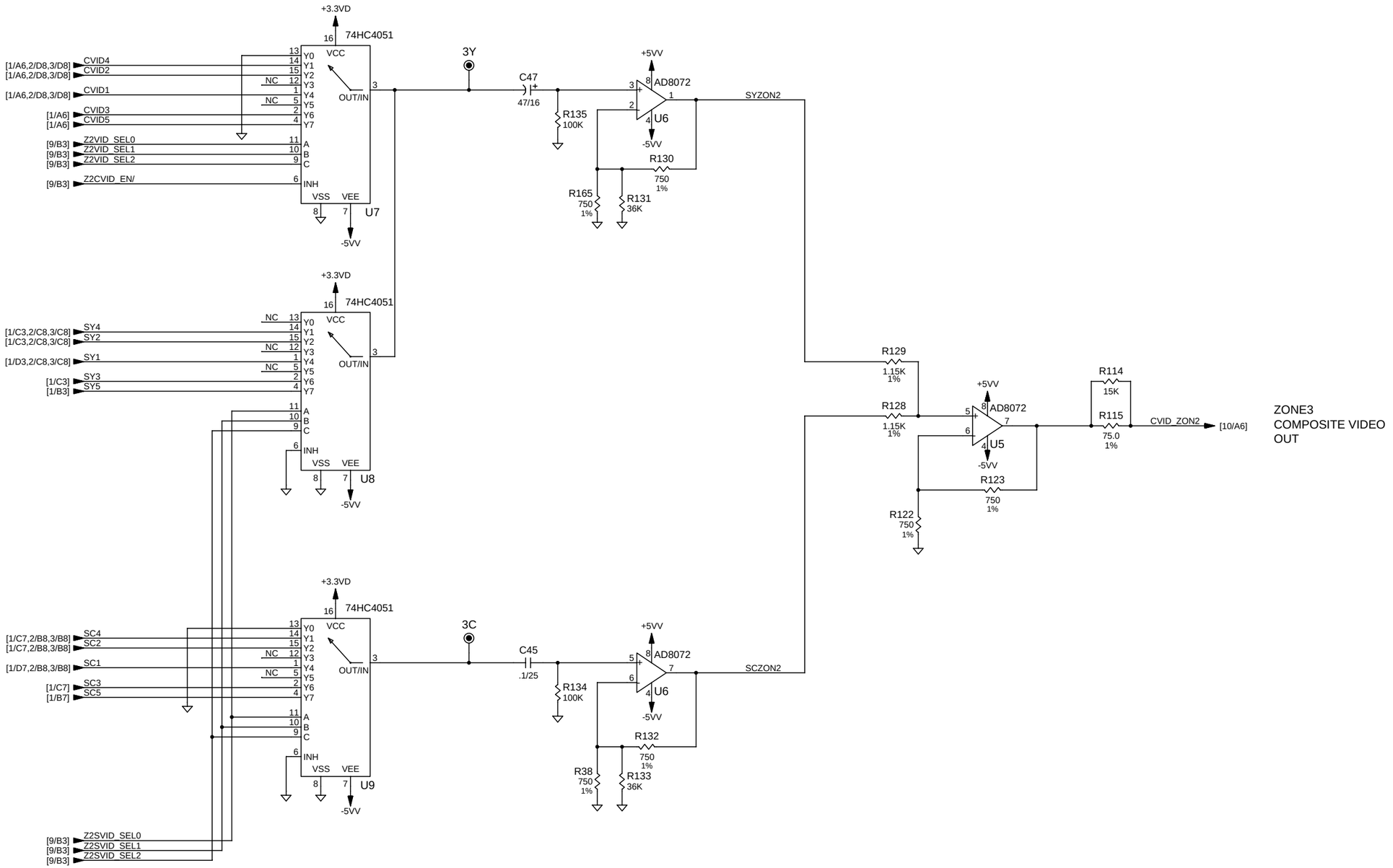
APPROVALS		DATE
DRAWN	RWH	8/9/02
CHECKED	ECM	8/28/02
Q.C.	CW	8/28/02
ISSUED	MAG	8/28/02

TITLE: SCHEM,VIDEO BD, RV8
ZONE 2

SIZE	CODE	NUMBER	REV
B		060-15589	3

FILE NAME: 15589-3 .3
SHEET 3 OF 10

10-16-2003_16:28



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 030106-00	RWH 1/13/03	CW 1/23/03
		ECM 1/21/03	MAG 1/23/03
2	CHANGED PER DCR 030421-00	RWH 5/20/03	CW 5/22/03
		ECM 5/20/03	MAG 5/22/03
3	CHANGED PER DCR 030623-00	RWH 10/8/03	CW 10/16/03
		ECM 10/9/03	MAG 10/16/03

CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	8/9/02
CHECKED	ECM	8/28/02
Q.C.	CW	8/28/02
ISSUED	MAG	8/28/02

TITLE
SCHEM,VIDEO BD, RV8
ZONE 3

SIZE	CODE	NUMBER	REV
B		060-15589	3

FILE NAME 15589-3 . 4

SHEET 4 OF 10

10-16-2003_16:28

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 030106-00	RWH 1/13/03	CW 1/23/03
		ECM 1/21/03	MAG 1/23/03
2	CHANGED PER DCR 030421-00	RWH 5/20/03	CW 5/22/03
		ECM 5/20/03	MAG 5/22/03
3	CHANGED PER DCR 030623-00	RWH 10/8/03	CW 10/16/03
		ECM 10/9/03	MAG 10/16/03

VIDEO DECODER

VIDEO ENCODER

+3.3VD +3.3VD

R230 10K R231 10K

[10/A6] VID_I2C_SDATA

[10/A6] VID_I2C_SCLK

[2/D5,7/D8] OSD_Y_IN R210 205 1% C156 .056/50 P13 AI11

R236 110 1%

[2/A5,7/C8] OSD_C_IN R213 205 1% C153 .056/50 P10 AI21

R234 110 1%

R232 1M

[2/D3] SY_MAIN1_D R143 205 1% C154 .056/50 P11 AI12

R235 110 1%

SC_MAIN1_D R140 205 1% C152 .056/50 P9 AI22

R233 110 1%

NC P7 AI23

NC P6 AI24

C151 .056/50 P8 AI2D

C155 .056/50 P12 AI1D

AOUT M10 AOUT

SAA-7109E DECODER

SDA_D L12
SCL_D M11

PD[7:0]

XPD7 K2 PD7
XPD6 K3 PD6
XPD5 L1 PD5
XPD4 L2 PD4
XPD3 L3 PD3
XPD2 M1 PD2
XPD1 M2 PD1
XPD0 N1 PD0

XTRI K1 — PLAYSPEED [9/C6]
XRV L5 — XRV — R226 47 DEC_XRH [6/D7,9/B7]
XRH N2
XCLK M3 — XCLK
XDQ M4 NC
XRDY N3 NC

R224 47 XCLK [9/B6]

HPD7 A13 NC
HPD6 D12 NC
HPD5 C12 NC
HPD4 B12 NC
HPD3 A12 NC
HPD2 C11 NC
HPD1 B11 NC
HPD0 A11 NC

IPD7 E14 NC
IPD6 D14 NC
IPD5 C14 NC
IPD4 B14 NC
IPD3 E13 NC
IPD2 D13 NC
IPD1 C13 NC
IPD0 B13 NC

ITRI G14 NC
IGPV F13 NC
IGPH G12 NC
IGP1 G13 NC
IGP0 F14 NC
ICLK H12 NC
IDQ H14 NC
ITRDY J14 NC

AMXCLK J12 NC
ALRCLK J13 NC
ASCLK K14 NC
AMCLK K12 NC

RTCO L13 NC
RTS0 K13 — DEC_HS/ [9/C6]
RTS1 L10 — DEC_VS/ [6/D7,9/C6]

LLC2 L14 NC
LLC M14 NC

RES_D M12 NC
CE N14 — DEC_RES/ [9/B3]

TMS_D M5 NC
TCLK_D M6 NC
TRST_D N4
TDI_D N6 NC
TDO_D N5 NC

TEST5 J2 NC
TEST4 J1 NC
TEST3 J3 NC
TEST2 C10 NC
TEST1 B10 NC
TEST0 H13 NC

XTALOUT_D P4 NC
XTALO_D P3 NC
XTALI_D P2

U34

[10/D7] 3.3VA_D

R225 10K C144 .1/25

24.576MHZ 4 VDD 3.3V 1 IN 3 OUT GND 2

U33

SAA-7109E ENCODER

G2 SDA_E
E2 SCL_E

NC C1 PD11
NC C2 PD10
NC B1 PD9
NC B2 PD8

PD7 A2 PD7
PD6 B4 PD6
PD5 B3 PD5
PD4 A3 PD4
PD3 F3 PD3
PD2 H1 PD2
PD1 H2 PD1
PD0 H3 PD0

RP1 5 4 3.3K HSIO E3 HSVGC
RP1 6 3 3.3K VSIO F1 VSVGC
RP1 7 2 3.3K FSIO G1 FSVGC
RP1 8 1 3.3K CBO/ G3 CBO

R227 3.3K TTXRQ C3 TTX/SRES
C4 TTXRQ/XCLKO2

NC G4 PIXCLKO
F2 PIXCLKI

NC D3 TMS_E
NC E1 TCK_E
A4 TRST_E
NC B5 TDI_E
NC D1 TDO_E

[9/B3] ENC_RES/ D2 RES_E

NC A6 XTALO_E
[9/B3] ENC_27MHZ A5 XTALI_E

R-CR-C C8 DAC_PR [6/C6]
G-VBS-CVBS C7 DAC_Y [6/D6]
B-CB-CVBS C6 DAC_PB [6/C6]

HCSOUT D8 NC
VSOUT D7 NC

RSET A9 — R229 1.00K 1%

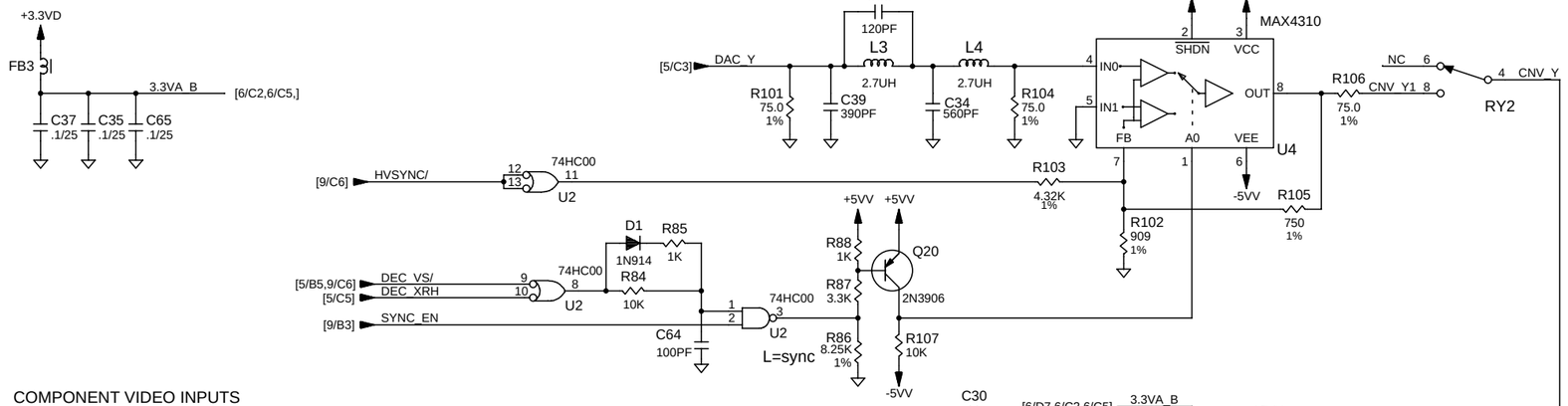
DUMPA A7
DUMPB B7 — R228 12

U34

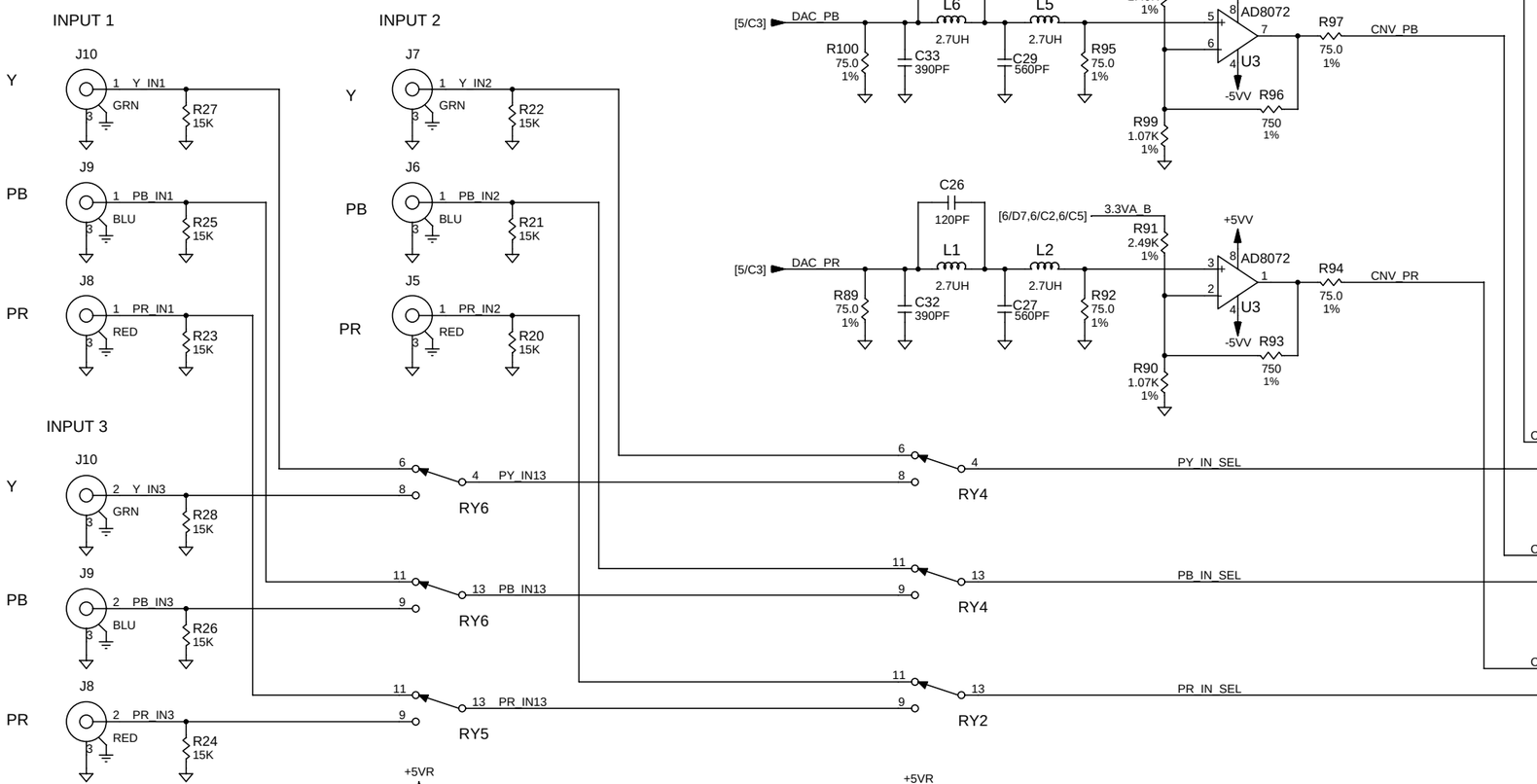
CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS	DATE	TITLE: SCHEM,VIDEO BD, RV8 VIDEO CONVERSION	
DRAWN RWH	8/9/02		
CHECKED ECM	8/28/02	SIZE B / CODE / NUMBER 060-15589 / REV 3	
Q.C. CW	8/28/02		
ISSUED MAG	8/28/02	FILE NAME 15589-35 / SHEET 5 OF 10	

10-16-2003_16:28

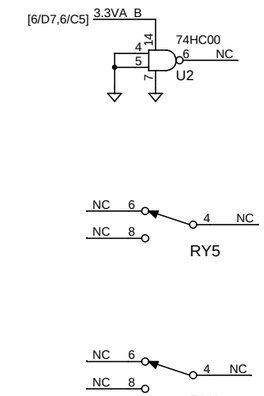
COMPONENT ENCODER FILTERS



COMPONENT VIDEO INPUTS



SPARES



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 030106-00	RWH 1/13/03	CW 1/23/03
		ECM 1/21/03	MAG 1/23/03
2	CHANGED PER DCR 030421-00	RWH 5/20/03	CW 5/22/03
		ECM 5/20/03	MAG 5/22/03
3	CHANGED PER DCR 030623-00	RWH 10/8/03	CW 10/16/03
		ECM 10/9/03	MAG 10/16/03

CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	8/9/02
CHECKED	ECM	8/28/02
Q.C.	CW	8/28/02
ISSUED	MAG	8/28/02

TITLE: SCHEM,VIDEO BD, RV8
COMPONENT VIDEO

SIZE	CODE	NUMBER	REV
B		060-15589	3

FILE NAME: 15589-3 . 6
SHEET 6 OF 10

10-16-2003_16:28

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 030106-00	RWH 1/13/03	CW 1/23/03
		ECM 1/21/03	MAG 1/23/03
2	CHANGED PER DCR 030421-00	RWH 5/20/03	CW 5/22/03
		ECM 5/20/03	MAG 5/22/03
3	CHANGED PER DCR 030623-00	RWH 10/8/03	CW 10/16/03
		ECM 10/9/03	MAG 10/16/03

ON-SCREEN DISPLAY

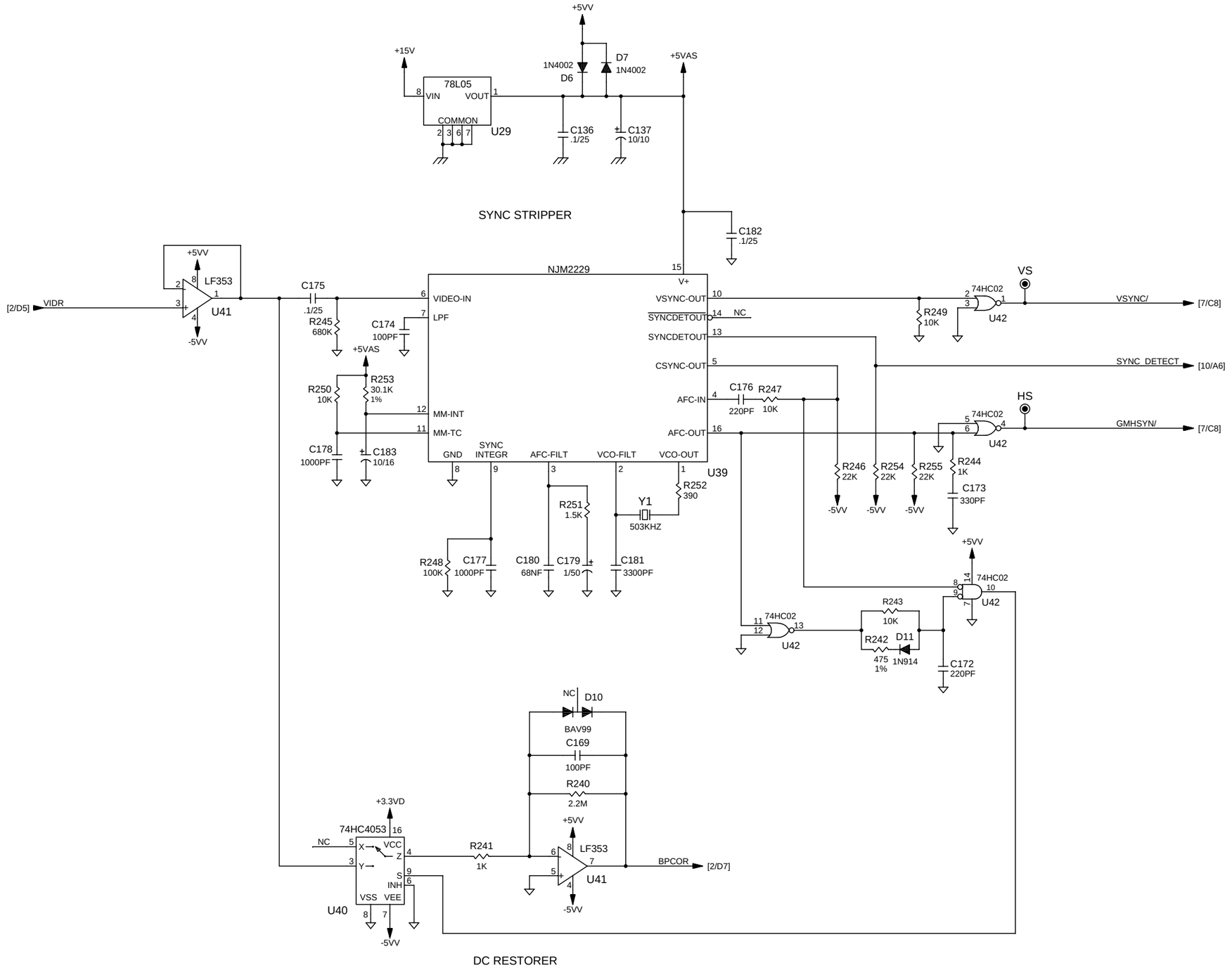
4XFSC OSCILLATORS

FONT MEMORY

CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS	DATE	TITLE: SCHEM,VIDEO BD, RV8 ON-SCREEN DISPLAY	
DRAWN RWH	8/9/02	SIZE B / CODE / NUMBER 060-15589 / REV 3	
CHECKED ECM	8/28/02		
Q.C. CW	8/28/02	FILE NAME 15589-37	SHEET 7 OF 10
ISSUED MAG	8/28/02		

10-16-2003 16:28

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 030106-00	RWH 1/13/03	CW 1/23/03
		ECM 1/21/03	MAG 1/23/03
2	CHANGED PER DCR 030421-00	RWH 5/20/03	CW 5/22/03
		ECM 5/20/03	MAG 5/22/03
3	CHANGED PER DCR 030623-00	RWH 10/8/03	CW 10/16/03
		ECM 10/9/03	MAG 10/16/03



CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS	DATE	TITLE	SCHEM,VIDEO BD, RV8 SYNC STRIPPER
DRAWN RWH	8/9/02	SIZE B	CODE
CHECKED ECM	8/28/02	NUMBER 060-15589	REV 3
Q.C. CW	8/28/02	FILE NAME 15589-3 . 8	SHEET 8 OF 10
ISSUED MAG	8/28/02		

10-16-2003_16:28

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 030106-00	RWH 1/13/03	CW 1/23/03
		ECM 1/21/03	MAG 1/23/03
2	CHANGED PER DCR 030421-00	RWH 5/20/03	CW 5/22/03
		ECM 5/20/03	MAG 5/22/03
3	CHANGED PER DCR 030623-00	RWH 10/8/03	CW 10/16/03
		ECM 10/9/03	MAG 10/16/03

[10/A5] VIDEO_DATA
[10/A5] VIDEO_SCLK
[10/A5] OSD_CS/
[10/A5] VIDEO_REG/

JTAG PROGRAMMING PORT

J17: RED VCC, BLK GND, YEL TCK, VIO TDO, WHT TDI, GRN TMS, NC

+3.3VD +3.3VD +3.3VD
R81 4.7K, R83 4.7K, R82 4.7K

JTAG_TCK, JTAG_TDO, JTAG_TDI, JTAG_TMS

XC95144XL

+3.3VD
VCCINT1 5, VCCINT2 57, VCCINT3 98, VCCIO1 26, VCCIO2 38, VCCIO3 51, VCCIO4 88

SDATI 92
SDATCLK , GCK1 22
OSD_CS 68
REG_CS 87
TCK 48
TDO 83
TDI 45
TMS 47

D[7:0] [7/B3]
A[15:0] [7/B3]

FLASH INTERFACE

OSD_TSC 90
VROM_WR 1

U35 74VHCT08
OSD_TSC/ 12, 13, 11 OSD_TSC5/ [7/B8]
VROM_WR/ [7/A4]

MVID_SEL0 77 [2/D8]
MVID_SEL1 81 [2/D8]
MVID_SEL2 79 [2/D8]
MCVID_EN 78 [2/D8]
MSVID_YOFF 82 [7/C2]
MORPHEN1 41 [2/C6]
MTHRU 58 [2/A5]
HINH 89 NC

RECVID_SEL0 93 [3/D8]
RECVID_SEL1 70 [3/D8]
RECVID_SEL2 71 [3/D8]
RECCVID_EN 76 [3/D8]
RECSVID_YOFF 37 [3/C6]
NTSC_EN 61 [7/B4]
PAL_EN 60 [7/A4]
SECAM_EN 94 [7/C6]

P_SEL0 40 [6/A7]
P_SEL1 35 [6/A4]
P_SEL2 39 [6/A6]
MORPHEN 36 [2/B6]

Z2VID_SEL0 95 [4/D8]
Z2VID_SEL1 63 [4/D8]
Z2VID_SEL2 64 [4/D8]
Z2CVID_EN 59 [4/D8]
DEC_RES 86 [5/B5]
ENC_RES 85 [5/B4]
SYNC_EN 42 [6/C7]
PLL_BYP 49 NC

MSVID_SEL0 53 [2/A8]
MSVID_SEL1 54 [2/A8]
MSVID_SEL2 55 [2/A8]
MSTHRU 33 [2/D5]

RECSVID_SEL0 56 [3/A8]
RECSVID_SEL1 72 [3/A8]
RECSVID_SEL2 74 [3/A8]

Z2SVID_SEL0 65 [4/A8]
Z2SVID_SEL1 66 [4/A8]
Z2SVID_SEL2 67 [4/A8]

ENC27M 52 R79 47 ENC_27MHZ [5/B4]
ENC15K 50
OSDSCLK 91

[5/B5] DEC_HS/
[5/B5,6/D7] DEC_VS/
[6/D7] HVSYNC/
[5/C5] PLAYSPEED
DEC_HS 2
DEC_VS 19
HVSYNC 34
PLAYSPEED 80

[10/A5] VIDEO_RST/ 99 RESETN , GSR
[5/C5] XCLK 7 DEC27M

NC 43 SPARE1
NC 46 SPARE2
NC 73 SPARE3

GND1 21, GND2 31, GND3 44, GND4 62, GND5 69, GND6 75, GND7 84, GND8 100

U14

+5VV
OSD_SCLKG 1, 2, 14 U35 74VHCT08 3 OSD_SCLK5 [7/B8]
OSD_CS/ 9, 10, 8 U35 74VHCT08 OSD_CS5/ [7/B8]
VIDEO_DATA 4, 5, 6 U35 74VHCT08 VIDEO_DATA5 [7/B8]

+3.3VD
FB2, FB1
C59 .1/25, C58 .1/25

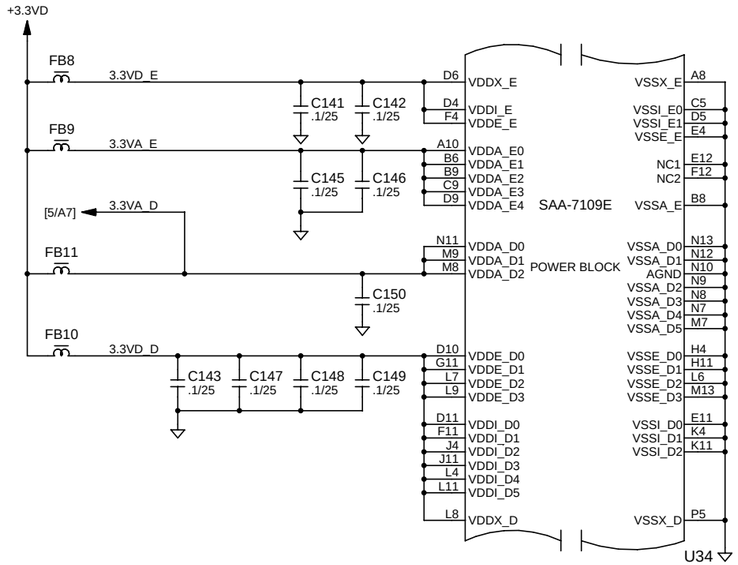
TLC2933
XRH
[5/C5] DEC_XRH
ENCH
ENC_15KHZ
VDDL, VDDV, BIAS, FIN_A, FIN_B, V_OUT, P_OUT, VCO_IN, TEST, PFD_INH, GNDL, NC, VCO_INH, GNDV
R77 2.2K, C57 .1/25, R80 47, R78 47K, R76 1.2K, R75 1M
C55 .1/25, C56 1/50, C54 47/16
VCOV
U1

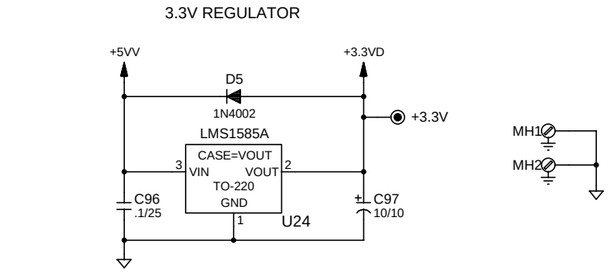
ENCODER CLOCK PLL

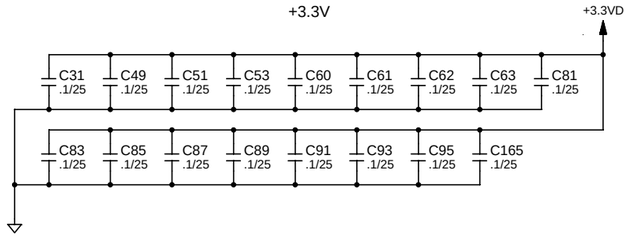
CONTRACT NO.	Lexicon 3 OAK PARK BEDFORD, MA 01730		
APPROVALS	DATE	TITLE: SCHEM,VIDEO BD, RV8 CPLD CONTROL REGISTERS,PLL	
DRAWN RWH	8/9/02	SIZE B / CODE / NUMBER 060-15589 / REV 3	
CHECKED ECM	8/28/02		
Q.C. CW	8/28/02		
ISSUED MAG	8/28/02	FILE NAME 15589-3 . 9 / SHEET 9 OF 10	

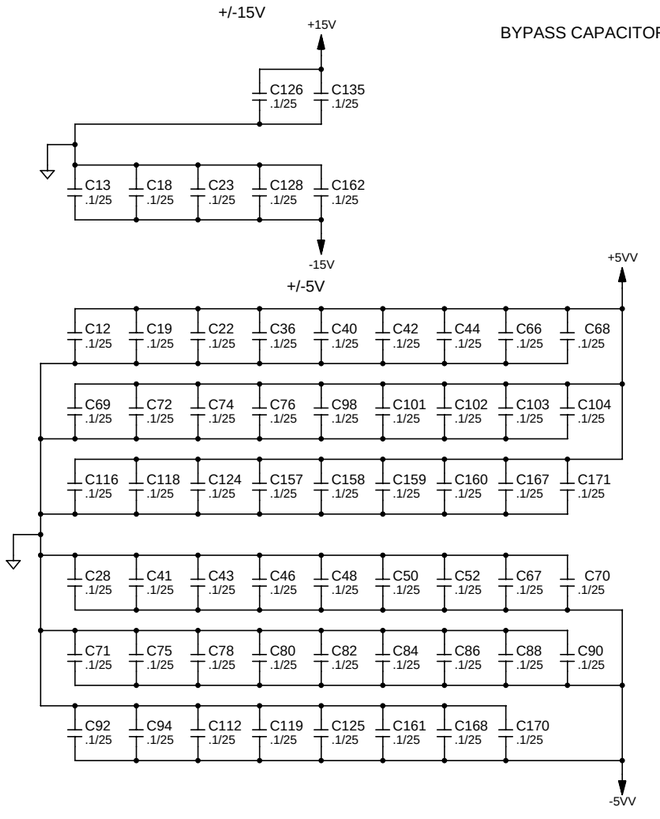
10-16-2003_16:28

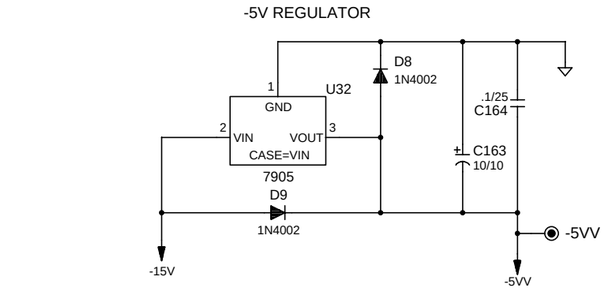
REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 030106-00	RWH 1/13/03	CW 1/23/03
		ECM 1/21/03	MAG 1/23/03
2	CHANGED PER DCR 030421-00	RWH 5/20/03	CW 5/22/03
		ECM 5/20/03	MAG 5/22/03
3	CHANGED PER DCR 030623-00	RWH 10/8/03	CW 10/16/03
		ECM 10/9/03	MAG 10/16/03

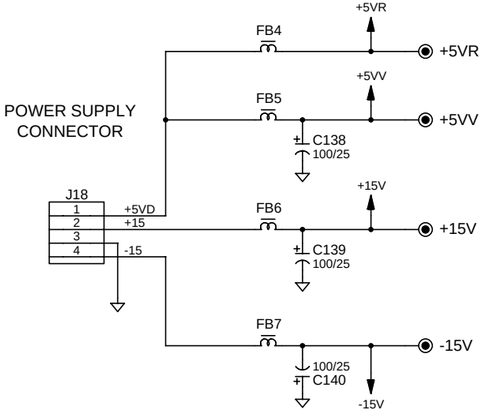


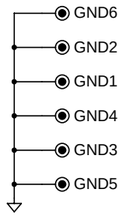


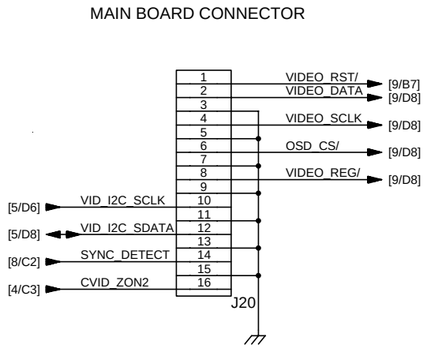






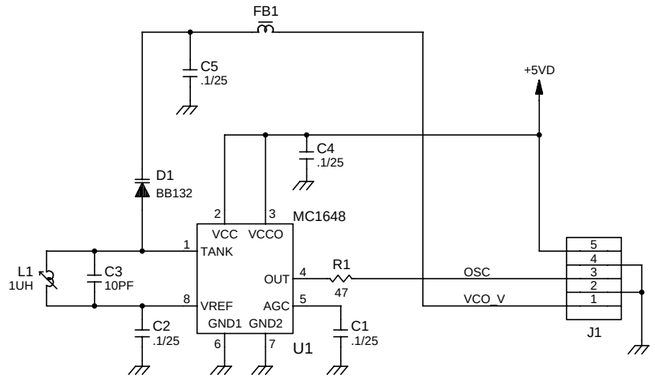






CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS	DATE	TITLE: SCHEM,VIDEO BD, RV8 POWER, INTERFACE CONNS	
DRAWN RWH	8/9/02		
CHECKED ECM	8/28/02	SIZE B / CODE / NUMBER 060-15589 / REV 3	
Q.C. CW	8/28/02		
ISSUED MAG	8/28/02	FILE NAME 15589-3 .10 / SHEET 10 OF 10	

10-16-2003 16:29



REVISIONS

REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.

NOTES

1 UNLESS OTHERWISE INDICATED, RESISTORS ARE 1/10W

2 UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%

3 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V

4 DIGITAL GROUND ANALOG GROUND CHASSIS GROUND POWER GROUND

5 LAST REFERENCE DESIGNATORS USED: C5, D1, FB1, J1, L1, R1, U1.

REFERENCE COPY

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CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	3/3/03
CHECKED	ECM	3/5/03
Q.C.	CW	3/7/03
ISSUED	KAB	3/11/03

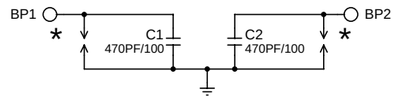
TITLE: SCHEM, VCO BD, MCLK

SIZE	CODE	NUMBER	REV
B		060-16139	0

FILE NAME: 16139-0.1 SHEET 1 OF 1

3-18-2003_9:15

BINDING POST FILTER



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.

NOTES

1 ⏚ DIGITAL GROUND ⏚ ANALOG GROUND ⏚ CHASSIS GROUND ⏚ POWER GROUND

2 LAST REFERENCE DESIGNATORS USED: BP2,C2

3 COMPONENTS MARKED WITH * ARE NOT INSTALLED.

REFERENCE COPY

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CONTRACT NO.

Lexicon

3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	5/1/03
CHECKED	ECM	5/1/03
Q.C.	CW	5/8/03
ISSUED	MAG	5/8/03

TITLE: SCHEM,SPKR EMI FILTER BD, RV8

SIZE	CODE	NUMBER	REV
B		060-16189	0

FILE NAME: 16189-0 .1

SHEET 1 OF 1

5-12-2003_9:05

Harman Specialty Group 3 Oak Park, Bedford, MA, 01730-1413 USA
Customer Service: Telephone: 781-280-0300 | Service Fax: 781-280-0499 | www.lexicon.com

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